

1.2V Drive Nch+Pch MOSFET

EM6M2

●Structure

Silicon N-channel MOSFET /
 Silicon P-channel MOSFET

●Features

- 1) Nch MOSFET and Pch MOSFET are put in EMT6 package.
- 2) High-speed switching.
- 3) Low voltage drive (1.2V drive).
- 4) Built-in G-S Protection Diode.

●Applications

Switching

●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6M2		○

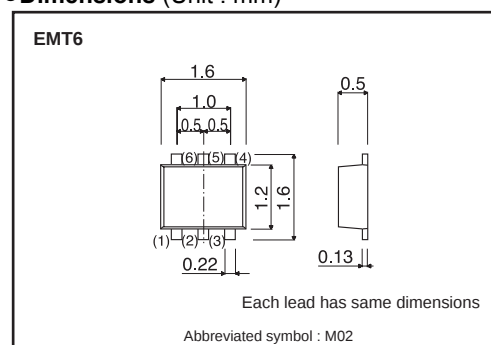
●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
		Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage	V_{DS}	20	-20	V
Gate-source voltage	V_{GS}	±8	±10	V
Drain current	Continuous	I_D	±200	mA
	Pulsed	I_{DP}^{*1}	±400	mA
Total power dissipation	P_D^{*2}	150		mW / TOTAL
		120		mW / ELEMENT
Channel temperature	T_{ch}	150		°C
Range of storage temperature	T_{stg}	-55 to +150		°C

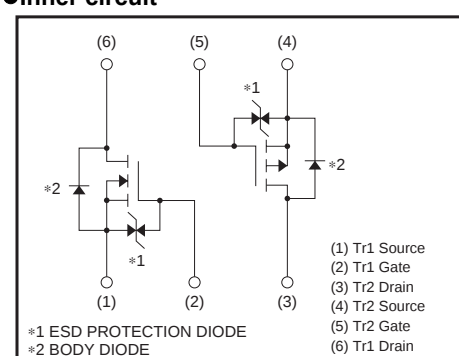
*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Each terminal mounted on a recommended land

●Dimensions (Unit : mm)



●Inner circuit



N-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} = ±8V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	20	–	–	V	I _D = 1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	1	μA	V _{DS} = 20V, V _{GS} =0V
Gate threshold voltage	V _{GS (th)}	0.3	–	1.0	V	V _{DS} = 10V, I _D = 1mA
Static drain-source on-state resistance	R _{DS (on)} *	–	0.7	1.0	Ω	I _D = 200mA, V _{GS} = 4.0V
		–	0.8	1.2	Ω	I _D = 200mA, V _{GS} = 2.5V
		–	1.0	1.4	Ω	I _D = 200mA, V _{GS} = 1.8V
		–	1.2	2.4	Ω	I _D = 40mA, V _{GS} = 1.5V
		–	1.6	4.8	Ω	I _D = 20mA, V _{GS} = 1.2V
Forward transfer admittance	Y _{fs} *	0.2	–	–	S	V _{DS} = 10V, I _D = 200mA
Input capacitance	C _{iss}	–	25	–	pF	V _{DS} = 10V
Output capacitance	C _{oss}	–	10	–	pF	V _{GS} = 0V
Reverse transfer capacitance	C _{rss}	–	10	–	pF	f=1MHz
Turn-on delay time	t _{d (on)} *	–	5	–	ns	V _{DD} ≐ 10V
Rise time	t _r *	–	10	–	ns	I _D = 150mA
Turn-off delay time	t _{d (off)} *	–	15	–	ns	V _{GS} = 4.0V
Fall time	t _f *	–	10	–	ns	R _L ≐ 67Ω R _G = 10Ω

* Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	1.2	V	I _S = 100mA, V _{GS} =0V

* Pulsed

P-ch

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I _{GSS}	–	–	±10	μA	V _{GS} = ±10V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR) DSS}	–20	–	–	V	I _D = –1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	–1	μA	V _{DS} = –20V, V _{GS} =0V
Gate threshold voltage	V _{GS (th)}	–0.3	–	–1.0	V	V _{DS} = –10V, I _D = –100μA
Static drain-source on-state resistance	R _{DS (on)} *	–	0.8	1.2	Ω	I _D = –200mA, V _{GS} = –4.5V
		–	1.0	1.5	Ω	I _D = –100mA, V _{GS} = –2.5V
		–	1.3	2.2	Ω	I _D = –100mA, V _{GS} = –1.8V
		–	1.6	3.5	Ω	I _D = –40mA, V _{GS} = –1.5V
		–	2.4	9.6	Ω	I _D = –10mA, V _{GS} = –1.2V
Forward transfer admittance	Y _{fs} *	0.2	–	–	S	V _{DS} = –10V, I _D = –200mA
Input capacitance	C _{iss}	–	115	–	pF	V _{DS} = –10V
Output capacitance	C _{oss}	–	10	–	pF	V _{GS} = 0V
Reverse transfer capacitance	C _{rss}	–	6	–	pF	f=1MHz
Turn-on delay time	t _{d (on)} *	–	6	–	ns	V _{DD} ≐ –10V
Rise time	t _r *	–	4	–	ns	I _D = –100mA
Turn-off delay time	t _{d (off)} *	–	17	–	ns	V _{GS} = –4.5V
Fall time	t _f *	–	17	–	ns	R _L ≐ 100Ω R _G = 10Ω

* Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V _{SD} *	–	–	–1.2	V	I _S = –200mA, V _{GS} =0V

* Pulsed

N-ch

●Electrical characteristic curve

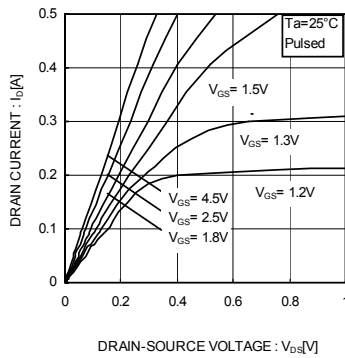


Fig.1 Typical Output Characteristics(I)

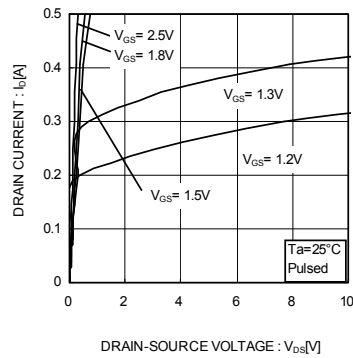


Fig.2 Typical Output Characteristics(II)

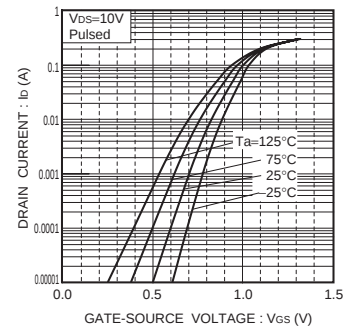


Fig.3 Typical transfer characteristics

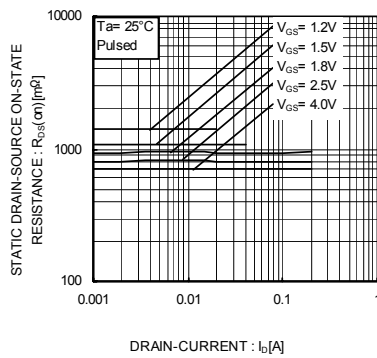


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

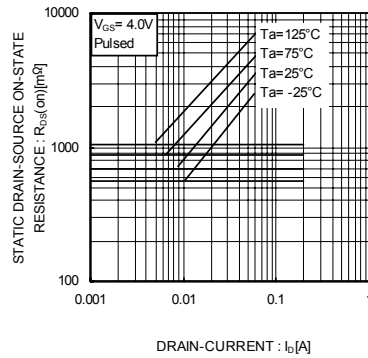


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

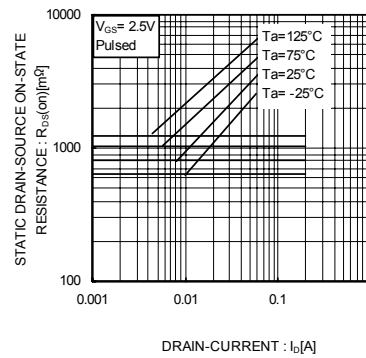


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(II)

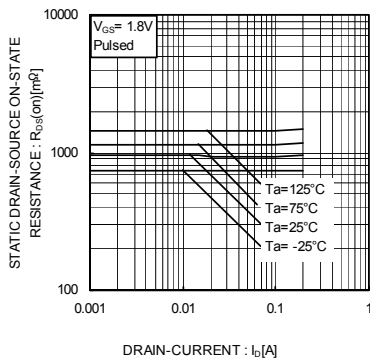


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(III)

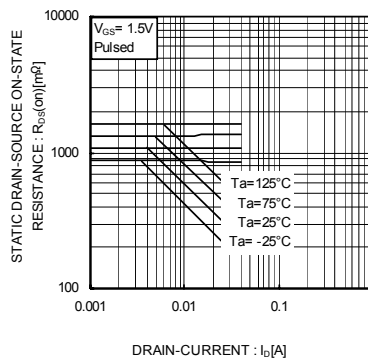


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

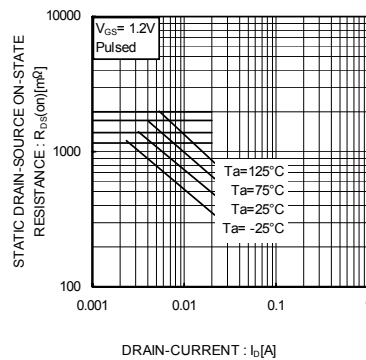


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(V)

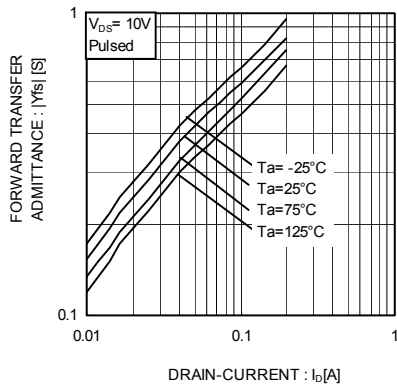


Fig. 10 Forward Transfer Admittance vs. Drain Current

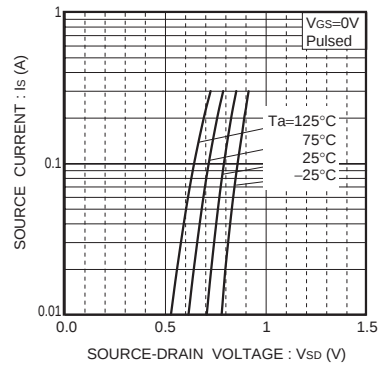


Fig. 11 Source current vs. source-drain voltage

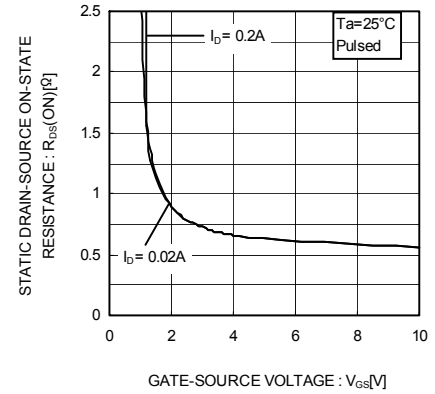


Fig. 12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

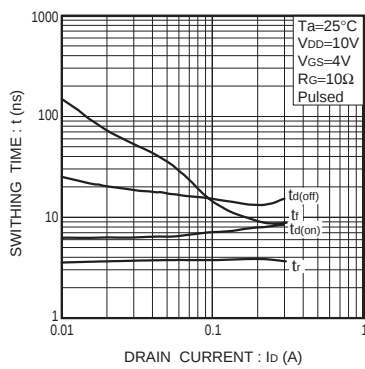


Fig. 13 Switching characteristics

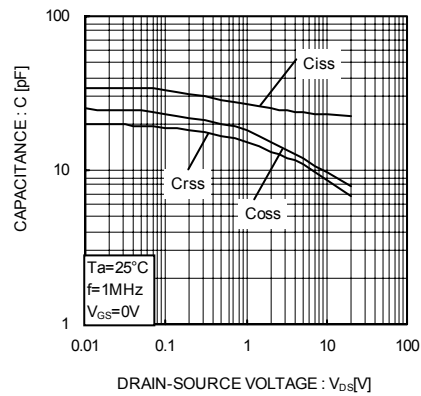


Fig. 14 Typical Capacitance vs. Drain-Source Voltage

P-ch

●Electrical characteristic curve

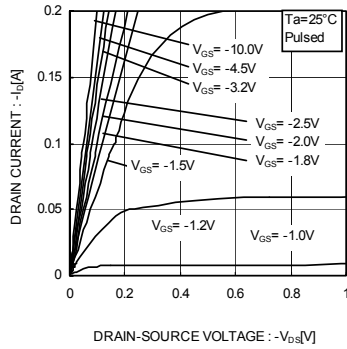


Fig.1 Typical output characteristics (I)

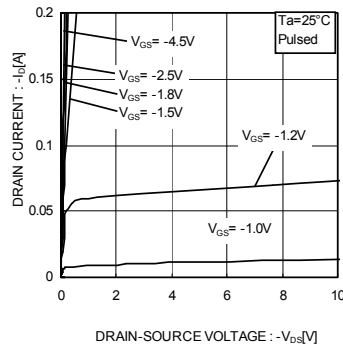


Fig.2 Typical output characteristics (II)

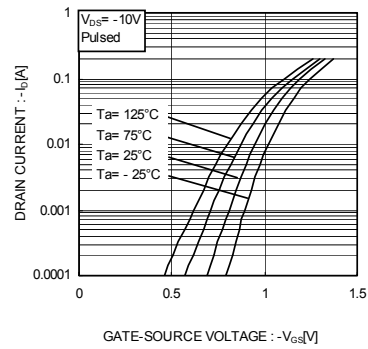


Fig.3 Typical Transfer Characteristics

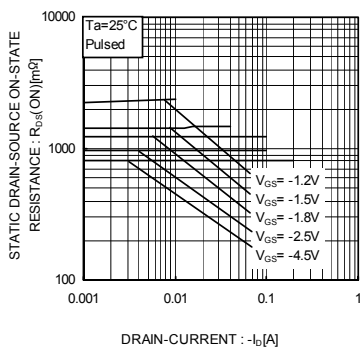


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

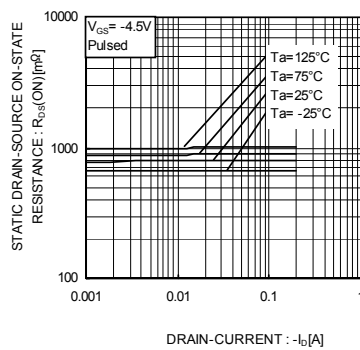


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

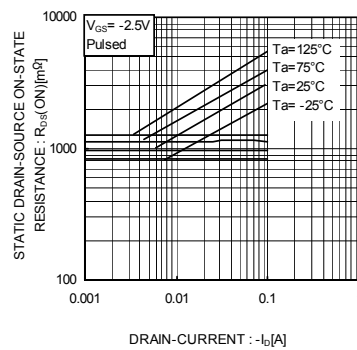


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

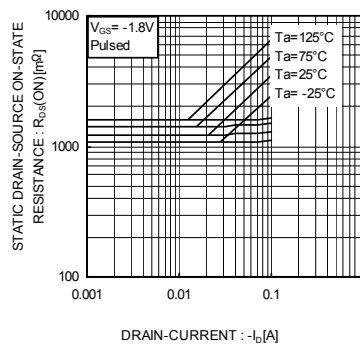


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

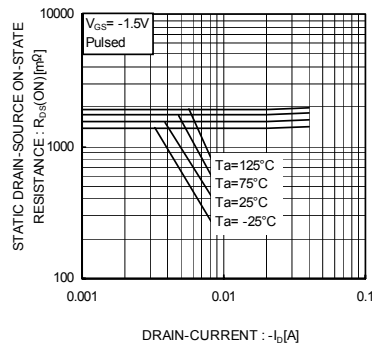


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (V)

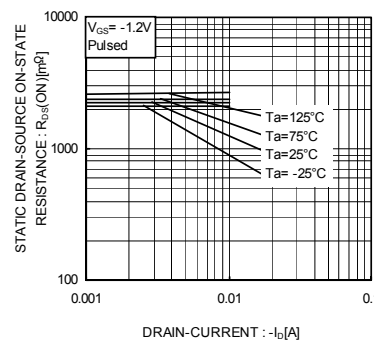


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (VI)

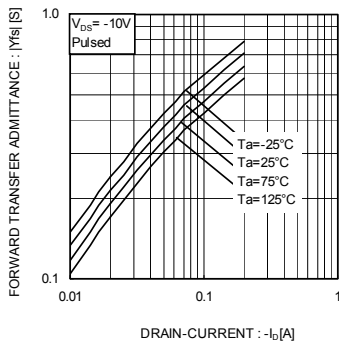


Fig.10 Forward Transfer Admittance vs. Drain Current

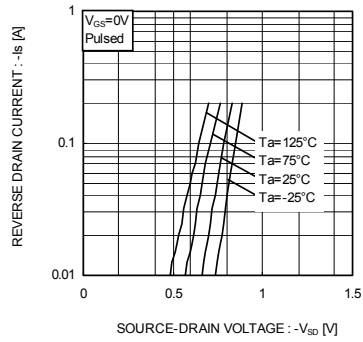


Fig.11 Reverse Drain Current vs. Source-Drain Voltage

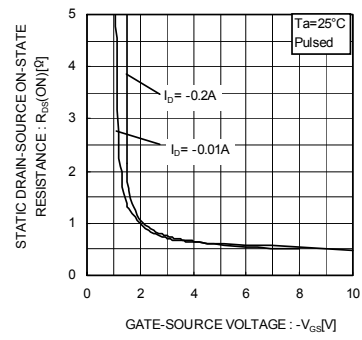


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

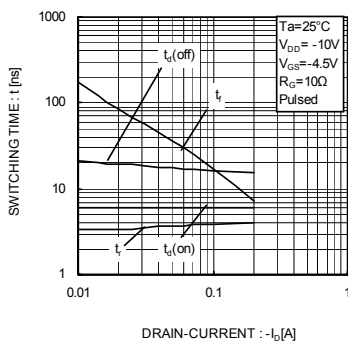


Fig.13 Switching Characteristics

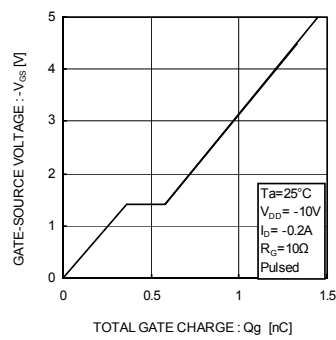


Fig.14 Dynamic Input Characteristics

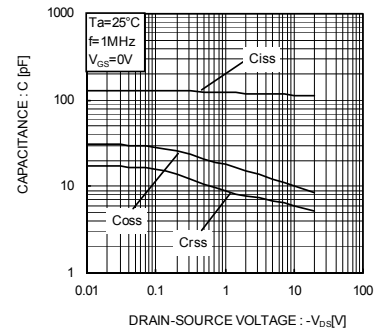


Fig.15 Typical Capacitance vs. Drain-Source Voltage

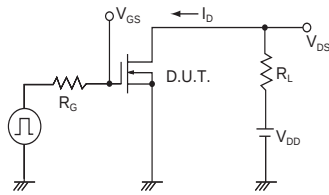
N-ch**●Measurement circuit**

Fig.1-1 Switching Time Measurement circuit

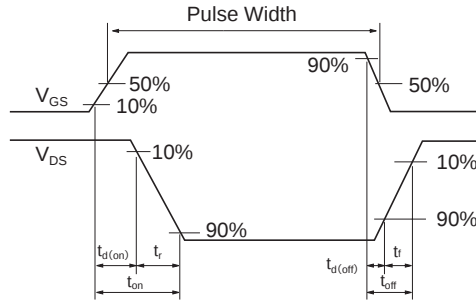


Fig.1-2 Switching Waveforms

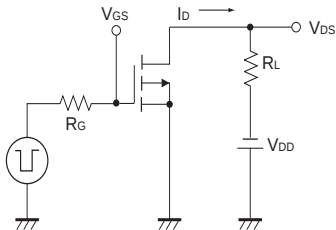
P-ch**●Measurement circuit**

Fig.2-1 Switching Time Measurement circuit

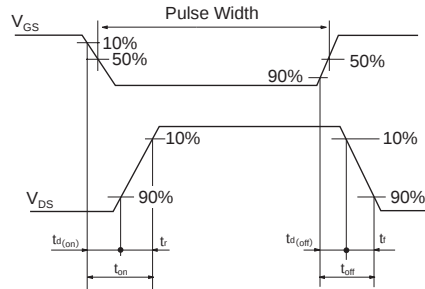


Fig.2-2 Switching Waveforms

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

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