

1.2V Drive Nch+Nch MOSFET

EM6K7

●Structure

Silicon N-channel
MOSFET

●Applications

Switching

●Features

- 1) The MOSFET elements are independent, eliminating mutual interference.
- 2) Mounting cost and area can be cut in half.
- 3) Low voltage drive (1.2V) makes this device ideal for portable equipment.

●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6K7		○

●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GS}	±8	V
Drain current	Continuous	I_D	±200	mA
	Pulsed	I_{DP}^{*1}	±400	mA
Total power dissipation		P_D^{*2}	150	mW / TOTAL
			120	mW / ELEMENT
Channel temperature		T_{ch}	150	°C
Range of storage temperature		T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle ≤ 1%

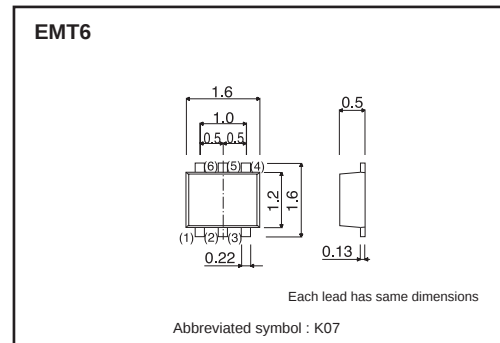
*2 Each terminal mounted on a recommended land.

●Thermal resistance

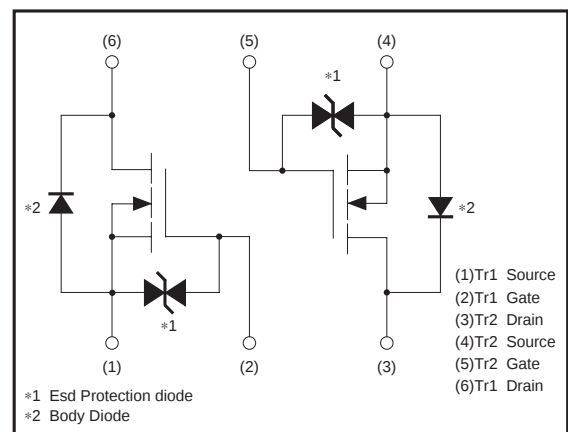
Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th(ch-a)}^{*}$	833	°C/W / TOTAL
		1042	°C/W / ELEMENT

* Each terminal mounted on a recommended land

●Dimensions (Unit : mm)



●Inner circuit



●Electrical characteristics (Ta=25°C)

<It is the same characteristics for the Tr1 and Tr2>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	—	—	± 10	μA	$V_{GS}=\pm 8V$, $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D=1mA$, $V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS}=20V$, $V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	0.3	—	1.0	V	$V_{DS}=10V$, $I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	—	0.8	1.2	Ω	$I_D=200mA$, $V_{GS}=2.5V$
		—	1.0	1.4	Ω	$I_D=200mA$, $V_{GS}=1.8V$
		—	1.2	2.4	Ω	$I_D=40mA$, $V_{GS}=1.5V$
		—	1.6	4.8	Ω	$I_D=20mA$, $V_{GS}=1.2V$
Forward transfer admittance	$ Y_{fs} $ *	200	—	—	mS	$V_{DS}=10V$, $I_D=200mA$
Input capacitance	C_{iss}	—	25	—	pF	$V_{DS}=10V$
Output capacitance	C_{oss}	—	10	—	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	—	10	—	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	—	5	—	ns	$V_{DD} \doteq 10V$, $I_D=150mA$
Rise time	t_r *	—	10	—	ns	$V_{GS}=4.0V$
Turn-off delay time	$t_{d(off)}$ *	—	15	—	ns	$R_L \doteq 67\Omega$
Fall time	t_f *	—	10	—	ns	$R_G=10\Omega$

* Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	—	—	1.2	V	$I_S=100mA$, $V_{GS}=0V$

* Pulsed

●Electrical characteristics curves

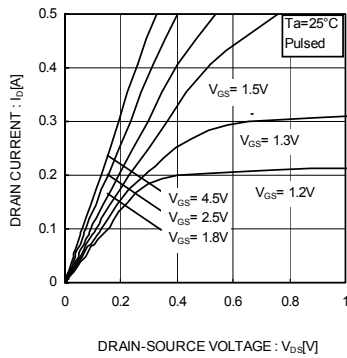


Fig.1 Typical Output Characteristics (I)

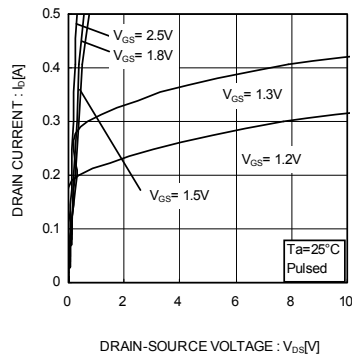


Fig.2 Typical Output Characteristics (II)

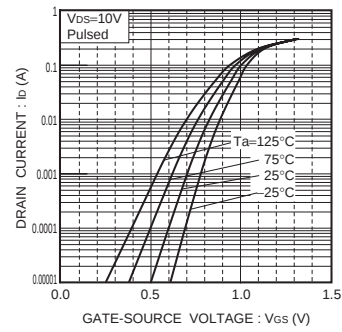


Fig.3 Typical transfer characteristics

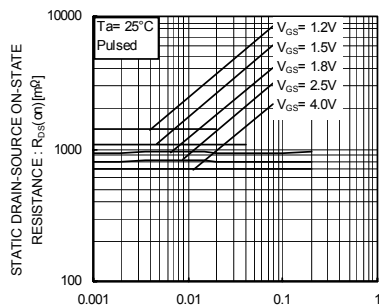


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

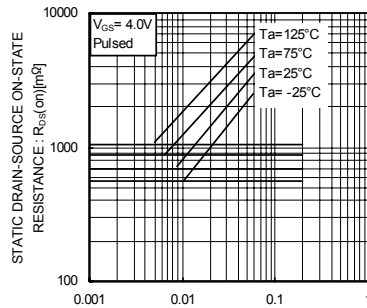


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

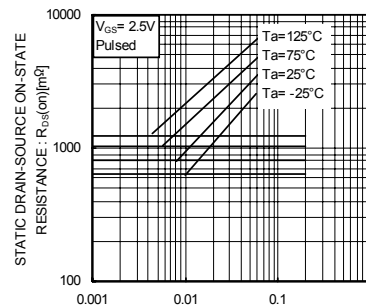


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(II)

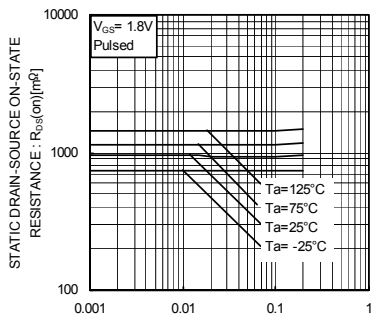


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(III)

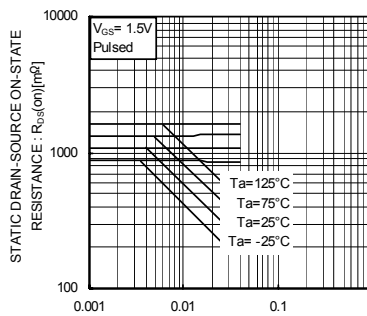


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

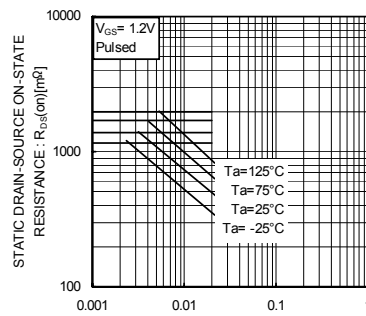


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(V)

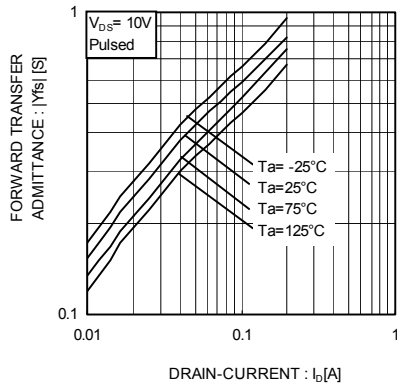


Fig.10 Forward Transfer Admittance vs. Drain Current

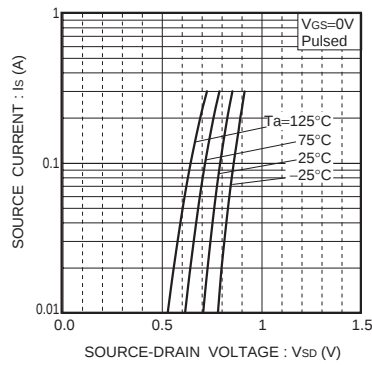


Fig.11 Source current vs. source-drain voltage

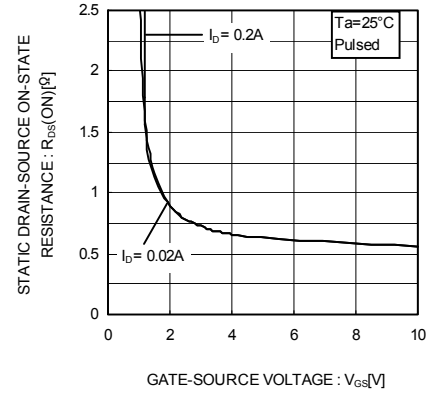


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

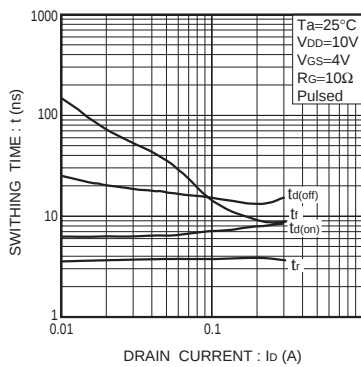


Fig.13 Switching characteristics

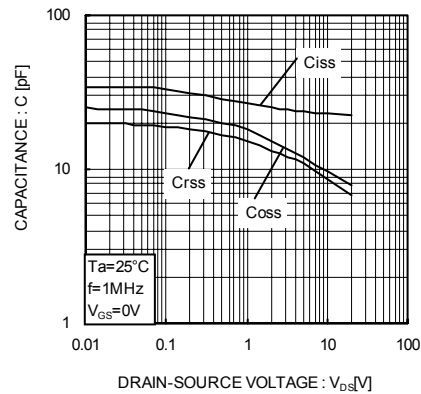


Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuit

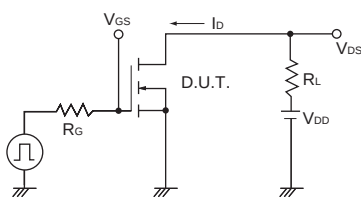


Fig.1-1 Switching time measurement circuit

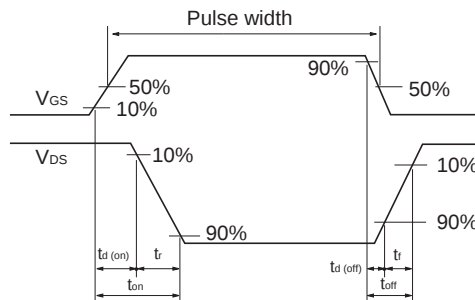


Fig.1-2 Switching waveforms

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit

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