Power Management IC Series for Automotive Body Control

Antenna Driver

BD6934FV

●Description

This 1ch half-bridje pre-driver for 125kH$_Z$ drive with a built-in oscillation circuit is equipped the driving current adjustment function.

●Features

1)Pre-driver for driving MOS-FET
2)4MHz ceramic resonator or external pulse are available
3)Driving current adjustment function (Dependence on power supply voltage)
4)Stand-by current 0μA（typ.）
5)Built-in the resistance between Gate to Source of FET
6)Built-in FET synchro on protect
7)Built-in thermal shutdown
8)Built-in under voltage lockout protection(UVLO)

●Applications

Usable in driving low frequency , the likes of TPMS and smart entry system.

●Absolute Maximum Ratings（Ta=25℃）

Parameter	Symbol	Rating	Unit
Supply voltage	Vcc1,Vcc2	12	V
Power dissipation	Pd	562 ＊	mW
Operating temperature range	T$_{opr}$	-40～85	℃
Storage temperature range	T$_{stg}$	-55～150	℃
Junction temperature	T$_{jmax}$	150	℃

＊Reduced by 4.496mW/℃,when mounted on a glass epoxy board (70mm×70mm×1.6mm)

●Operating range (Ta=25℃)

Parameter	Symbol	Operating range	Unit
Supply voltage	Vcc1,Vcc2	3.5～8	V
RP,RN voltage	Vrp,Vrn	VCC2	V
XOUT,RT,CT voltage	Vxout,Vrt,Vct	VCC1	V
Input voltage	V$_{IN}$	-0.3～VCC1	V

＊This product described in this specification isn't judged whether it applies to COCOM regulations.
　It should not be exported without authorization from the appropriate government.
＊This product is not designed for protection against radioactive rays.
＊Status of this document
　The Japanese version of this document is the formal specification.
　A customer may use this translation version only for a reference to help reading the formal version.
　If there are any differences in translation version of this document, formal version takes priority.

●Electrical characteristics （Unless otherwise specified, VCC1=VCC2=3.5～8V,Ta=-40～85℃）

Parameter	Symbol	Limit			Unit	Conditions	Measurement circuit
		Min.	Typ.	Max.			
［Circuit current］							
VCC drive current	Icc1	-	3.5	7	mA	IN=High	Fig.31
VCC stand-by current	Icc2	-	-	10	μA	IN=Low	Fig.32
[Output]							
Upper side output voltage H	V_{OHH}	VCC-0.4	VCC-0.2	-	V	Io=-5mA	Fig.33
Upper side output voltage L	V_{OHL}	-	0.2	0.4	V	Io=5mA	Fig.33
Lower side output voltage H	V_{OLH}	VCC-0.4	VCC-0.2	-	V	Io=-5mA	Fig.33
Lower side output voltage L	V_{OLL}	-	0.2	0.4	V	Io=5mA	Fig.33
Output leak current H	I_{LH}	-	-	10	μA	Vo=0V	Fig.32
Output leak current L	I_{LL}	-	-	10	μA	Vo=12V	Fig.32
ON Duty 3.5V	$D_{ON}3.5$	6.84	9.17	11.5	%	VCC1=VCC2=3.5V	Fig.34
ON Duty 4V	$D_{ON}4$	13	15	17	%	VCC1=VCC2=4V	Fig.34
ON Duty 7V	$D_{ON}7$	44	49	54	%	VCC1=VCC2=7V	Fig.34
Oscillating start time *	T_{OSC}	-	-	8	μsec	*	Fig.34
［Input （IN,SEL） ］							
Input voltage H	V_{IH}	VCC*0.8	-	-	V		Fig.33
Input voltage L	V_{IL}	-	-	1.3	V		Fig.34
Input current H	I_{IH}	10	-	150	μA	VIN=VCC	Fig.31
Input current L	I_{IL}	-	-	10	μA	VIN=0V	Fig.32
［Under voltage lockout protection］							
UVLO ON voltage	V_{UVON}	2.7	3	3.3	V		Fig.31
UVLO OFF voltage	V_{UVOFF}	2.9	3.2	3.5	V		Fig.31
［Trianglar wave generation］							
RT voltage	V_{RT}	0.63	0.7	0.77	V		Fig.35
CT charge current	I_{CTC}	346	432	518	μA	VCT＝1.1V	Fig.35
CT discharge current	I_{CTD}	300	430	560	μA	VCT＝1.1V	Fig.35

* Oscillating start time ： Time till operating output, after UVLO turn off during oscillating ceramic resonator.

◎This product is not designed for protection against radioactive rays.
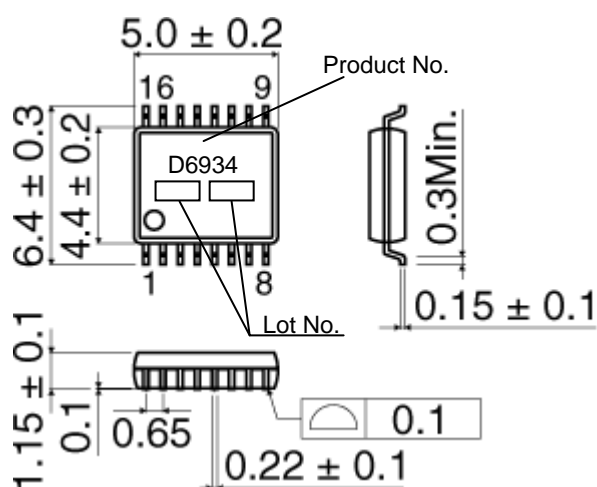
●Dimension

Fig.1　SSOP-B16 （UNIT:mm）
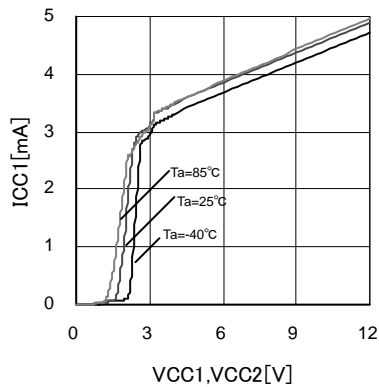
●Reference Data

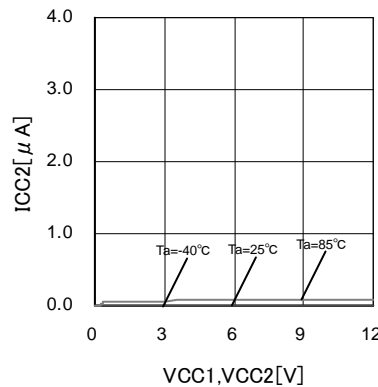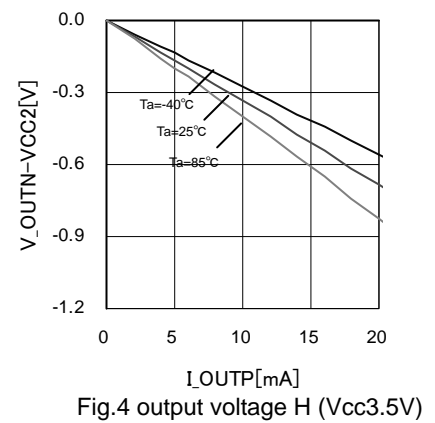Fig.2 VCC drive current

Fig.3 VCC stand-by current

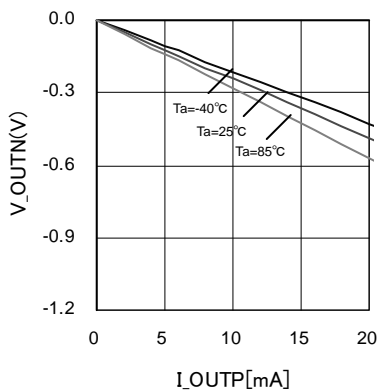Fig.4 output voltage H (Vcc3.5V)

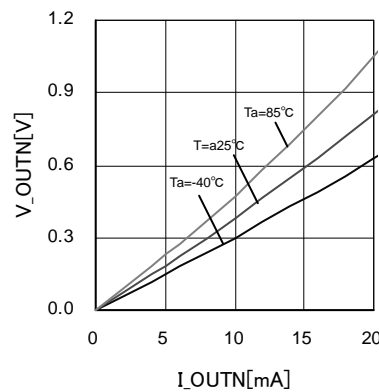Fig.5 output voltage H (Vcc8V)
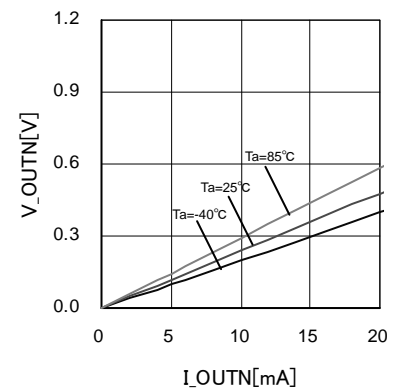

Fig.6 output voltage L (Vcc3.5V)
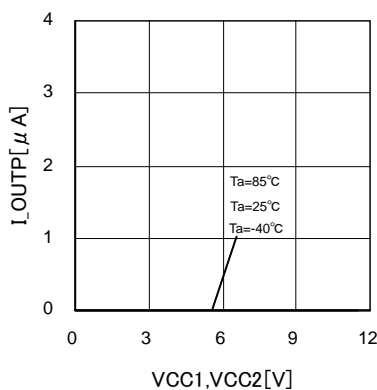

Fig.7 output voltage L (Vcc8V)
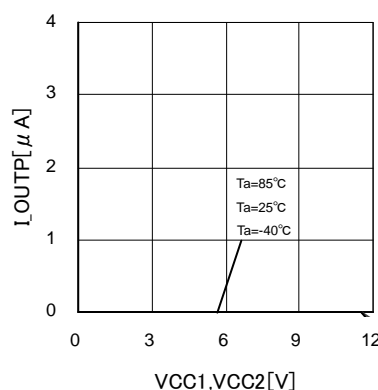

Fig.8 Output leak current H
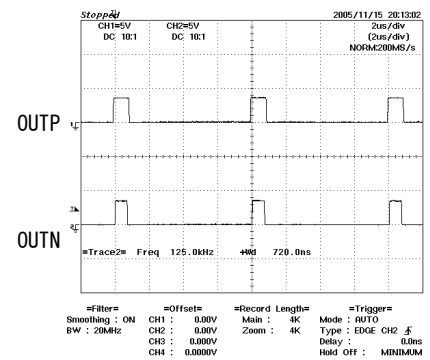

Fig.9 Output leak current L
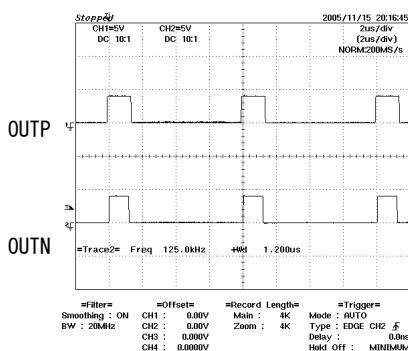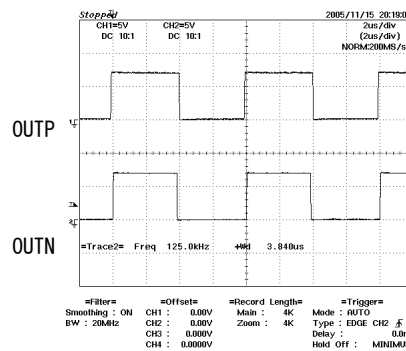

Fig.10 ON Duty3.5V

Fig.11 ON Duty4V

Fig.12 ON Duty7V

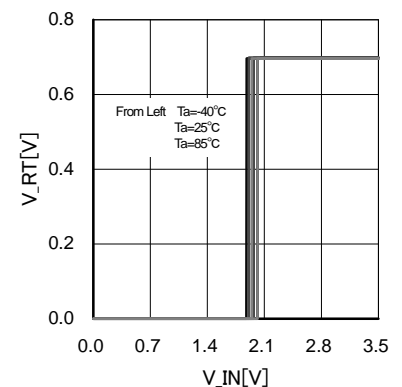
Fig.13 Input voltage H / L (Vcc3.5V)
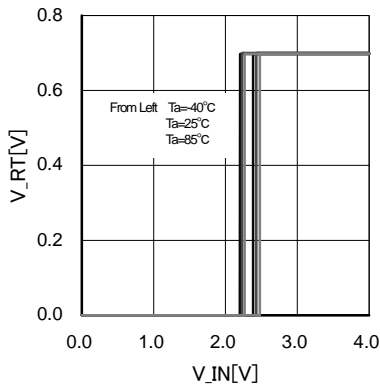
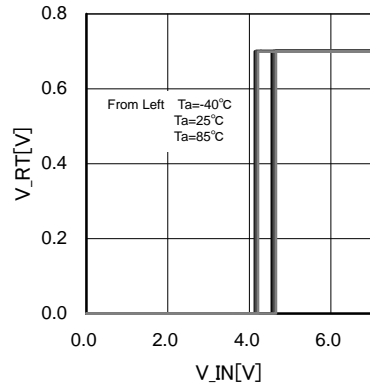Fig.14 Input voltage H / L (Vcc4V)

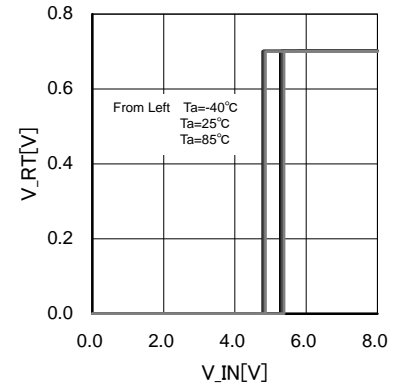Fig.15 Input voltage H / L (Vcc7V)

Fig.16 Input voltage H / L (Vcc8V)
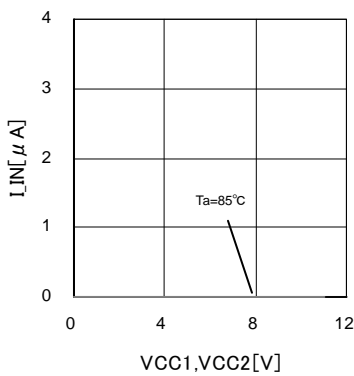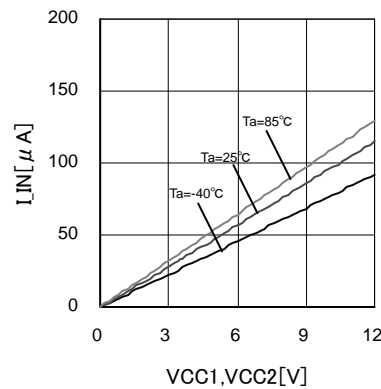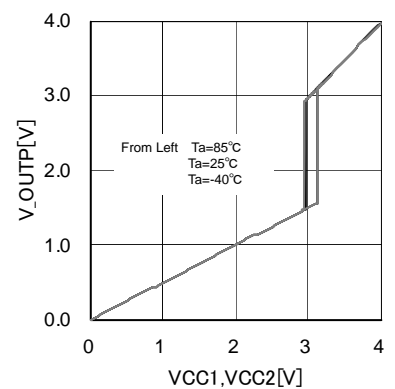

Fig.17   Input current H
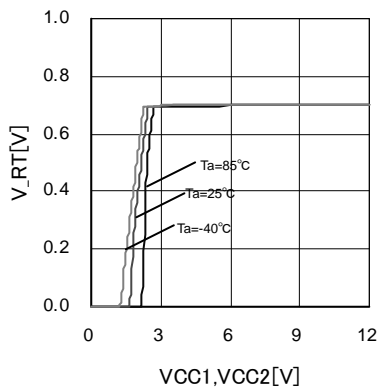

Fig.18 Input current L

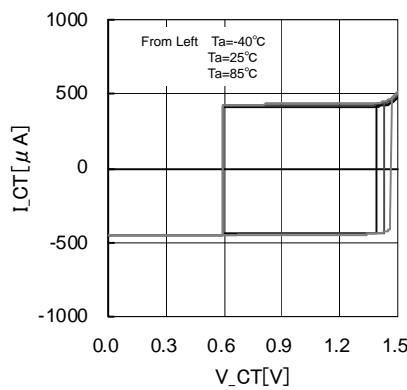

Fig.19   UVLO ON/OFF voltage

Fig.20   RT voltage

Fig.21 CT charge-discharge current

●Block diagram
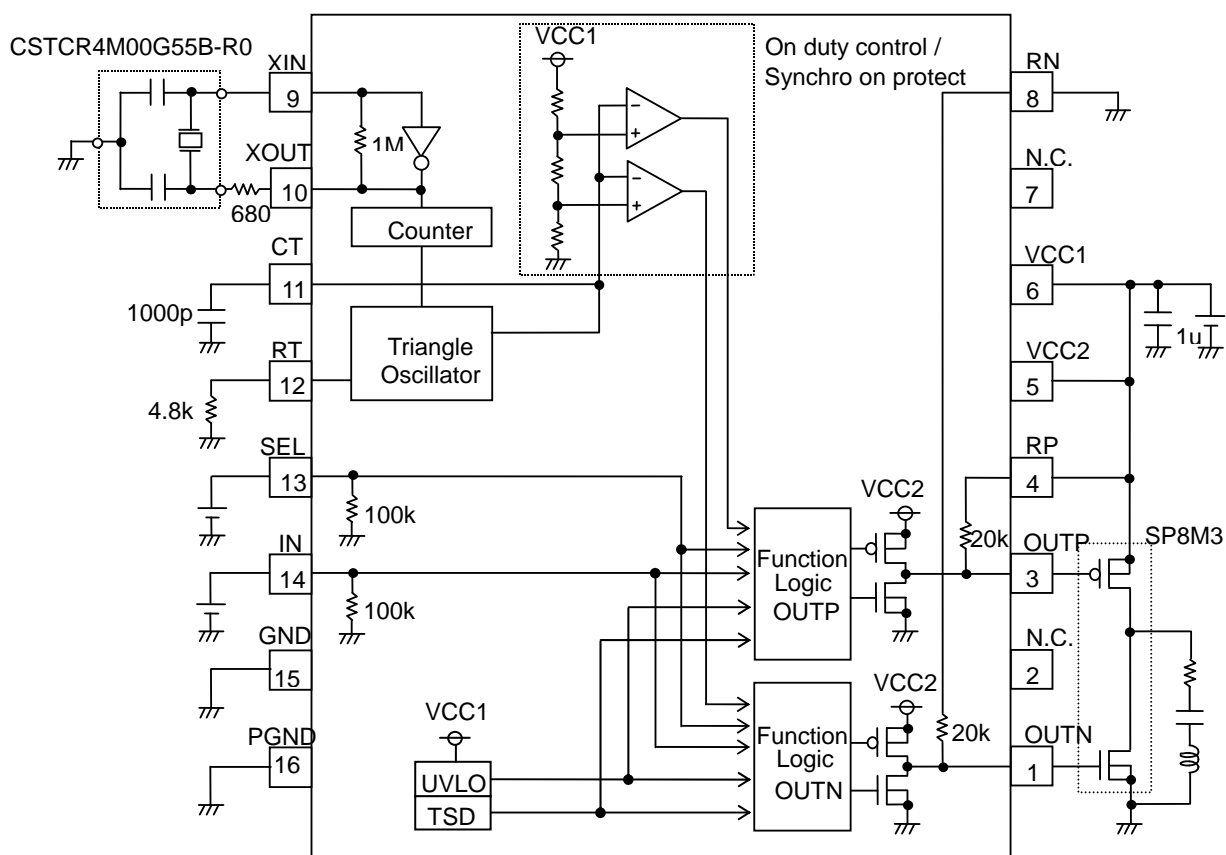
Fig.22   Resonator mode
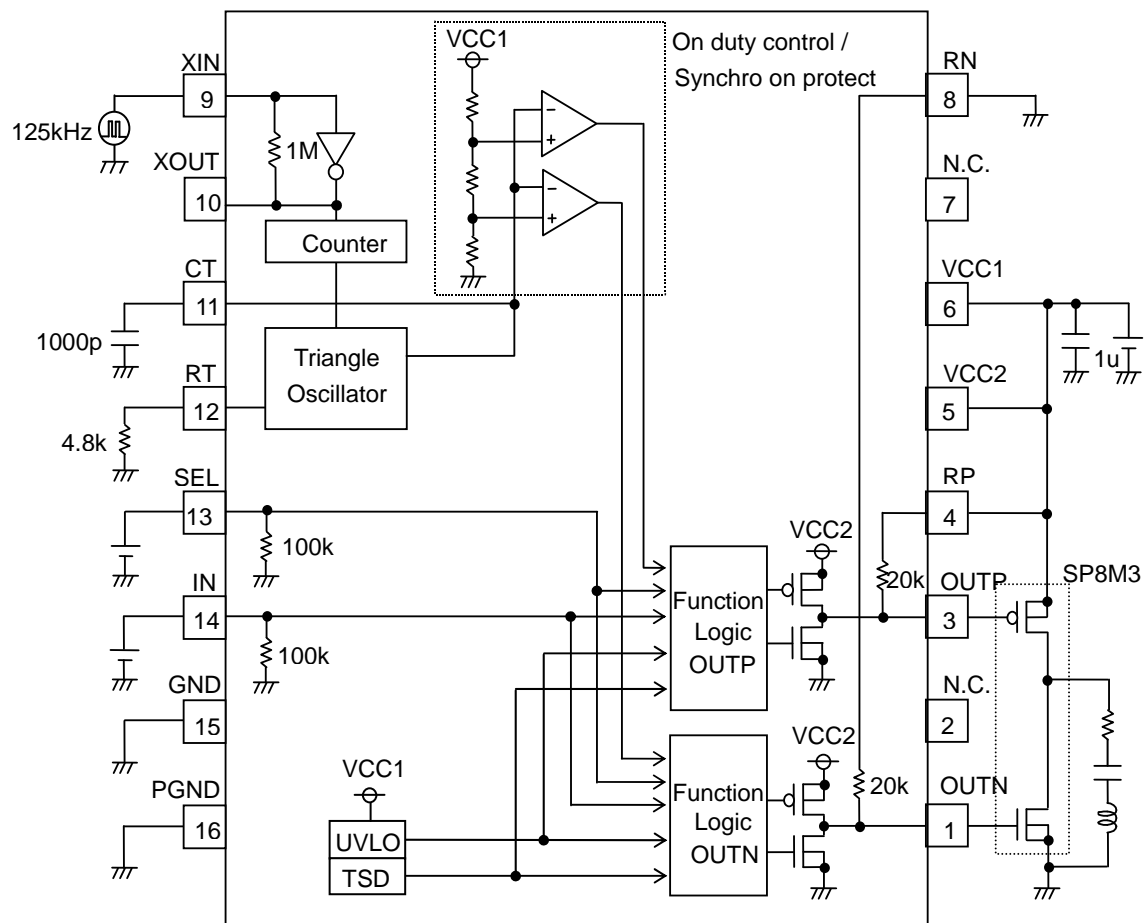
Fig.23   External pulse mode

∗ Product No.and constants of external devices are recommended condition.

●Pin name

PIN NO.	Pin name	Function
1	OUTN	Nch FET GATE connection
2	N.C.	N.C.
3	OUTP	Pch FET GATE connection
4	RP	For pull-up resistance of Pch FET Gate
5	VCC2	Power VCC terminal
6	VCC1	Signal VCC terminal
7	N.C.	N.C.
8	RN	For pull – down resistance of Nch FET Gate
9	XIN	Resonator connection
10	XOUT	Resonator connection
11	CT	Capacitor connection for triangular wave generation
12	RT	Capacitor connection for triangular wave generation
13	SEL	Input terminal for mode selection(Resonator mode:L,External pulse mode:H)
14	IN	Input terminal (Stand-by:L, Enable:H)
15	GND	Signal GND terminal
16	PGND	Power GND terminal

●I/O Circuit Diagram

Fig.24   SEL(13pin)   IN(14pin)

Fig.25   XIN(9pin)   XOUT(10pin)
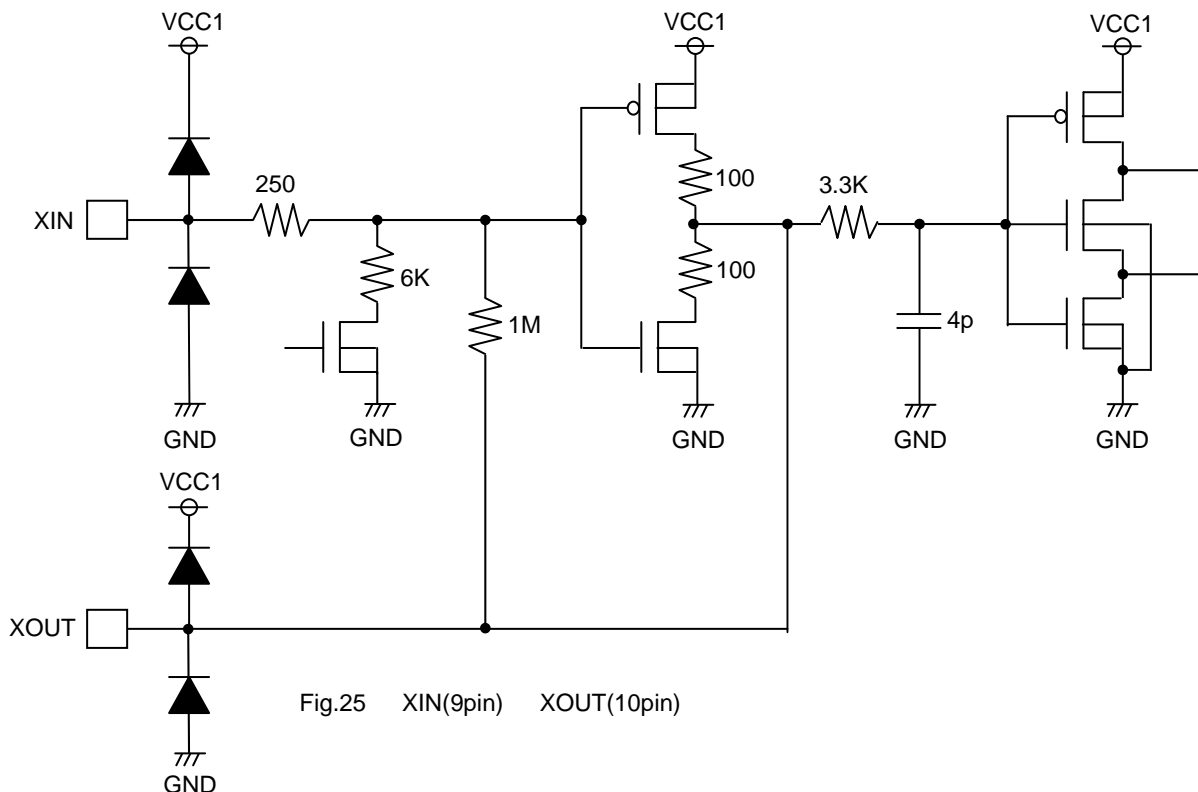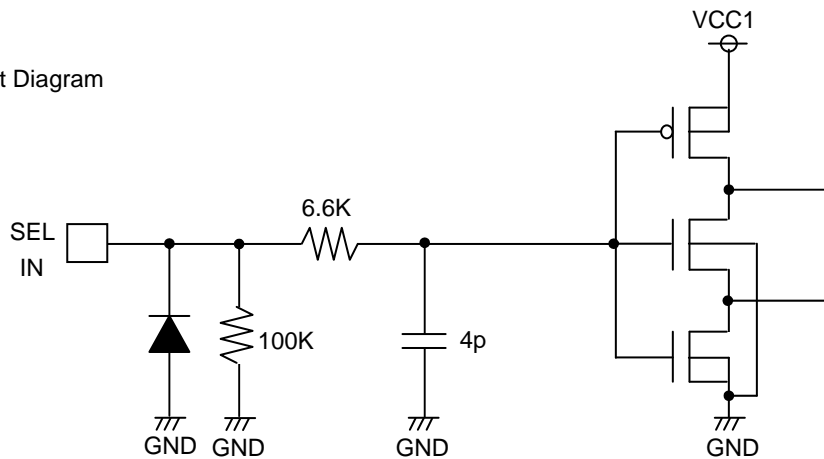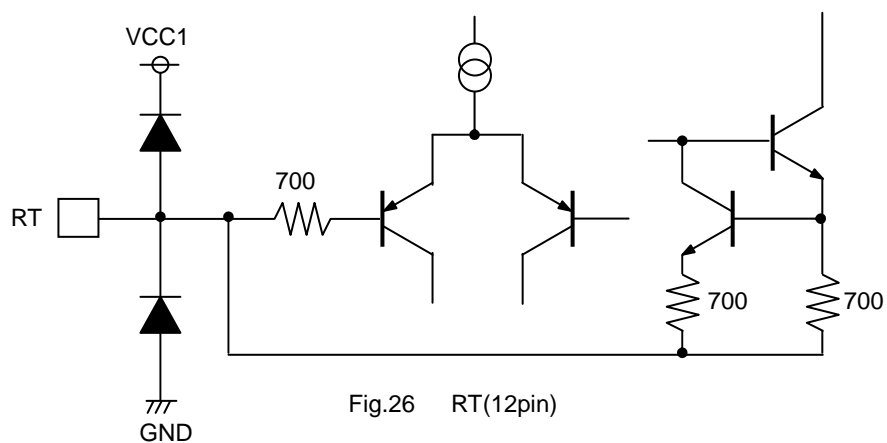
Fig.26   RT(12pin)
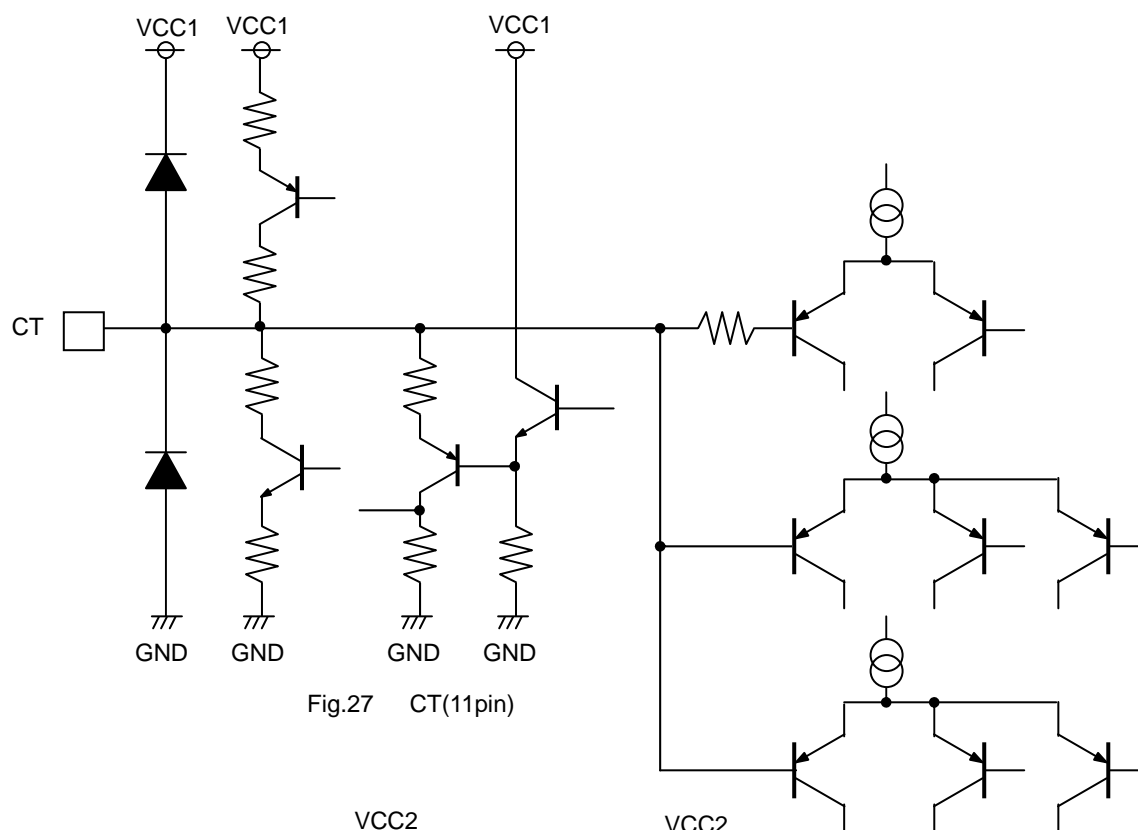
Fig.27   CT(11pin)
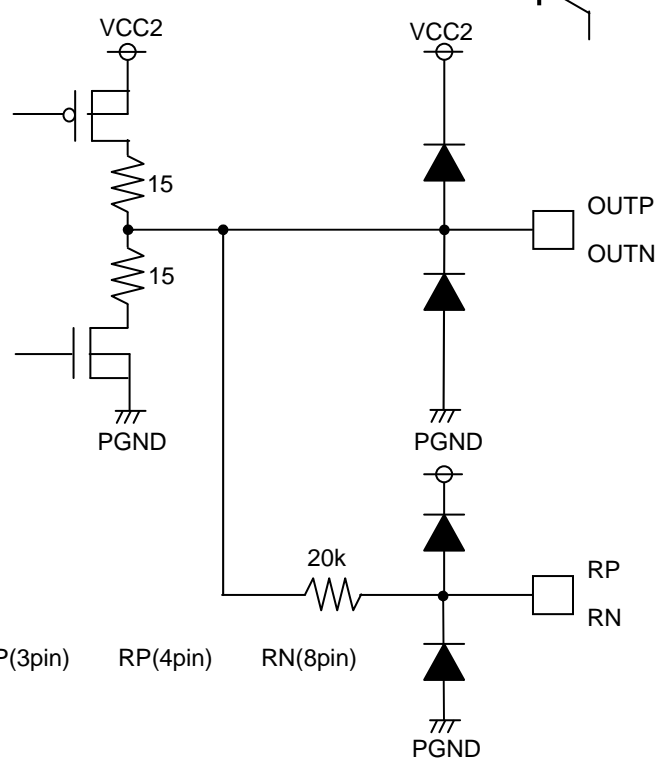
Fig.28   OUTN(1pin) OUTP(3pin)   RP(4pin)   RN(8pin)

●Truth table

	Input			Output	
Pin Name	XIN	IN	SEL	OUTP	OUTP
Pin No.	9	14	13	3	1
Resonator	4MHz	L	L	Hiz	Hiz
4MHz	4MHz	H	L	Enable	Enable
External signal	125KHz	L	L	Hiz	Hiz
125KHz	125KHz	H	H	Enable	Enable

●Timing chart

XIN（4MHz）

Internal CLK H
（125kHz） L

period 8usec

Variation as to supply voltage

CT

OUTP H / L

OUTN H / L

ON time   Dead time   Dead time

Fig.29　Timing chart(driving)

VCC
(=IN)

8V
7V
3.2V
3.0V
0V

OUTP   Hi   Enable   Hiz

OUTN   Hi   Enable   Hiz

Fig.30　VCC-OUTP・OUTN　Operating range

●Measurement circuit

Fig.31 $I_{CC1}, I_{IH}, V_{OVDN}, V_{UVOFF}$

Fig.32 $I_{CC2}, I_{IH}, I_{LL}, I_{IL}$
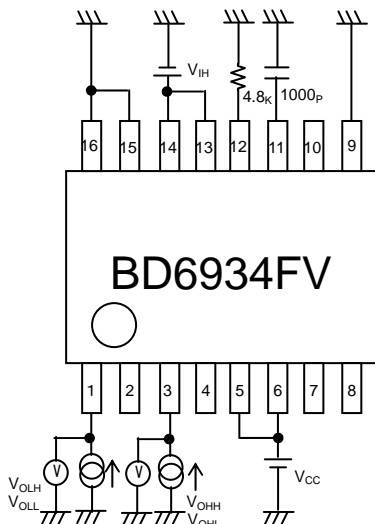
Fig.33 $V_{OHH}, V_{OHL}, V_{OLH}, V_{OLL}, V_{IH}$
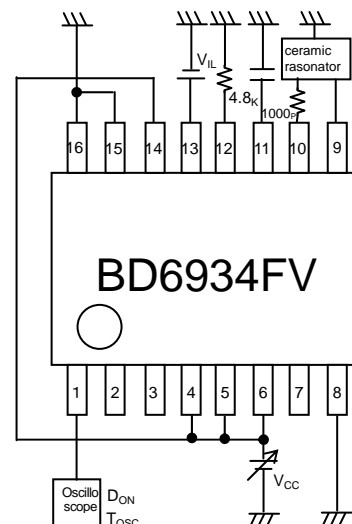
Fig.34 $D_{ON}3.5, D_{ON}4, D_{ON}7, T_{OSC}, V_{IL}$
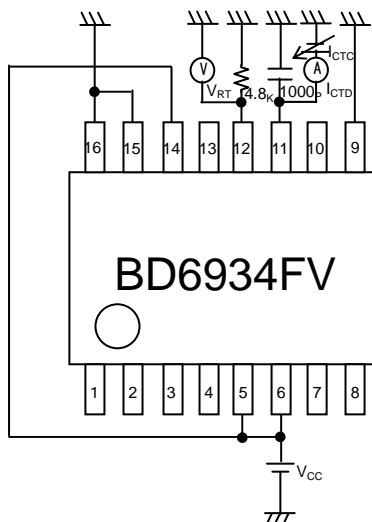
Fig.35 V_{RT}, I_{CTC}, I_{CTD}

2009.09 - Rev.B

●Operating explanation

Driving current adjustment function.

This IC control the duty of output pulse in response to supply voltage(Vcc).

This function is allowed to control driving current and adjust the arrival range of radio frequency. The relationship between supply voltage(Vcc) and output(OUTN) is as shown in the following figure.

This data is typical , refer to the electrical characteristics in regard to variation.

Fig.36 Supply voltage (Vcc) - Output (OUTN) Duty

External FET

Connect   PchMOS to OUTP and Nch MOS to OUTN

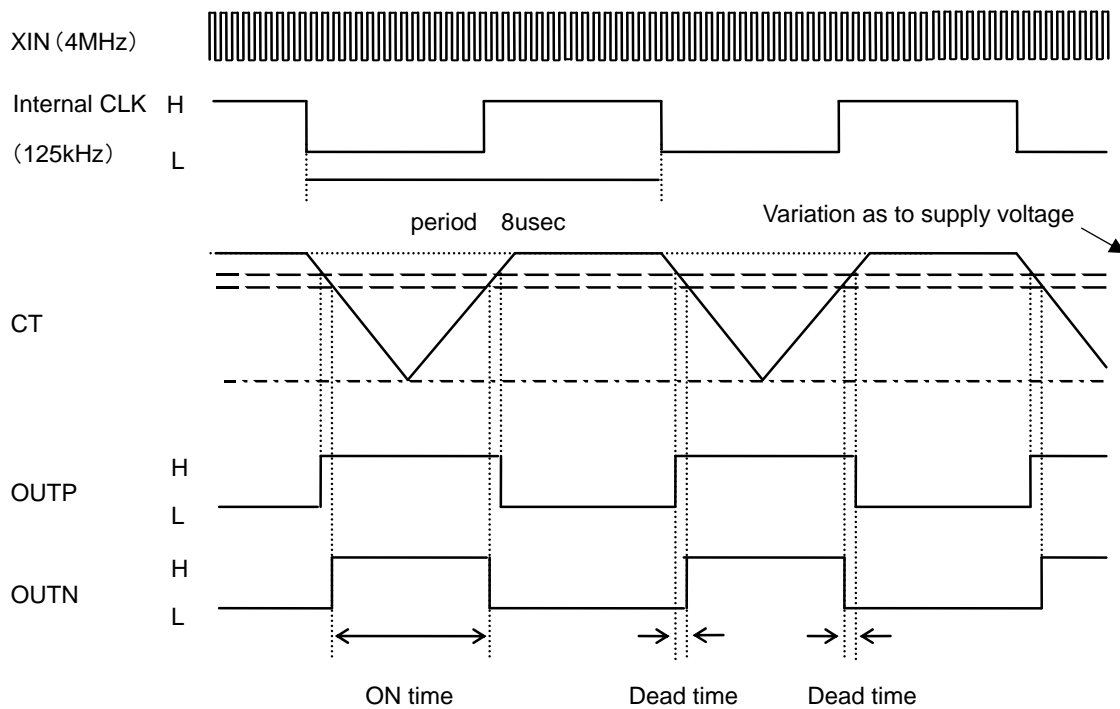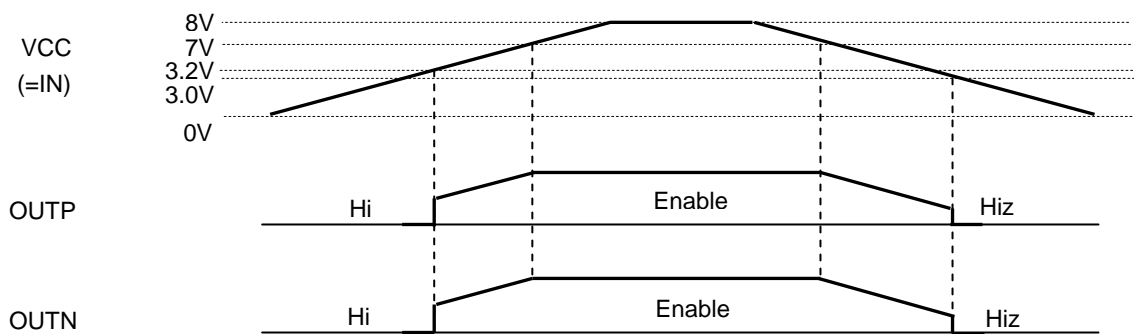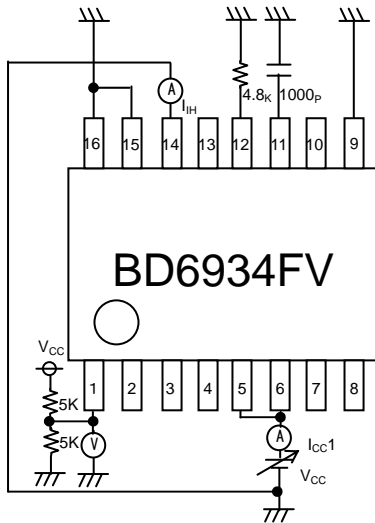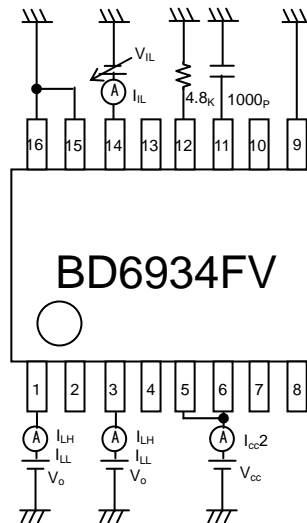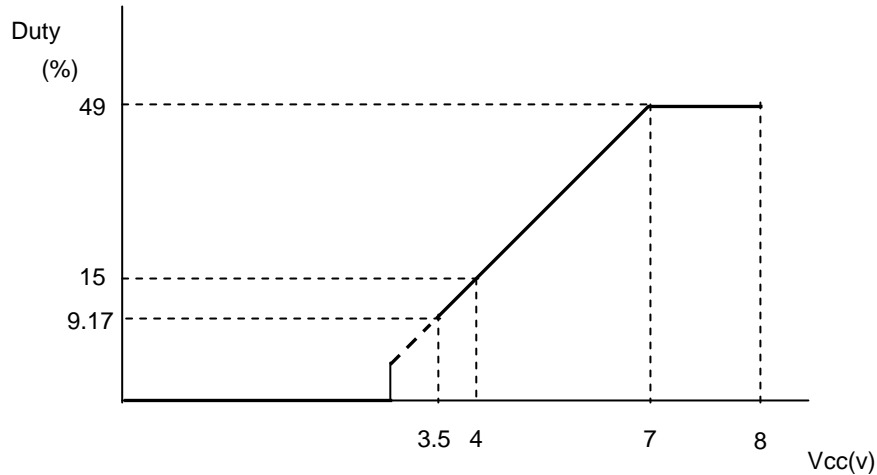Vds＞VCC, Vgs＞VCC, Allowable current ＞ Output current

There is a possibility that upper and lower FET turn on at the same time. It is recommended to use 1000pF or smaller at input capacitor of external FET. However , these characteristics change in the layout pattern and parts variation and so on. Make evaluations with using board in mass production.

Oscillation precision and condition

The oscillation precision depends on the condition of ceramic resonator. This IC is evaluated with the ceramic resonator (Product No.CSTCR4M00G55B-R0) of MURATA manufacturing. In the range of   Vcc 2.2~2.7V, this IC stops its oscillation without disenabling the ceramic resonator.

● OPERATING NOTES

 1)   Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a specialmode where the absolute maximum ratings may be exceeded is anticipated.

2)   GND potential

Ensure a minimum GND pin potential in all operating conditions.

3)   Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4)   Pin short and mistake mounting

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC. Ensure a minimum GND pin potential in all operating conditions.

5)   Actions in strong magnetic field

Keep in mind that the IC may malfunction in strong magnetic fields.

6) Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

7) This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements. For example, when the resistors and transistors are connected to the pins as shown in the following figure,

○The P/N junction functions as a parasitic diode when GND > Pin A for the resistor or GND > Pin B for the transistor(NPN).

○Similarly, when GND > Pin B for the transistor (NPN), the parasitic diode described above combines with the N layer of other adjacent elements to operate as a parasitic NPN transistor.

The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements, such as by the application of voltages lower than the GND (P substrate) voltage to input pins. Keep in mind that the IC may malfunction in strong magnetic fields.
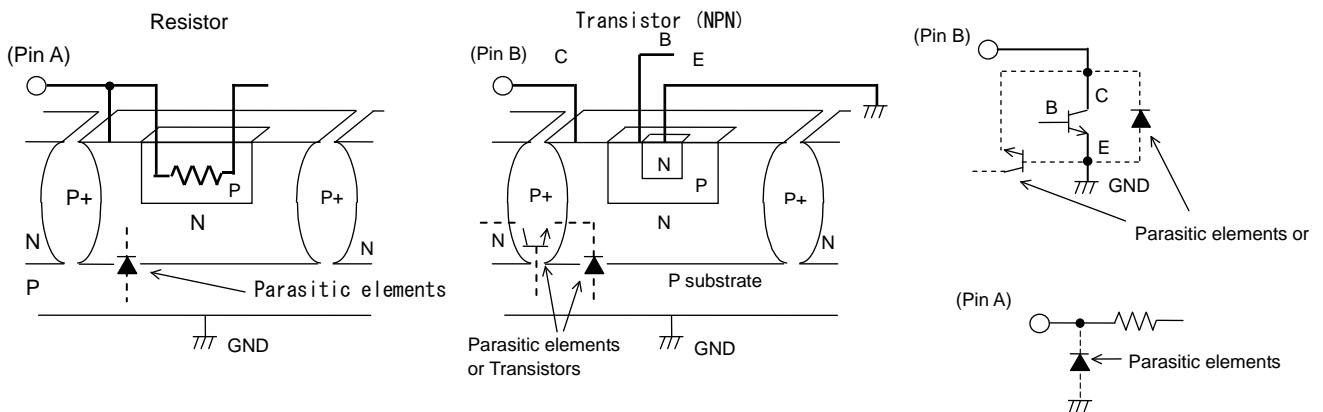
8) Ground patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external parts, either.

9) Thermal shutdown circuit (TSD)

This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the junction temperature (Tj) will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature (Tj) drops. Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

10) External parts

Driving current adjustment function in use low accuracy parts (Especially, RT terminal connection resistance, CT terminal connection capacitor and resonator) may malfunction.

The external parts use highly accuracy, and be careful additional impedance and capacitor for wiring pattern.

11)RP, RN terminal

The resistance is built in between OUTP and RP, and OUTN and RN to turn off external MOS - FET in stand - by.

Please wire with RP=VCC2 and RN =PGND.

Improper wiring may result in damage for the penetration current.

● **Ordering part number**

B	D		6	9	3	4		F	V	-	E	2

Part No.   Part No.   Package   Packaging and forming specification

FV: SSOP-B16   E2: Embossed tape and reel

SSOP-B16

5.0±0.2

6.4±0.3

4.4±0.2

0.3Min.

0.15±0.1

1.15±0.1

0.10

0.65

0.22±0.1

(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel   1pin   Direction of feed

＊Order quantity needs to be multiple of the minimum quantity.
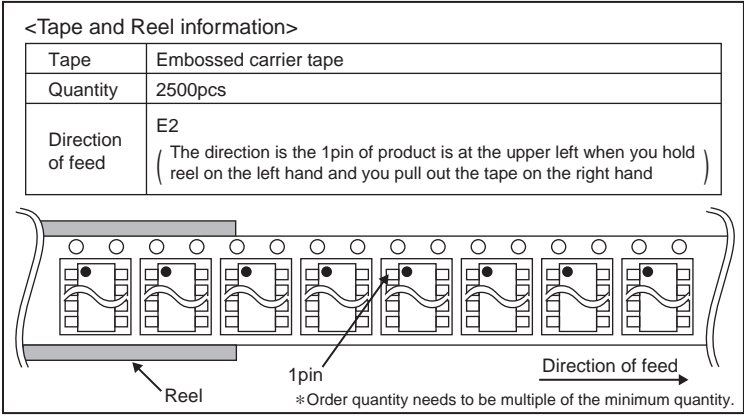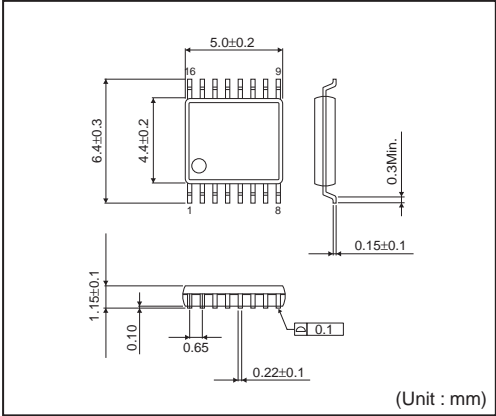
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