High Performance Regulators for PCs

Nch FET Ultra LDO for Desktop PCs

BD35281HFN

No.11030EAT38

●Description

The BD35281HFN ultra low-dropout linear regulator operates from a very low input supply, and offers ideal performance in low input voltage to low output voltage applications. It incorporates a built-in N-MOSFET power transistor to minimize the input-to-output voltage differential to the ON resistance ($R_{ON\ max}$=150mΩ) level. By lowering the dropout voltage in this way, the regulator realizes high current output (Iomax=1.5A) with reduced conversion loss, and thereby obviates the switching regulator and its power transistor, choke coil, and rectifier diode. Thus, the BD35281HFN designed to enable significant package profile downsizing and cost reduction. In BD35281HFN, The NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to whatever power supply sequence is required.

●Features

1) Internal high-precision reference voltage circuit (0.65V±1%)
2) Internal high-precision output voltage circuit
3) Built-in V_{CC} undervoltage lockout circuit (V_{CC}=3.80V)
4) NRCS (soft start) function reduces the magnitude of in-rush current
5) Internal Nch MOSFET driver offers low ON resistance (100mΩ typ)
6) Built-in short circuit protection (SCP)
7) Built-in current limit circuit (1.5A min)
8) Built-in thermal shutdown (TSD) circuit
9) Small package HSON8 : 2.9mm×3.0mm×0.6mm
10) Tracking function

●Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Input Voltage 1	V_{CC}	+6.0 *1	V
Input Voltage 2	V_{IN}	+6.0 *1	V
Maximum Output Current	I_O	2*1	A
Enable Input Voltage	V_{EN}	-0.3～+6.0	V
Power Dissipation 1	Pd1	0.63 *2	W
Power Dissipation 2	Pd2	1.35 *3	W
Power Dissipation 3	Pd3	1.75*4	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+125	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Reduced by 5.04mW/℃ for each increase in Ta≧25℃
(when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer, copper foil area : less than 0.2%)
*3 Reduced by 10.8mW/℃ for each increase in Ta≧25℃
(when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer, copper foil area : less than 7.0%)
*4 Reduced by 14.0mW/℃ for each increase in Ta≧25℃
(when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer, copper foil area : less than 65.0%)

●**Operating Voltage** (Ta=25℃)

Parameter	Symbol	Ratings		Unit
		Min.	Max.	
Input Voltage 1	V_{CC}	4.3	5.5	V
Input Voltage 2	V_{IN}	1.5	V_{CC}-1 *5	V
Output Voltage Setting Range	I_O	1.2 (fixed)		V
Enable Input Voltage	V_{EN}	-0.3	5.5	V
NRCS Capacity	CNRCS	0.001	1	μF

*5 V_{CC} and V_{IN} do not have to be implemented in the order listed.
★This product is not designed for use in radioactive environments.

●**Electrical Characteristics** (Unless otherwise specified, Ta=25℃, V_{CC}=5V, V_{EN}=3V, V_{IN}=1.7V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	I_{CC}	-	0.7	1.2	mA	
V_{CC} Shutdown Mode Current	I_{ST}	-	0	10	μA	V_{EN}=0V
Output Voltage	I_O	1.5	-	-	A	
Feedback Voltage 1	V_{OS}1	1.188	1.200	1.212	V	
Feedback Voltage 2	V_{OS}2	1.176	1.200	1.224	V	Tj=-10 to 100℃
Line Regulation 1	Reg.l1	-	0.1	0.5	%/V	V_{CC}=4.3V to 5.5V
Line Regulation 2	Reg.l2	-	0.1	0.5	%/V	V_{IN}=1.5V to 3.3V
Load Regulation	Reg.L	-	0.5	10	mV	I_O=0 to 1.5A
Output ON Resistance	R_{ON}	-	100	150	mΩ	I_O=1.5A,V_{IN}=1.2V, Tj=-10 to 100℃
Standby Discharge Current	I_{DEN}	1	-	-	mA	V_{EN}=0V, V_O=1V
[ENABLE]						
Enable Pin Input Voltage High	EN_{HIGH}	2	-	-	V	
Enable Pin Input Voltage Low	EN_{LOW}	0	-	0.8	V	
Enable Input Bias Current	I_{EN}	-	7	10	μA	V_{EN}=3V
[NRCS]						
NRCS Charge Current	I_{NRCS}	12	20	28	μA	
NRCS Standby Voltage	V_{STB}	-	0	50	mV	V_{EN}=0V
[UVLO]						
V_{CC} Undervoltage Lockout Threshold Voltage	V_{CC}UVLO	3.5	3.8	4.1	V	V_{CC}:Sweep-up
V_{CC} Undervoltage Lockout Hysteresis Voltage	V_{CC}HYS	100	160	220	mV	V_{CC}:Sweep-down
V_{IN} Undervoltage Lockout Threshold Voltage	V_{IN}UVLO	0.72	0.84	0.96	V	V_{IN}:Sweep-up
[SCP]						
SCP Start up Voltage	V_{OSCP}	V_O×0.3	V_O×0.4	V_O×0.5	V	
SCP Threshold Voltage	T_{SCP}	45	90	200	μsec	

●Reference Data

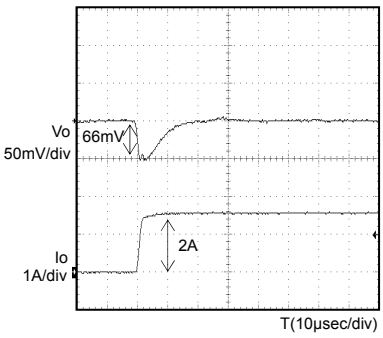


Fig.1 Transient Response
(0A→1.5A)
Co=100µF
cfb=1000pF

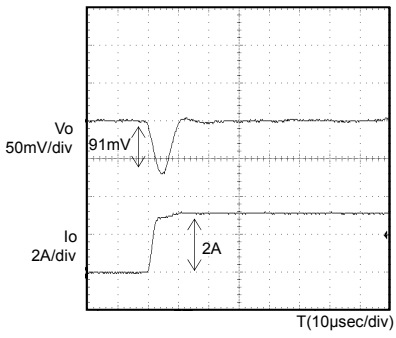


Fig.2 Transient Response
(0A→1.5A)
Co=47µF
cfb=1000pF

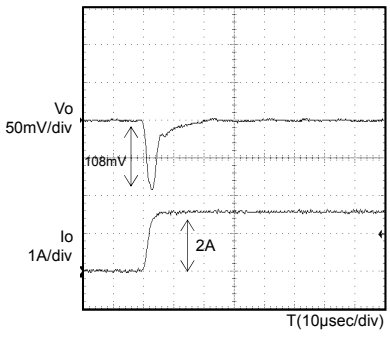


Fig.3 Transient Response
(0A→1.5A)
Co=22µF
cfb=1000pF

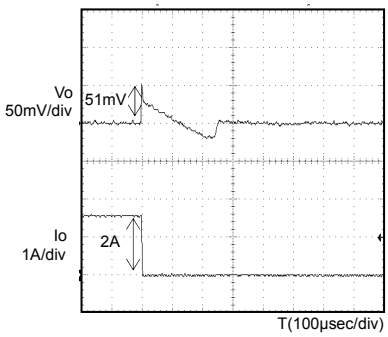


Fig.4 Transient Response
(1.5A→0A)
Co=100µF
cfb=1000pF

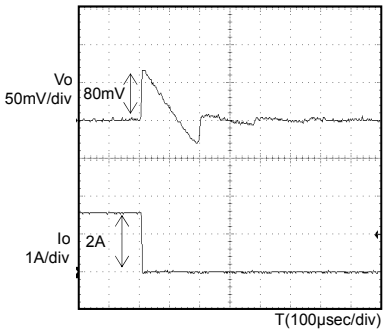


Fig.5 Transient Response
(1.5A→0A)
Co=47µF
cfb=1000pF

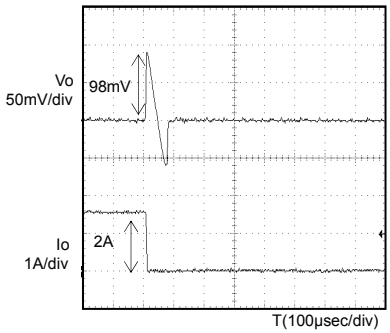


Fig.6 Transient Response
(1.5A→0A)
Co=22µF
cfb=1000pF

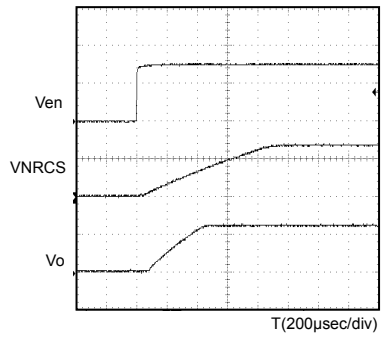


Fig.7 Waveform at output start

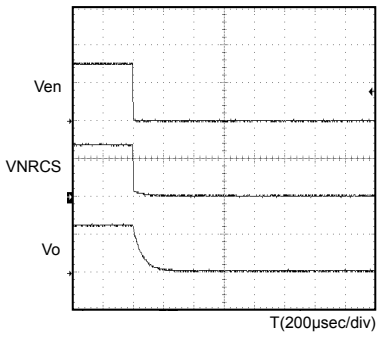


Fig.8 Waveform at output OFF

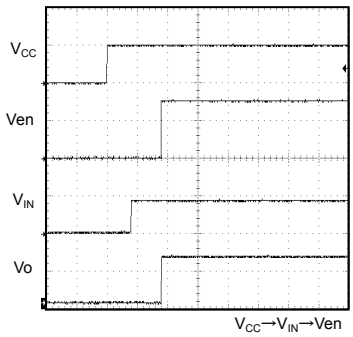


Fig.9 Input sequence

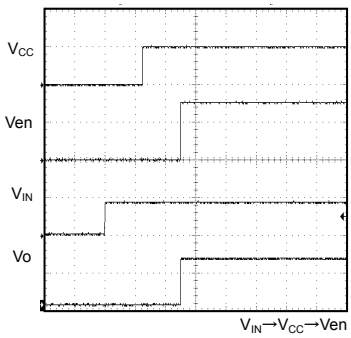


Fig.10 Input sequence

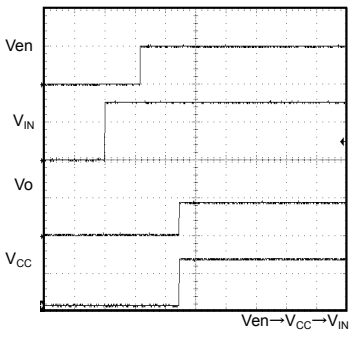


Fig.11 Input sequence

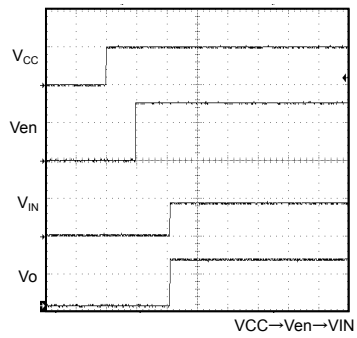


Fig.12 Input sequence

●Reference Data

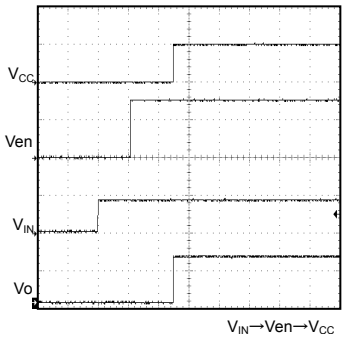


Fig.13 Input sequence

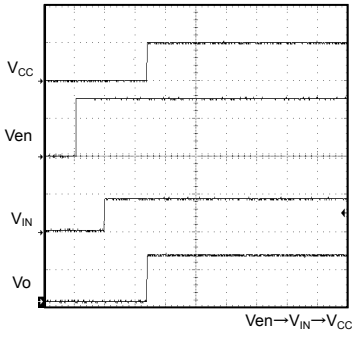


Fig.14 Input sequence

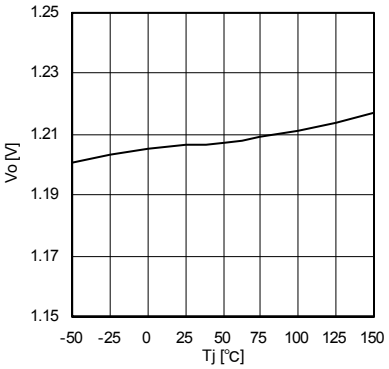


Fig.15 Tj-Vo (Io=0mA)

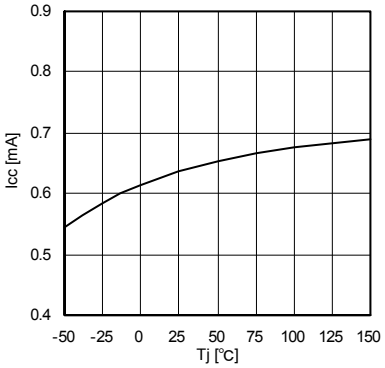


Fig.16 Tj-ICC

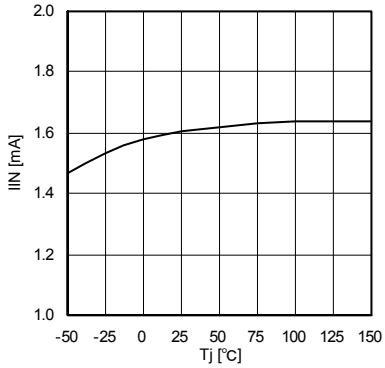


Fig.17 Tj-IIN

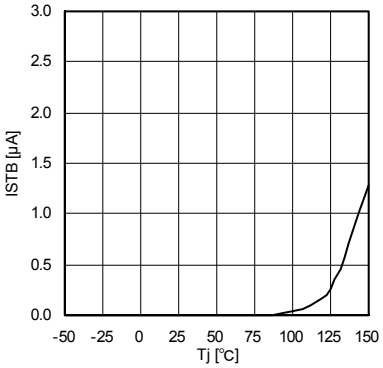


Fig.18 Tj-ICCSTB

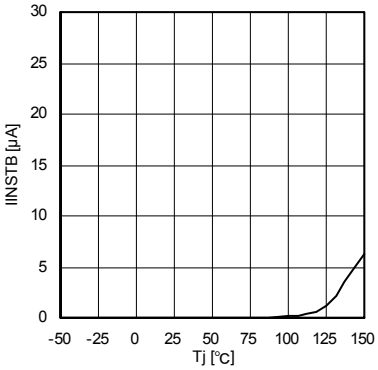


Fig.19 Tj-IINSTB

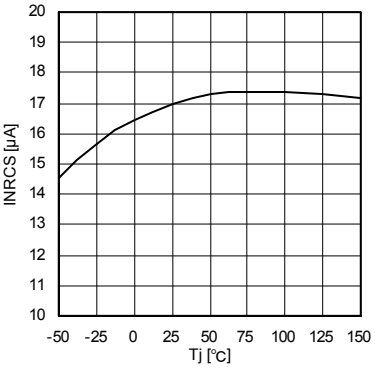


Fig.20 Tj-NRCS

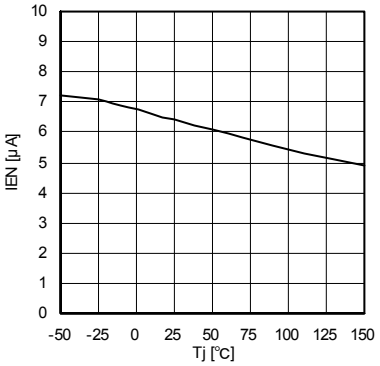


Fig.21 Tj-IEN

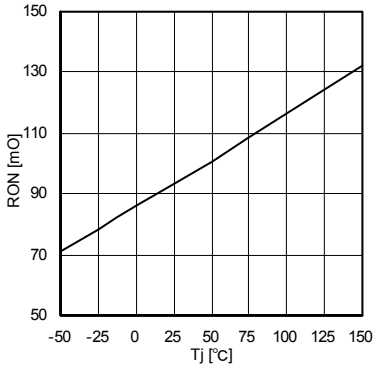


Fig.22 Tj-RON
(Vcc=5V/Vo=1.2V)

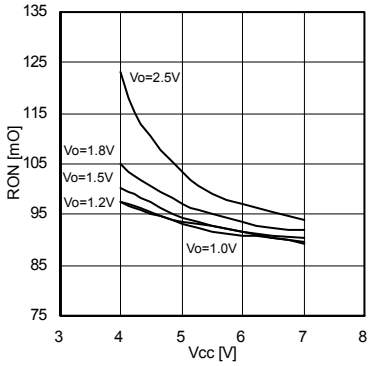
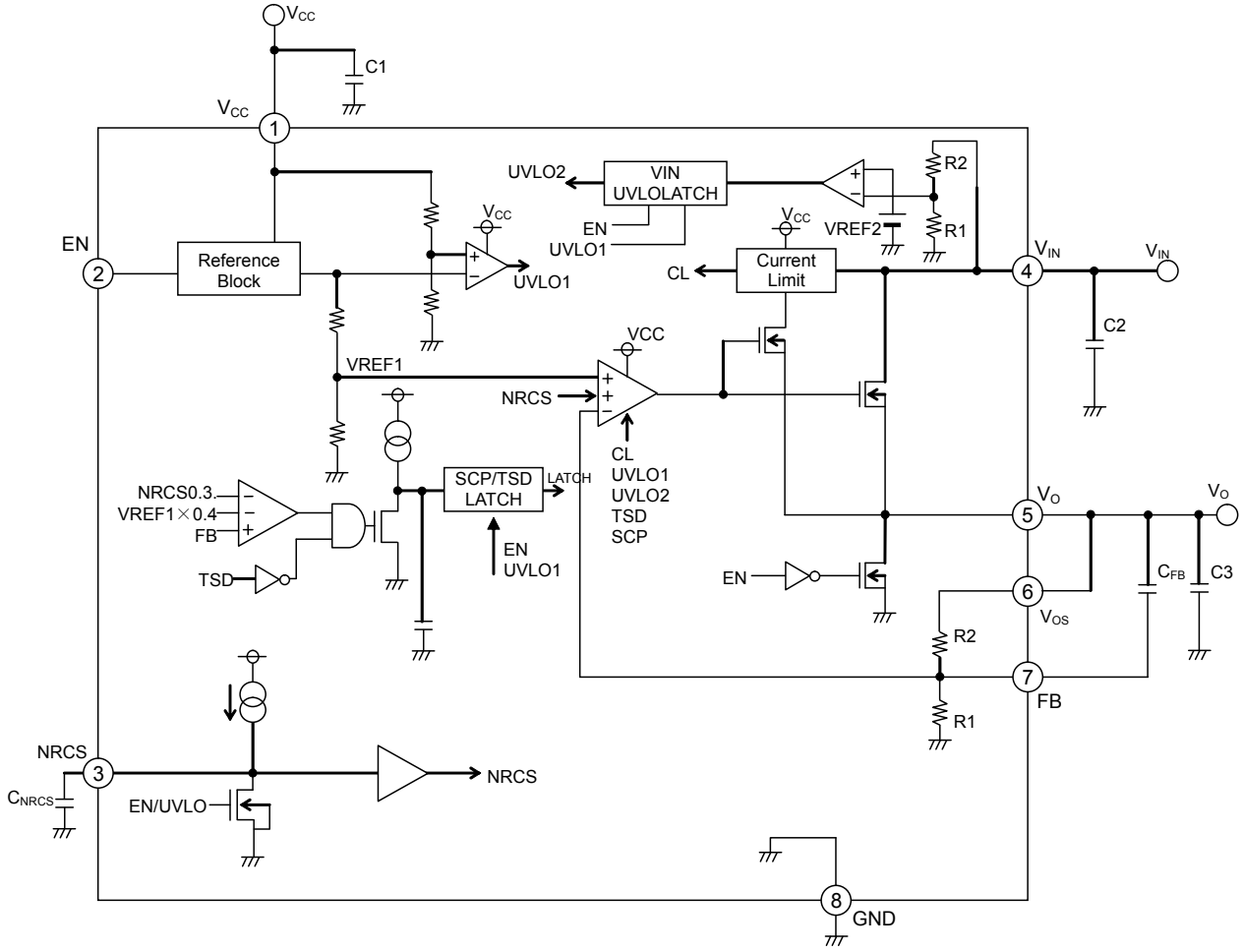
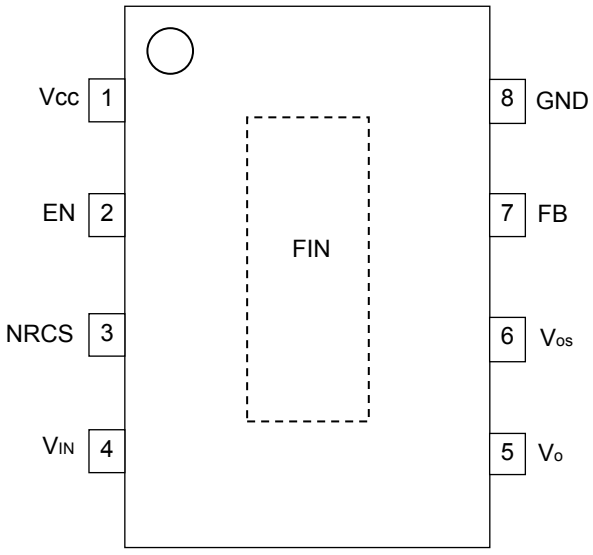


Fig.23 Vcc- RON

●Block Diagram



●Pin Layout



●Pin Function

PIN No.	PIN name	PIN Function
1	V_{CC}	Power Supply Pin
2	EN	Enable Input Pin
3	NRCS	In-rush Current Protection (NRCS) Capacitor Connection Pin
4	V_{IN}	Input Voltage Pin
5	V_O	Output Voltage Pin
6	V_{OS}	Output Voltage Control Pin
7	FB	Reference Voltage Feedback Pin
8	GND	Ground Pin
-	FIN	Connected to heatsink and GND

●Operation of Each Block

・AMP

This is an error amp that compares the reference voltage (0.65V) with V_O to drive the output Nch FET (Ron=150mΩ). Frequency optimization helps to realize rapid transient response, and to support the use of ceramic capacitors on the output capacitors. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to V_{CC}. When EN is OFF, or when UVLO is active, output goes LOW and the output of the NchFET switches OFF.

・EN

The EN block controls the regulator's ON/OFF state via the EN logic input pin. In the OFF position, circuit voltage is maintained at 0μA, thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin V_O, thereby draining the excess charge and preventing the IC on the load side from malfunctioning. Since no electrical connection is required (e.g. between the V_{CC} pin and the ESD prevention diode), module operation is independent of the input sequence.

・V_{CC}UVLO

To prevent malfunctions that can occur during a momentary decrease in V_{CC}, the UVLO circuit switches the output OFF, and (like the EN block) discharges NRCS and V_O. Once the UVLO threshold voltage (TYP3.80V) is reached, the power-on reset is triggered and output continues.

・V_{IN}UVLO

When V_D voltage exceeds the threshold voltage, V_DUVLO becomes active. Once active, the status of output voltage remains ON even if V_D voltage drops. (When V_{IN} voltage drops, SCP engages and output switches OFF.)
Unlike EN and V_{CC}, it is effective at output startup. V_DUVLO can be restored either by reconnecting the EN pin or V_{CC} pin.

・CURRENT LIMIT

When output is ON, the current limit function monitors the internal IC output current against the parameter value. When current exceeds this level, the current limit module lowers the output current to protect the load IC. When the overcurrent state is eliminated, output voltage is restored to the parameter value. However, when output voltage falls to or below the SCP startup voltage, the SCP function becomes active and the output switches OFF.

・NRCS (Non Rush Current on Start-up)

The soft start function enabled by connecting an external capacitor between the NRCS pin and ground. Output ramp-up can be set for any period up to the time the NRCS pin reaches V_{FB} (0.65V). During startup, the NRCS pin serves as a 20μA (TYP) constant current source to charge the external capacitor. Output start time is calculated via the formula below.

$$T_{NRCS}(\text{typ.}) = \frac{C_{NRCS} \times V_{FB}}{I_{NRCS}}$$

・TSD (Thermal Shut down)

The shutdown (TSD) circuit automatically is latched OFF when the chip temperature exceeds the threshold temperature after the programmed time period elapses, thus serving to protect the IC against "thermal runaway" and heat damage. Because the TSD circuit is intended to shut down the IC only in the presence of extreme heat, it is crucial that the Tj (max) parameter not be exceeded in the thermal design ,in order to avoid potential problems with the TSD.

・V_{IN}

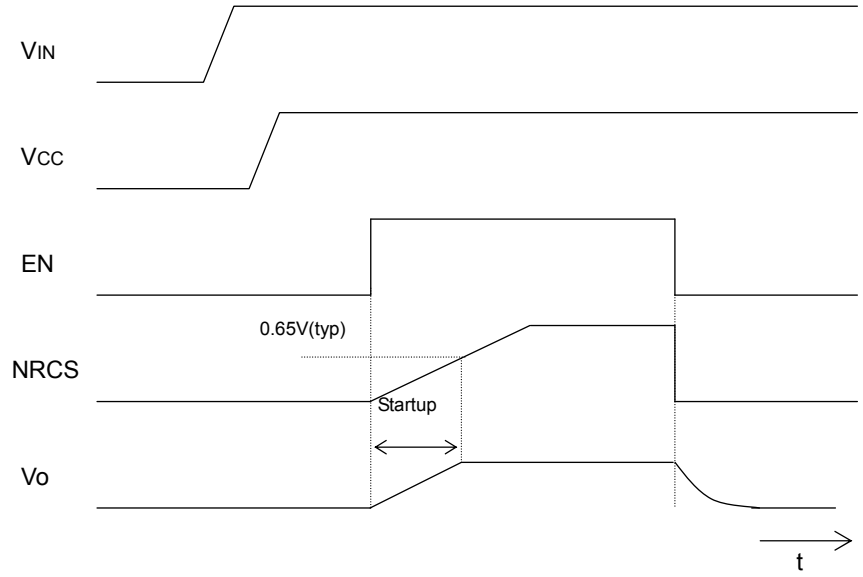
The V_{IN} line acts as the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the V_{CC} pin and the ESD protection diode) is necessary, V_{IN} operates independent of the input sequence. However, since an output NchFET body diode exists between V_{IN} and V_O, a V_{IN}-V_O electric (diode) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to V_{IN} from V_O.

・SCP

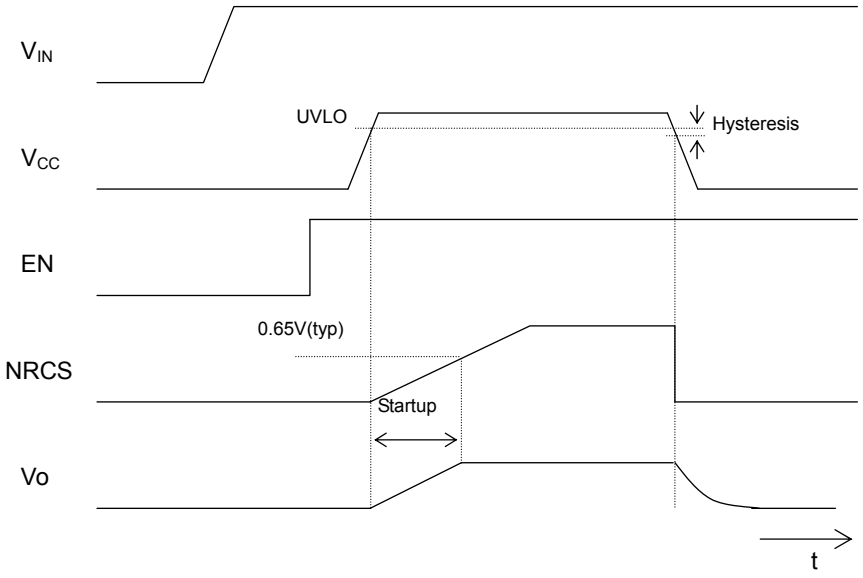
When output voltage (Vo) drops, the IC assumes that V_O pin is shorted to GND and switches the output voltage OFF. After the GND short has been detected and the programmed delay time has elapsed, output is latched OFF. It is also effective during output startup. SCP can be cleared either by reconnecting the EN pin or V_{CC} pin.

●Timing Chart

EN ON/OFF

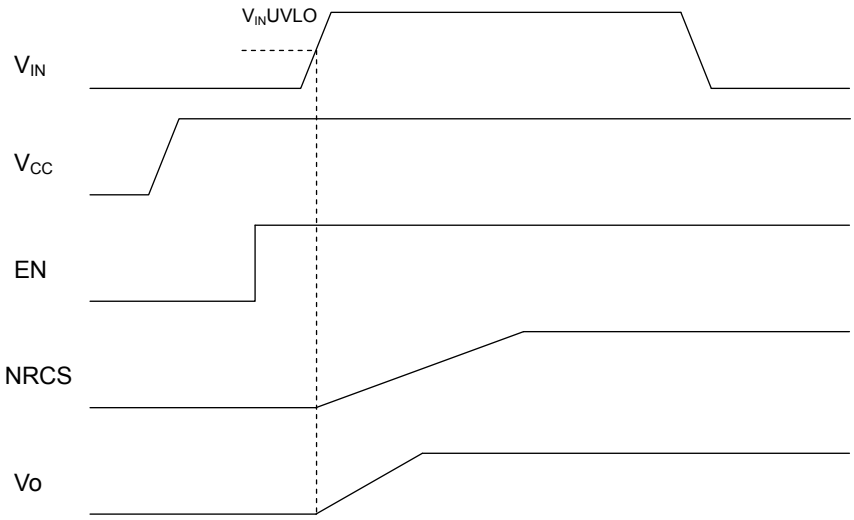


V_{CC} ON/OFF

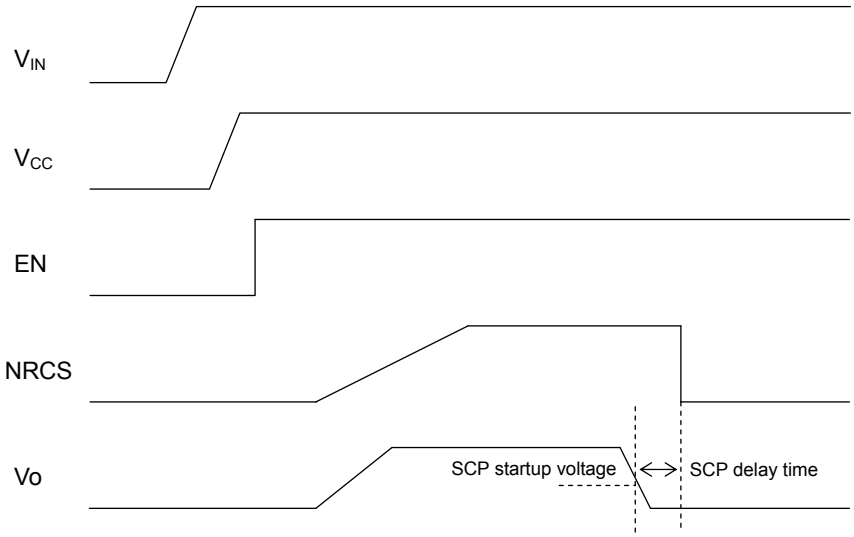


●Timing Chart

V_{IN} ON

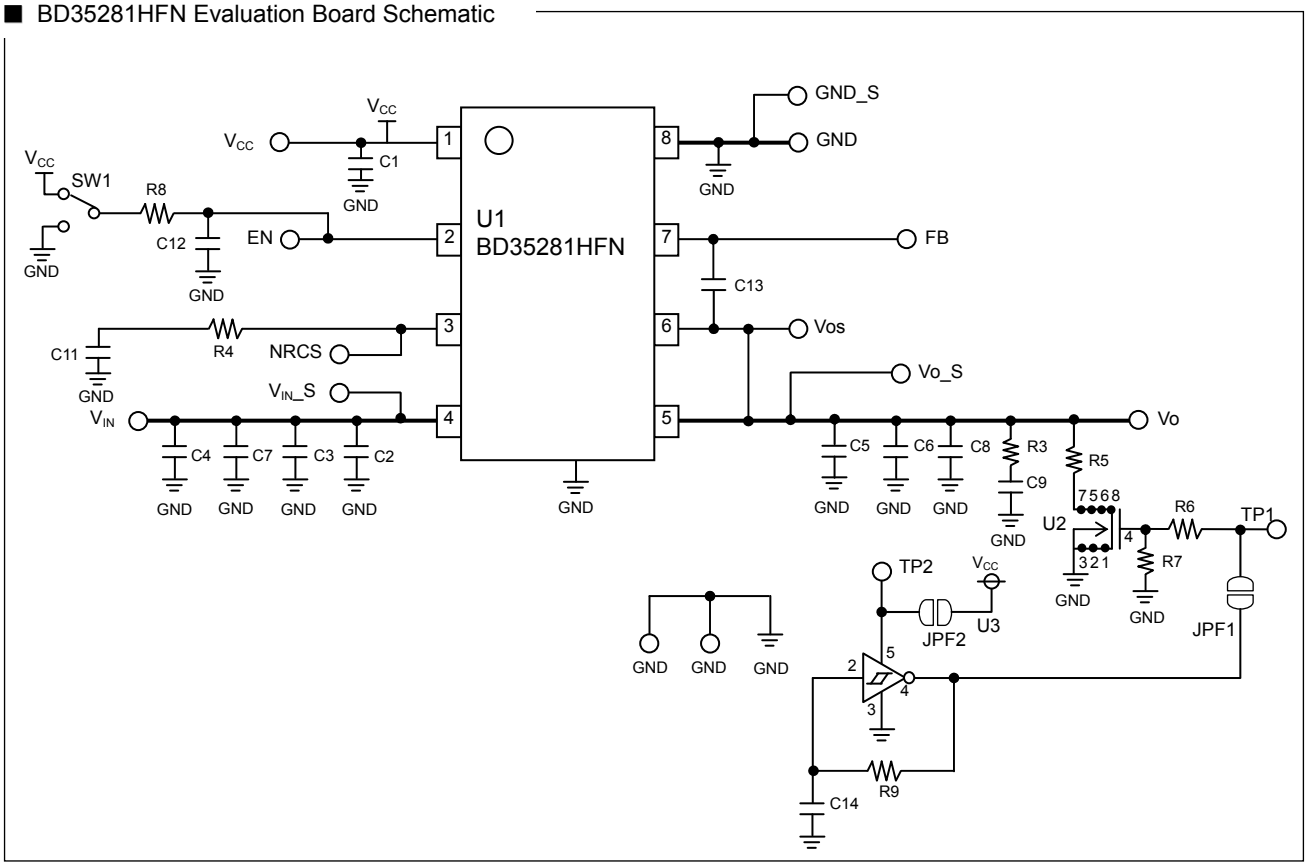


SCP OFF



●Evaluation Board

■ BD35281HFN Evaluation Board Schematic

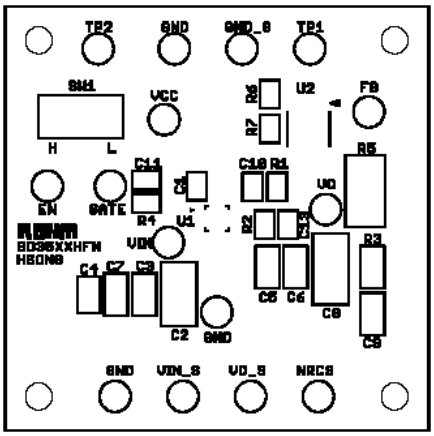


■BD35281HFN Evaluation Board List

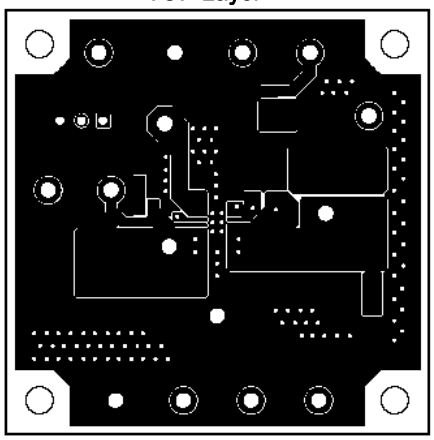
Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD35281HFN
C1	1μF	MURATA	GRM188B11A105KD
C3	10μF	KYOCERA	CM32X5R226M10A
C5	22μF	KYOCERA	CM32X5R226M10A
C11	0.01μF	MURATA	GRM188B11H103KD
C13	1000pF	MURATA	GRM188B11H102KD
R4	0Ω	-	Jumper
R8	0Ω	-	Jumper

■BD35281HFN Evaluation Board Layout
(2nd layer and 3rd layer are GND line.)

Silk Screen



TOP Layer



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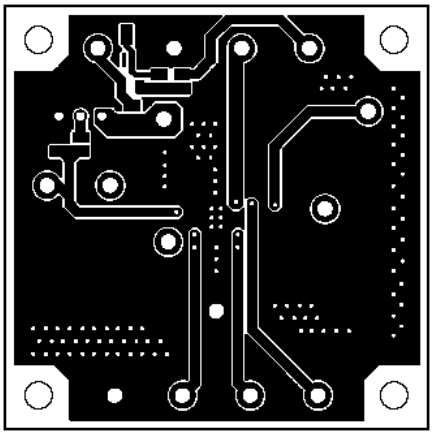
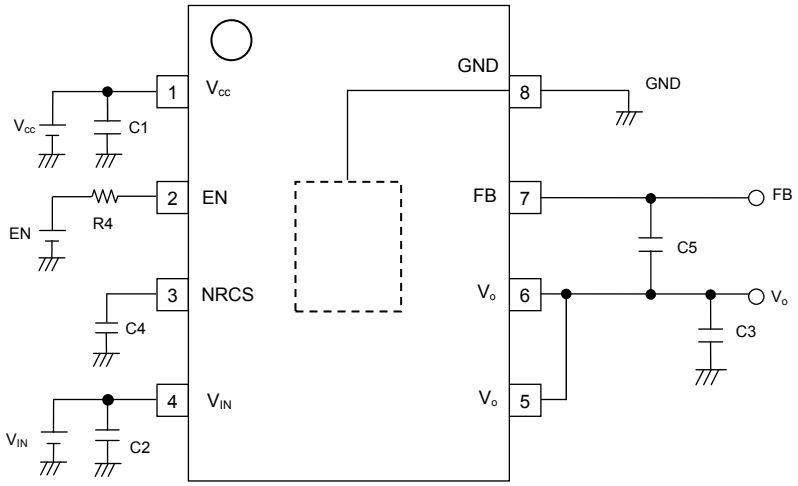


●Recommended Circuit Example



Component	Recommended Value	Programming Notes and Precautions
C3	22µF	To assure output voltage stability, please be certain the output capacitors are connected between Vo pin and GND. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 22µF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.
C1	1µF	Input capacitors reduce the output impedance of the voltage supply source connected to the (V_{CC}) input pins. If the impedance of this power supply were to increase, input voltage (V_{CC}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 1µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C2	10µF	Input capacitors reduce the output impedance of the voltage supply source connected to the (V_{IN}) input pins. If the impedance of this power supply were to increase, input voltage (V_{IN}) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 10µF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C4	0.01µF	The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (V_{IN} to V_O) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.
C5	1000pF	This component is employed when the C3 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.

●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 100℃.
2. Chip junction temperature (Tj) can be no higher than 150℃.

Chip junction temperature can be determined as follows:

① Calculation based on ambient temperature (Ta)

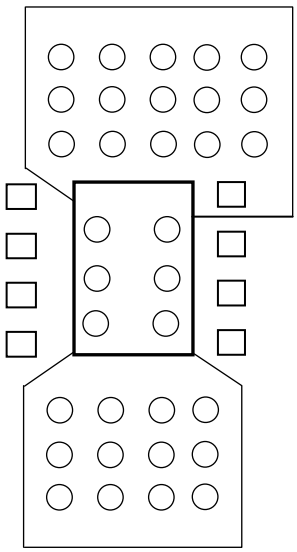
$Tj=Ta+\theta j\text{-}a \times W$

＜Reference values＞

θ j-a:HSON8 198.4℃/W 1-layer substrate (copper foil area : below 0.2%)
92.4℃/W 1-layer substrate (copper foil area : 7%)
71.4℃/W 2-layer substrate (copper foil area : 65%)

Substrate size: $70 \times 70 \times 1.6mm^3$ (substrate with thermal via)

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 2.9mm × 3.0mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below enable to get the superior heat radiation characteristic. (This figure is the image. It is recommended that the VIA size and the number is designed suitable for the actual situation.).



Most of the heat loss that occurs in the BD35281HFN is generated from the output Nch FET. Power loss is determined by the total V_{IN}-Vo voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the V_{IN} and Vo in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3523XHFN) make certain to factor conditions such as substrate size into the thermal design.

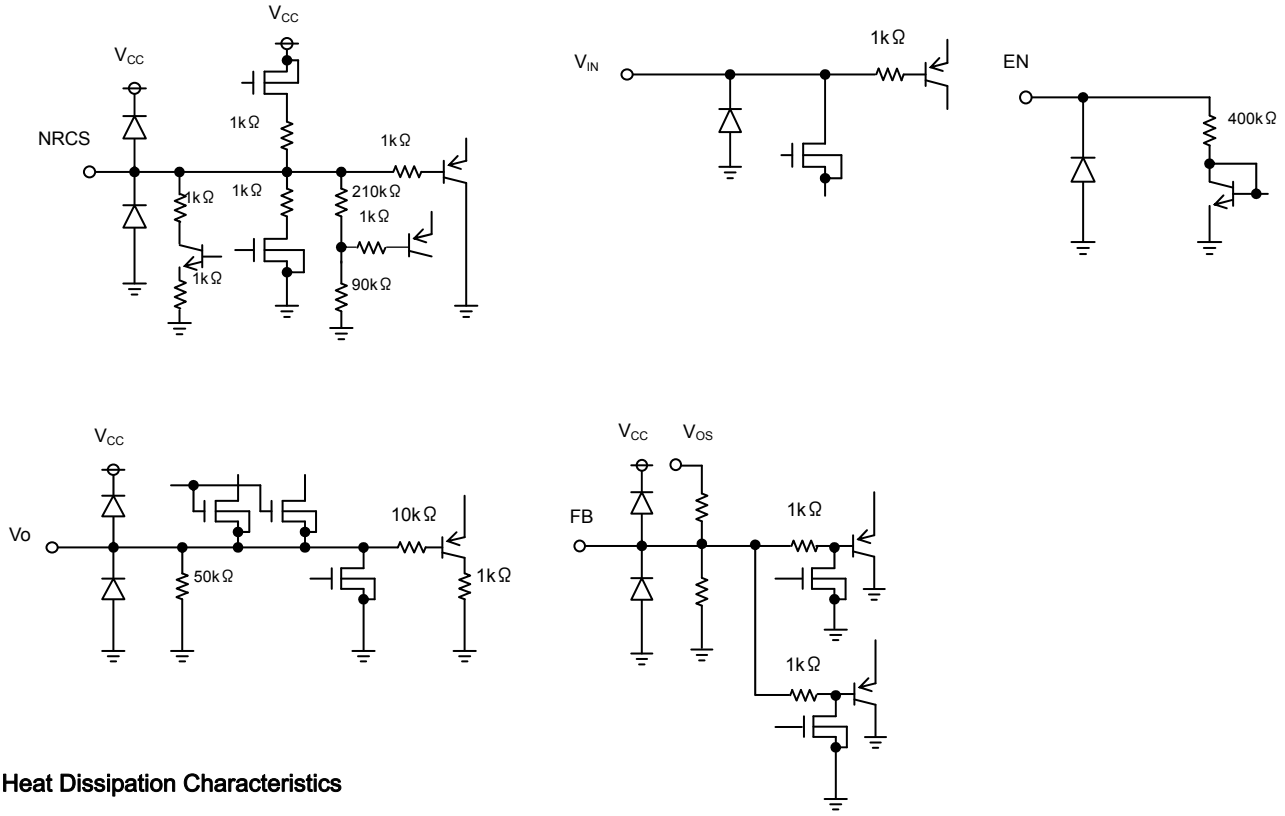
$$\text{Power consumption (W)} = \{\text{Input voltage } (V_{IN}) - \text{Output voltage } (V_O)\} \times Io(Ave)$$

Example)

Where V_{IN}=1.7V, Vo=1.2V, Io(Ave) = 2A,

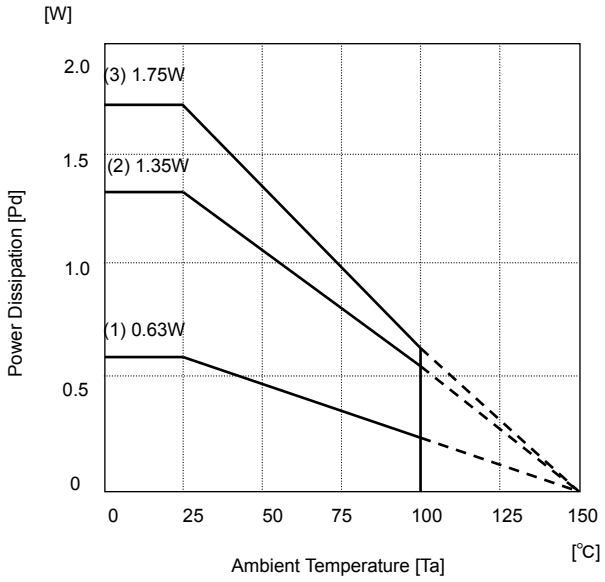
$$\text{Power consumption (W)} = \{1.7\,(V) - 1.2\,(V)\} \times 2.0(A)$$
$$= 1.0(W)$$

●Input-Output Equivalent Circuit Diagram



●Heat Dissipation Characteristics

◎HSON8



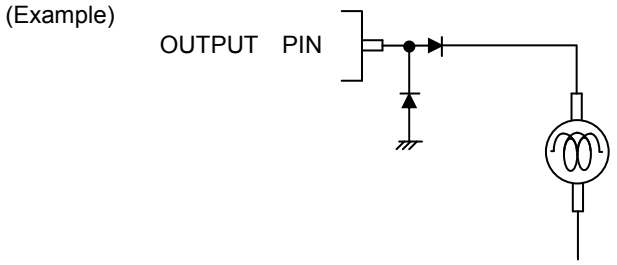
(1) 1 layer substrate (substrate surface copper foil area: below 0.2%)
θ j-a=198.4℃/W
(2) 2 layer substrate (substrate surface copper foil area:7%)
θ j-a=92.4℃/W
(3) 2 layer substrate (substrate surface copper foil area:65%)
θ j-a=71.4℃/W

●Notes for use

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward
   Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines
   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.



4. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO
   When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit
   The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)
BD35281HFN	175

10. Testing on application boards
    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

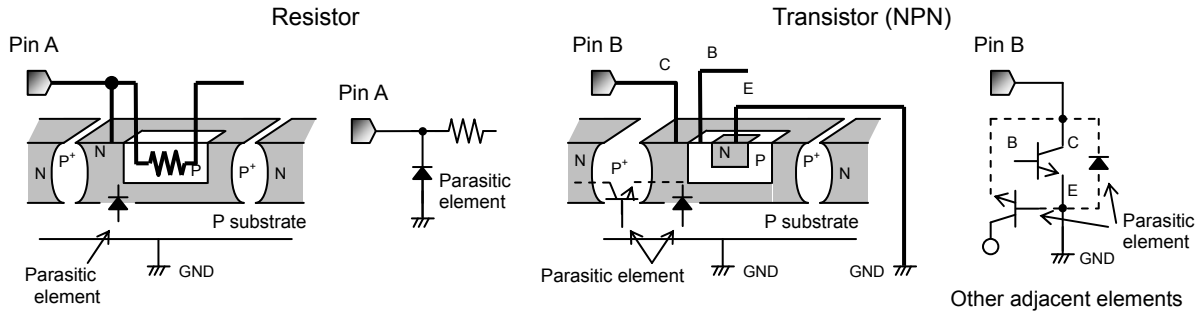
11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



Example of IC structure

12. Ground Wiring Pattern.

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Ordering part number

B	D	3	5	2	8	1	H	F	N	-	T	R

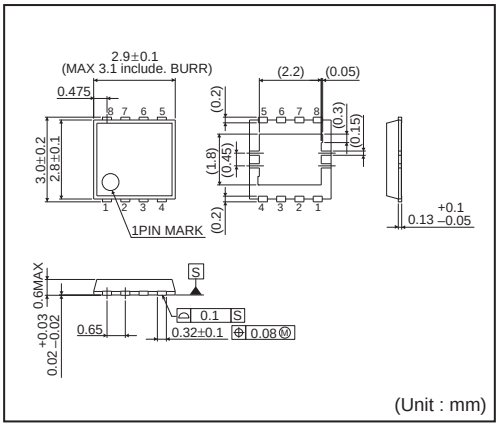
Part No.

Part No.

Package
HFN: HSON8

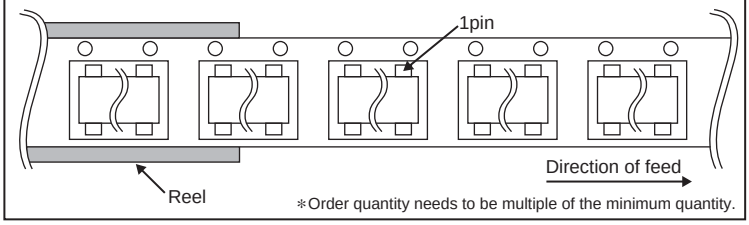
Packaging and forming specification
TR: Embossed tape and reel

HSON8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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