Audio sound controller
BH3857AFV

The BH3857AFV is a signal-processing IC for controlling audio quality in CD radio-cassette players and mini-component stereo systems. Three-line serial control is available making it easy to adjust tone and volume using a microprocessor.

●Applications
Mini-component stereo systems, CD radio cassette players, car audio systems and TVs.

●Features
1) Volume (main volume) and tone (bass and treble) control possible by direct serial link to a microprocessor. DC control is also possible.
2) Volume control is done with a low-distortion, low-noise VCA, and step noise is suppressed.
3) The gain of the input amplifier can be adjusted, and two surround matrixes are available to expand the sound.

4) The IC includes a stable reference voltage source and input buffer to reduce external component requirements, and comes in a compact 40-pin SSOP package that is perfect for compact designs.
5) Four open-collector outputs are provided to make logic control possible.

●Absolute maximum ratings (Ta = 25°C)

| Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	10.0	V
Power dissipation	Pd	1000	mW
Operating temperature	Topr	$-40\sim+85$	℃
Storage temperature	Tstg	$-55\sim+150$	℃
Port pin voltage	PORT1$\sim$PORT4	15.0	V
Control pin applied voltage	Vc, Tc Bc, Sc	V_{ref}	V

＊ Reduced by 8mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	5.4	8.0	9.5	V

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●Block diagram
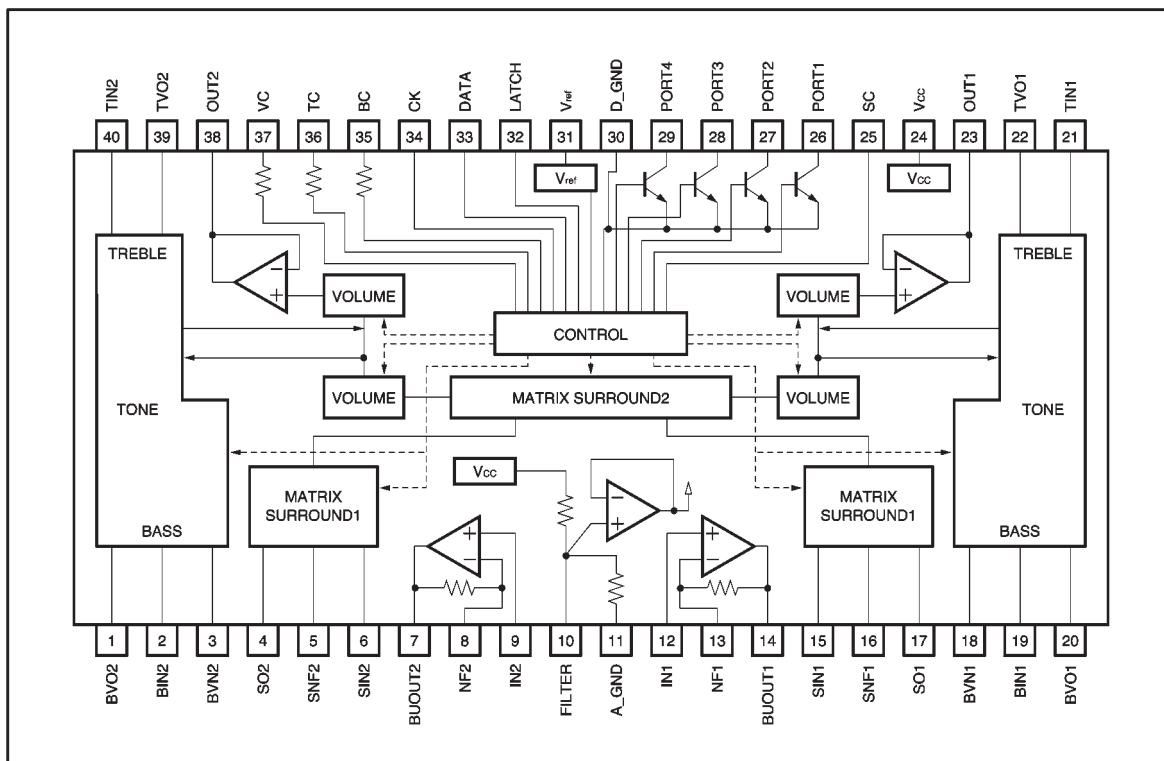
◎ Control of volume, bass, treble and surround 2 can also be done by external application of a DC voltage to the VC (volume), BC (bass), TC (treble) and SC (surround 2) terminals.

◎ The impedance of the VC, TC, and BC terminals is 10kΩ (Typ.).

◎ The impedance of the SC terminal is 200kΩ (Typ.).

●Pin descriptions

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	BVO2	Channel 2 bass filter	21	TIN1	Channel 1 treble filter
2	BIN2	Channel 2 bass filter	22	TVO1	Channel 1 treble filter
3	BVN2	Channel 2 bass filter	23	OUT1	Channel 1 volume output
4	SO2	Channel 2 surround constant setting	24	V_{CC}	Power supply
5	SNF2	Channel 2 surround constant setting	25	SC	Time constant setting terminal to prevent switching shock
6	SIN2	Channel 2 surround input	26	PORT1	Port output
7	BUOUT2	Input-stage amplifier output	27	PORT2	Port output
8	NF2	Input-stage amplifier gain setting	28	PORT3	Port output
9	IN2	Channel 2 volume input	29	PORT4	Port output
10	FILTER	Filter	30	D_GND	Digital ground
11	A_GND	Analog ground	31	V_{ref}	Reference voltage output
12	IN1	Channel 1 volume input	32	LATCH	Latch input
13	NF1	Input-stage amplifier gain setting	33	DATA	Data input
14	BUOUT1	Input-stage amplifier output	34	CK	Clock input
15	SIN1	Channel 1 surround input	35	BC	Time constant setting terminal to prevent switching shock
16	SNF1	Channel 1 surround constant setting	36	TC	Time constant setting terminal to prevent switching shock
17	SO1	Channel 1 surround constant setting	37	VC	Time constant setting terminal to prevent switching shock
18	BVN1	Channel 1 bass filter	38	OUT2	Channel 2 volume output
19	BIN1	Channel 1 bass filter	39	TVO2	Channel 2 treble filter
20	BVO1	Channel 1 bass filter	40	TIN2	Channel 2 treble filter

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●Electrical characteristics　(unless otherwise noted, Ta = 25°C, V_{CC} = 8V, f = 1kHz, BW = 20Hz to 20kHz,
VOL = MAX, Tone = ALL FLAT, R_g = 600Ω, R_L = 10kΩ, INPUT_AMP_GAIN = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Quiescent current	I_Q	9	19	26	mA	No signal	
Maximum input voltage	V_{im}	1.7	1.9	—	V_{rms}	THD＝1％, V_{OL}＝－20dB（ATT）	
Maximum output voltage	V_{om}	1.8	2.0	—	V_{rms}	THD＝1％	
Voltage gain	G_V	−2.0	0.0	＋2.0	dB	V_{IN}＝1V_{rms}	
Maximum attenuation	ATT	90	110	—	dB	V_O＝1V_{rms}	
Crosstalk	V_{CT}	64	70	—	dB	V_O＝1V_{rms}, BPF＝400Hz～30kHz	
Bass control range	VBmax	＋12	＋15	＋18	dB	75Hz, V_{IN}＝100mV_{rms}	
	VBmin	−18	−15	−12	dB	75Hz, V_{IN}＝100mV_{rms}	
Treble control range	VTmax	＋12	＋15	＋18	dB	10kHz, V_{IN}＝100mV_{rms}	
	VTmin	−18	−15	−12	dB	10kHz, V_{IN}＝100mV_{rms}	
Mute attenuation	V_{MT}	90	110	—	dB	V_O＝1V_{rms}	＊
Total harmonic distortion	THD	—	0.03	0.1	％	V_O＝0.3V_{rms}, BPF＝400Hz～30kHz	
Output noise voltage	V_{NO}1	—	25	34	μV_{rms}	No signal, V_{OL}＝MAX, Rg＝0	＊
Output residual noise voltage at full boost	V_{NO}2	—	80	120	μV_{rms}	No signal, TONE＝ALL MAX, V_{OL}＝MAX, Rg＝0	＊
Residual output noise voltage	VM_{NO}	—	2	10	μV_{rms}	No signal, V_{OL}＝-infinity, Rg＝0	＊
Reference power supply output voltage	V_{ref}	3.5	3.8	4.1	V	I_{ref}＝3mA	
Reference power supply output current capacity	I_{ref}	3.0	10	—	mA	V_{ref}＞3.7V	
Channel balance	G_{CB}	−2.0	0	＋2.0	dB	Measured with respect to Ch1	
Port output current	I_{PMAX}	5.0	—	—	mA	—	
Output low level voltage	V_{OL}	—	0.4	0.5	V	I_{OL}＝5mA	
"H" output disable current	I_{OZH}	—	—	1.0	μA	V_O＝5V	
Volume attenuation (-10dB)	ATT10	−12.0	−10.0	−8.0	dB	V_{IN}＝0dBV, gain when control data 10101010 is input.	
SC pin (on voltage)	SC_{ON}	—	0	0.5	V	—	
VC pin impedance	R_{VC}	8.0	10	12	kΩ	—	
BC pin impedance	R_{BC}	8.0	10	12	kΩ	—	
TC pin impedance	R_{TC}	8.0	10	12	kΩ	—	
SC pin impedance	R_{SC}	160	200	240	kΩ	—	

＊ Measurement performed using Matsushita Communication Industrial VP-9690A DIN AUDIO filter (average value wave detection, effective value display). Operating specifications: same phase for the input and output signals.
◎Not designed for radiation resistance.
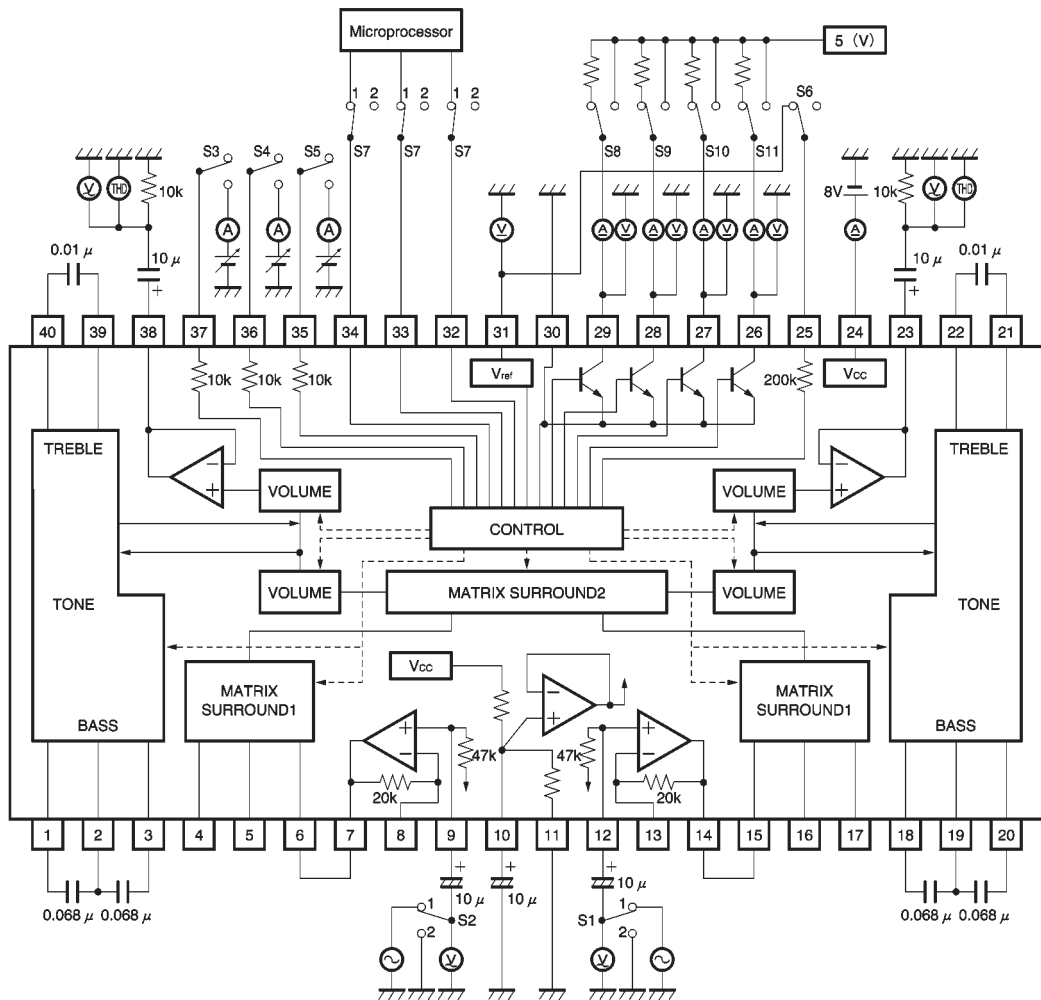
●Measurement circuit

Fig. 1

●Circuit operation

(1)   About the data format

As shown in Fig. 2, there are 32 bits of data. When the power is applied, a reset is applied to switch ports 1 to 4 off, but the reset is not applied to the other ports, so they are unstable. For this reason, it is necessary to input the data at least once while the set mute circuit is on.
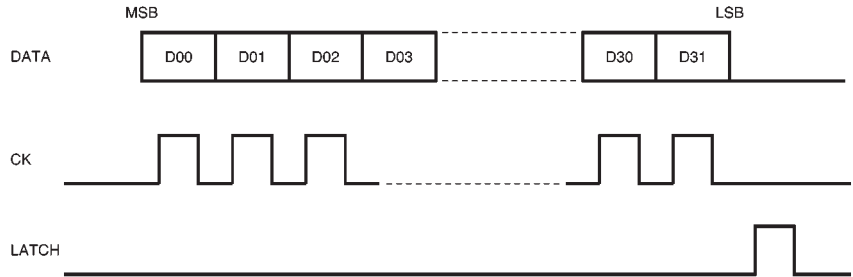

Fig. 2

Data	Function
D00～D07	Volume control
D08～D12	Treble control
D13～D17	Bass control
D18～D19	Surround control
D20～D23	Port control
D24～D31	Chip select + parity

* D18 : Surround matrix 1 control
  D19 : Surround matrix 2 control

D20	D21	D22	D23
Port 1	Port 2	Port 3	Port 4

• Surround is on when the bit data is 0, and off when it is 1.

• With regard to the port 1 to 4 outputs, when the power is on, if no data is input the transistors for each output are set to off. The outputs are on when the bit data is 1, and off when it is 0.

* Apply the following data for chip select and parity.

D24 · · · · · · D31
0 1 0 1 0 1 1 1

(2) Logic input terminals

Logic input terminals have a bipolar construction, so take care with regard to source current.

(3) Timing chart

The timing chart is shown in Fig. 3.
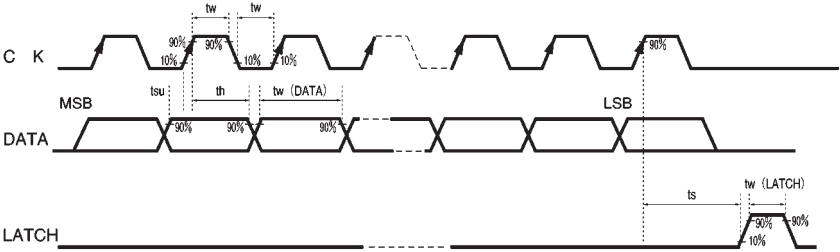
Timing (recommended conditions)

Fig.3

Timing chart constants

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input high level voltage	V_{IH}	4.0	5.0	6.0	V
Input low level voltage	V_{IL}	—	0	1.0	V
Minimum clock width	tw	2.0	—	—	μs
Minimum data width	tw (DATA)	2.0	—	—	μs
Minimum latch width	tw (LATCH)	2.0	—	—	μs
Setup time (DATA to CLK)	tsu	1.0	—	—	μs
Hold time (CLK to DATA)	th	1.0	—	—	μs
Setup time (CLK to LATCH)	ts	1.0	—	—	μs

∗ Hold the logic terminal inputs at a "L" voltage until the voltage on the Vcc terminal reaches the minimum operating voltage (5.4V). The port terminals (pins 26 to 29) are off (open) at this time.

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(4)　Data table

The transmission data is given in the table below.

Volume data settings (reference values)

Hex display	Volume gain	MSB V8	V7	V6	V5	V4	V3	V2	LSB V1	
FF	0dB	1	1	1	1	1	1	1	1	
E5	−1dB	1	1	1	0	0	1	0	1	
DB	−2dB	1	1	0	1	1	0	1	1	
D3	−3dB	1	1	0	1	0	0	1	1	
CC	−4dB	1	1	0	0	1	1	0	0	
C6	−5dB	1	1	0	0	0	1	1	0	
C0	−6dB	1	1	0	0	0	0	0	0	
BA	−7dB	1	0	1	1	1	0	1	0	
B5	−8dB	1	0	1	1	0	1	0	1	
B0	−9dB	1	0	1	1	0	0	0	0	10
AB	−10dB	1	0	1	0	1	0	1	1	
A7	−11dB	1	0	1	0	0	1	1	1	
A3	−12dB	1	0	1	0	0	0	1	1	
9F	−13dB	1	0	0	1	1	1	1	1	
9C	−14dB	1	0	0	1	1	1	0	0	
98	−15dB	1	0	0	1	1	0	0	0	
95	−16dB	1	0	0	1	0	1	0	1	
91	−17dB	1	0	0	1	0	0	0	1	
8E	−18dB	1	0	0	0	1	1	1	0	
8A	−19dB	1	0	0	0	1	0	1	0	20
87	−20dB	1	0	0	0	0	1	1	1	
81	−22dB	1	0	0	0	0	0	0	1	
7B	−24dB	0	1	1	1	1	0	1	1	
75	−26dB	0	1	1	1	0	1	0	1	
70	−28dB	0	1	1	1	0	0	0	0	
6B	−30dB	0	1	1	0	1	0	1	1	
66	−32dB	0	1	1	0	0	1	1	0	
62	−34dB	0	1	1	0	0	0	1	0	
5D	−36dB	0	1	0	1	1	1	0	1	
59	−38dB	0	1	0	1	1	0	0	1	30
55	−40dB	0	1	0	1	0	1	0	1	
51	−42dB	0	1	0	1	0	0	0	1	
4D	−44dB	0	1	0	0	1	1	0	1	
4A	−46dB	0	1	0	0	1	0	1	0	
47	−48dB	0	1	0	0	0	1	1	1	
43	−50dB	0	1	0	0	0	0	1	1	
40	−52dB	0	1	0	0	0	0	0	0	
3D	−54dB	0	0	1	1	1	1	0	1	
3A	−56dB	0	0	1	1	1	0	1	0	40
37	−58dB	0	0	1	1	0	1	1	1	
34	−60dB	0	0	1	1	0	1	0	0	
32	−62dB	0	0	1	1	0	0	1	0	

Hex display	Volume gain	V8	V7	V6	V5	V4	V3	V2	V1
		MSB							LSB
2F	−64dB	0	0	1	0	1	1	1	1
2D	−66dB	0	0	1	0	1	1	0	1
2B	−68dB	0	0	1	0	1	0	1	1
28	−70dB	0	0	1	0	1	0	0	0
26	−72dB	0	0	1	0	0	1	1	0
24	−74dB	0	0	1	0	0	1	0	0
23	−76dB	0	0	1	0	0	0	1	1
21	−78dB	0	0	1	0	0	0	0	1
1F	−80dB	0	0	0	1	1	1	1	1
1E	−82dB	0	0	0	1	1	1	1	0
1C	−84dB	0	0	0	1	1	1	0	0
00	−∞	0	0	0	0	0	0	0	0

Note: The values given in this table are for reference only. Be sure to check them carefully in actual use.

Bass and treble settings (reference values)

Treble data

MSB				LSB	Treble gain (dB)	Hex display
0	0	0	0	0	−15	00
0	0	1	0	0	−14	04
0	0	1	1	0	−12	06
0	1	0	0	0	−10	08
0	1	0	0	1	−8	09
0	1	0	1	0	−6	0A
0	1	0	1	1	−4	0B
0	1	1	0	0	−2	0C
0	1	1	1	1	±0	0F
1	0	1	0	0	+2	14
1	0	1	0	1	+4	15
1	0	1	1	0	+6	16
1	0	1	1	1	+8	17
1	1	0	0	0	+10	18
1	1	0	1	0	+12	1A
1	1	1	0	0	+14	1C
1	1	1	1	1	+15	1F

Bass data

MSB				LSB	Bass gain (dB)	Hex display
0	0	0	0	0	−15	00
0	0	1	0	1	−14	05
0	0	1	1	1	−12	07
0	1	0	0	1	−10	09
0	1	0	1	0	−8	0A
0	1	0	1	1	−6	0B
0	1	1	0	0	−4	0C
0	1	1	0	1	−2	0D
0	1	1	1	1	±0	0F
1	0	0	1	1	+2	13
1	0	1	0	0	+4	14
1	0	1	0	1	+6	15
1	0	1	1	0	+8	16
1	0	1	1	1	+10	17
1	1	0	0	1	+12	19
1	1	0	1	1	+14	1B
1	1	1	1	1	+15	1F

Note: 1.The gain values given in the bass data setting table above are for when the filter constants are set so that the peak or bottom values in the frequency characteristic graph become the maximum or minimum gain values.
2.The values given in this table are for reference only. Be sure to check them carefully in actual use.
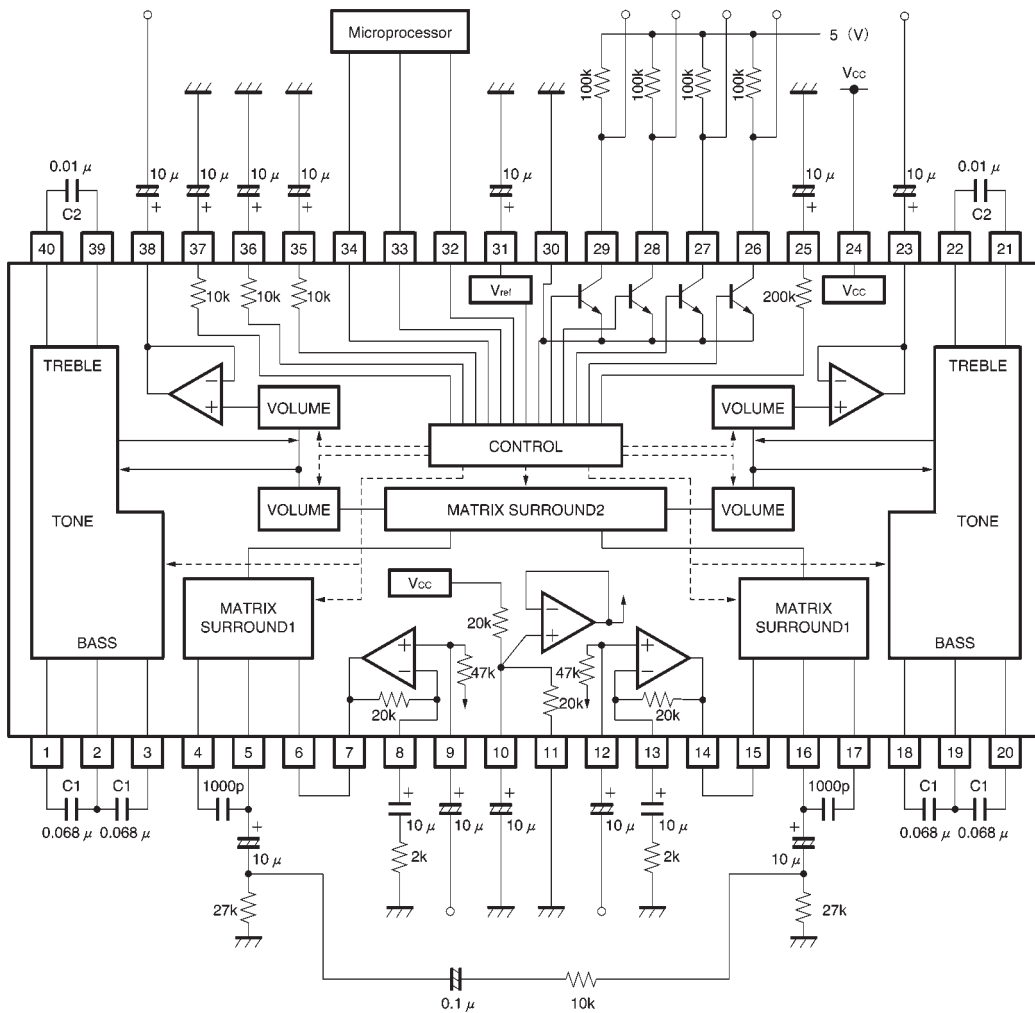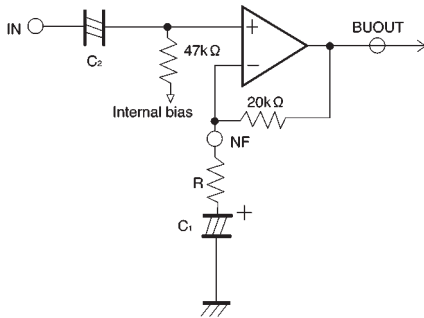
●Application example

Fig. 4
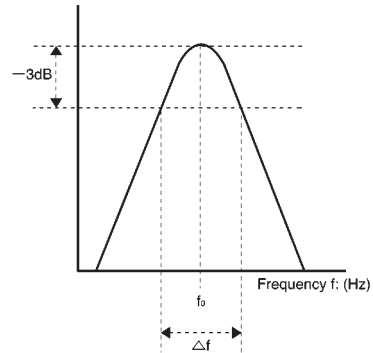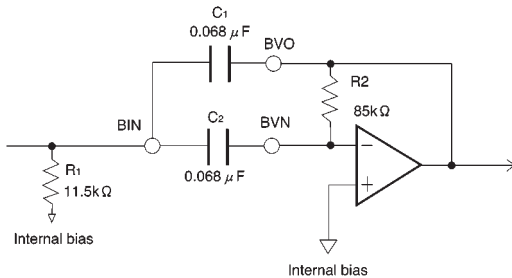
●Attached components

(1)   Input buffer

• The input impedance is 47kΩ.
• A buffer if R and C_1 are not present.
• The gain can be set by R and the 20kΩ.

$$G_{VC} = (R + 20k\Omega) / R$$

Note: Set C_2 (input coupling) and C_1 (used to set the gain) depending on the frequency band used.

(2)   Bass filter

• A band-pass filter is constructed using a multiple-feedback type active filter.
f_0 can be changed using the C valve.

(Theoretical formula)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}} \qquad Q \doteqdot \left[\left(\frac{1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

$$G = \frac{R_2}{5k} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

Note: The filter gain is calculated using these formulas, but the internal circuit must be added to give the total output gain.

(When $R_1 = 11.5k\Omega$, $R_2 = 85k\Omega$, and $C_1 = C_2 = C$)

$$f_0 = \frac{5.1 \times 10^{-6}}{C} \qquad Q \doteqdot 1.36 \quad G = 8.5$$

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(3) Treble filter
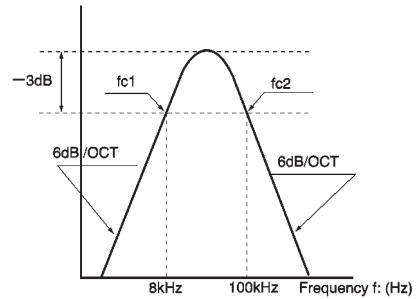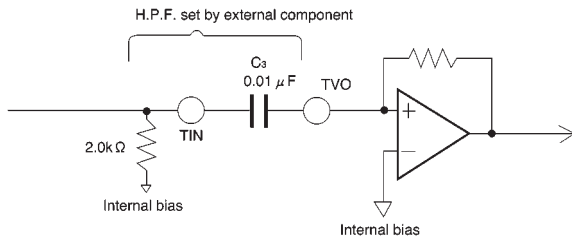
• The bypass filter cutoff frequency (fc1) can be altered by changing the value of the external capacitor C_3.

$$fc1 = \frac{1}{2\pi \times C_3 \times 2k}$$

The recommended value for fc1 is about 8kHz.

• The bandwidth of the internal amplifier is determined by fc2 (about 100kHz).

The tone control provides gain boost or cut over a frequency range that you decide. At the peak and bottom of the frequency characteristic the boost is 15dB, and the cut is -15dB (Typ.). Take the frequency characteristic into consideration when designing the filter.

1) Amount of tone boost
When the amount of volume attenuation is large, the tone control width will change. Reference values are given below.
Note, however, that the actual values will vary due to differences in individual components.

Reference values :
Tone control width at 0dB volume attenuation : ±15.0dB
Tone control width at -40dB volume attenuation : ±13.5dB
Tone control width at -60dB volume attenuation : ±12.0dB

(4) Surround matrix
1) Surround 1
Circuit example
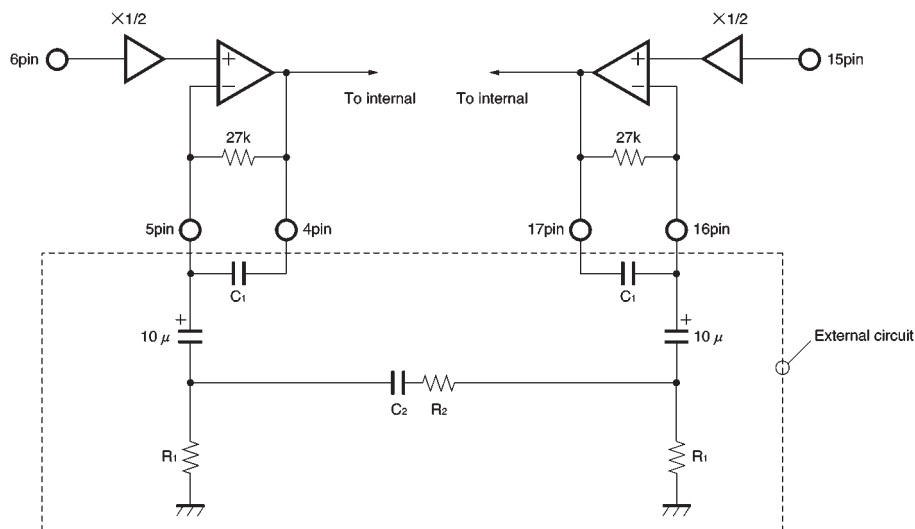
✳ The internal constants for surround for the maintenance products BH3857FV and BH3857AFV are different.

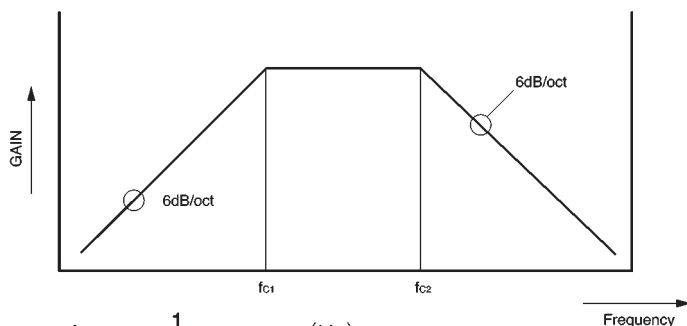| BH3857FV	4.7k
BH3857AFV	27k

• Gain setting

Same-phase gain　　$\dfrac{1}{2} \times \dfrac{R_1 + 27k}{R_1}$　　　　（1ch, 2ch）

Single-phase gain　　$\dfrac{1}{2} \times \dfrac{(R_1//R_2) + 27k}{R_1//R_2}$　　　（1ch）

　　　　　　　　　　$\dfrac{1}{2} \times \dfrac{27k}{R_2}$　　　　　（2ch）
　　　　　　　　　　　　　　　　　　　　　（✳ Channel 1 input, channel 2 AC ground）

Reverse-phase gain　$\dfrac{1}{2} \times \dfrac{(R_1//R_2)/2 + 27k}{(R_1//R_2)/2}$　（1ch, 2ch）

• Mixing signal frequency characteristic settings

$f_{C1} = \dfrac{1}{2\pi\, C_2 R_2}$　　（Hz）

$f_{C2} = \dfrac{1}{2\pi\, C_1 \times 27k}$　　（Hz）

2) Surround 2

(3/2L−1/2R)

(3/2R−1/2L)

◎The surround matrix construction is shown in the diagram on the left.
The gain calculations are given by the formulas in the diagram.

Same-phase gain	0dB
Reverse-phase gain	3.5dB

(However, the reverse-phase gain is input to one channel only)
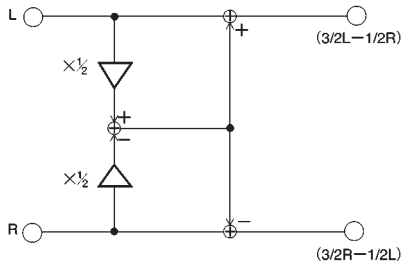
●Operation notes

We guarantee the application example, but recommend that you thoroughly check its characteristics and pay attention to the points of caution given below.If you change any of the external component values, check both the static and transient characteristics of the circuit, and allow sufficient margin in your selections to take into account variations in the components and ICs.

(1)   Operating power supply voltage range

The basic circuit functions are guaranteed to operate if the circuit is operated within the recommended temperature and supply voltage ranges. Please confirm the values of the circuit constants, voltage setting, and temperature in actual use.

(2)   Step switching noise

The VC (pin 37), TC (pin 36), BC (pin 35), and SC (pin 25) terminals have components connected to them in the application example. The values of these components may need to be changed depending on the signal level setting and PCB pattern. Investigate carefully before deciding on the values of the various circuit constants.

The equivalent circuit for these terminals is given below (an integrator circuit is set at the first stage to slow the variation).
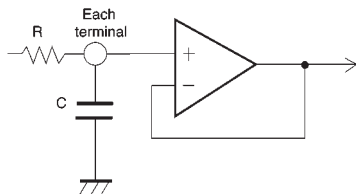
	R value (kΩ)
VC，BC，TC	10
SC	200

(3)   Volume and tone level settings

This specification sheet gives reference values for the amount of attenuation and gain with respect to the serial control data.

The internal D/A convertor is an R-2R circuit, and data exists for the places where continuous variation does not occur between data.

Use this when fine setting is required. The setting limits are up to 8 bits for volume (256 steps) and 5 bits (32 steps) for tone.

(4)   Digital / analog separation

The digital and analog power supplies and grounds are completely separate. The digital circuits are supplied from a stable reference source that is on the chip (V_{ref} (pin 31)). For this reason, there is no need to worry about timing shifts, or interference due to digital noise.

(5)   Output ports

Ports 1 to 4 (pins 26 to 29), are reset when the power is applied. The reset state continues until the next serial data is input.

Note: The CK, DATA and LATCH line data must be held low up until the next data is input after power is applied.

•Do not apply more than 15V to the output ports.

(6)   DC control

An internal impedance of 10kΩ is seen from the VC (pin 37), TC (pin 36), and BC (pin 35) terminals, and 200kΩ is seen from the SC (pin 25) terminal, so with regard to DC control, we recommend direct control with the voltage source.

When using variable volume, take the impedance into consideration when making the setting.

Note: The DC control voltage range is 0V to V_{ref}.

Do not apply voltages above V_{ref} to the terminals.

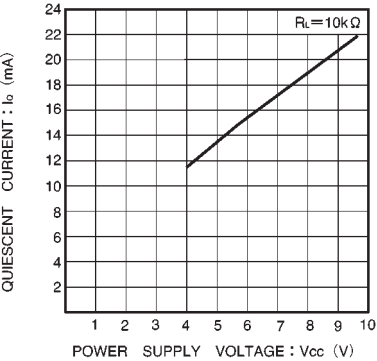●Electrical characteristic curves
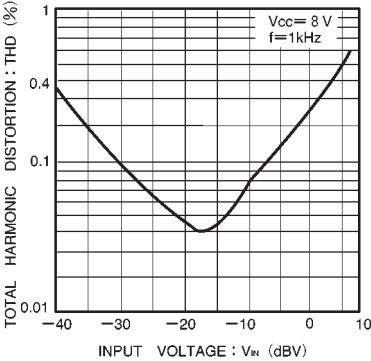
Fig. 5 Quiescent current vs.
power supply voltage

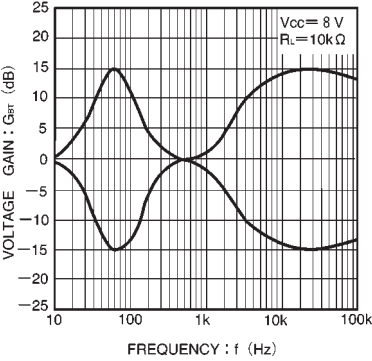Fig. 6 Total harmonic distortion vs.
input voltage

Fig. 7 Output gain vs. frequency

●External dimensions (Units: mm)

SSOP-B40

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