

LVDS Interface ICs

70bit

# LVDS Distributor



BU90RT102

No.10057EAT08

## ●Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operates from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

Driver and Receiver of 4 bits operate to 250MHz. It can be used for a variety of purposes, home appliances such as LCD-TV, business machines such as decoders, instruments, and medical equipment.

## ●Features

- 1) RGB10bits dual channel LVDS Receiver and Transmitter
- 2) Operating frequency range : 20~135MHz
- 3) Power down mode supported.
- 4) Support spread spectrum clock generator.
- 5) Support reduced swing LVDS for low EMI.
- 6) Package HTSSOP-C64

## ●Applications

Digital TV (Signal System)  
Car Navigation System  
Copier  
FA equipment  
Medical equipment  
Vending machine, Ticket vending machine

### ●Absolute Maximum Ratings

| Parameter                 | Symbol    | Ratings             | Unit |
|---------------------------|-----------|---------------------|------|
| Supply Voltage            | $V_{DD}$  | -0.3 ~ 4.0          | V    |
| Input Voltage             | $V_{IN}$  | -0.3 ~ $V_{DD}+0.3$ | V    |
| Output Voltage            | $V_{OUT}$ | -0.3 ~ $V_{DD}+0.3$ | V    |
| Storage Temperature Range | Tstg      | -55 ~ 125           | °C   |

### ●Recommended Operating Conditions

| Parameter                   | Symbol   | Ratings |     |      | Unit |
|-----------------------------|----------|---------|-----|------|------|
|                             |          | Min     | Typ | Max  |      |
| Supply Voltage              | $V_{DD}$ | 3.0     | 3.3 | 3.6  | V    |
| Operating Temperature Range | Topr     | -20     | -   | 85   | °C   |
| Dual-in/Dual-out            | Fin      | 20      | -   | 135  | MHz  |
|                             | Fout     | 20      | -   | 135  | MHz  |
| Distribution                | Fin      | 20      | -   | 135  | MHz  |
|                             | Fout     | 20      | -   | 135  | MHz  |
| Single-in / Dual-out        | Fin      | 40      | -   | 135  | MHz  |
|                             | Fout     | 20      | -   | 62.5 | MHz  |
| Dual-in / Single-out        | Fin      | 20      | -   | 62.5 | MHz  |
|                             | Fout     | 40      | -   | 135  | MHz  |

●Block Diagram

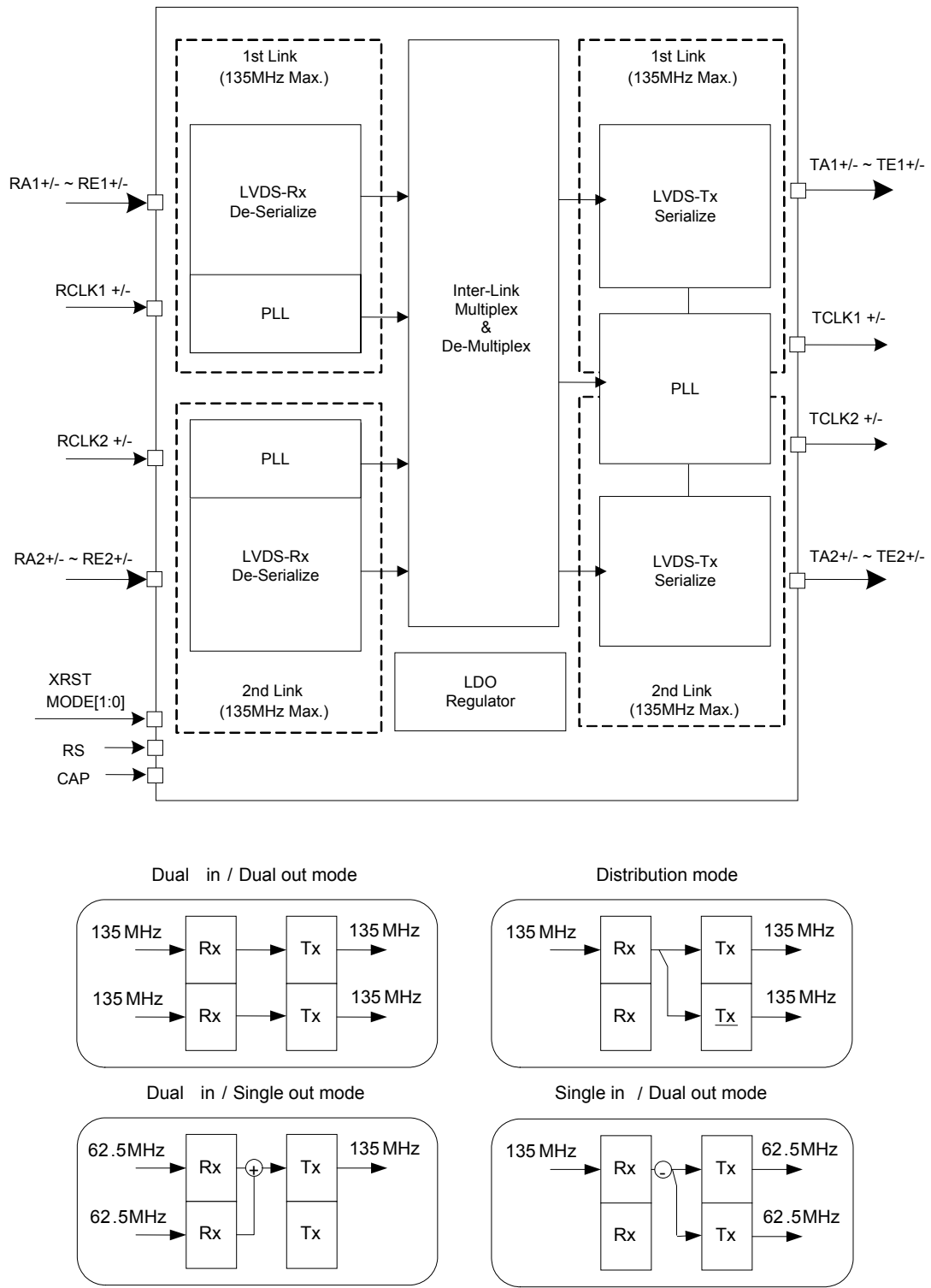


Fig.1 Block Diagram

●Pin Configuration

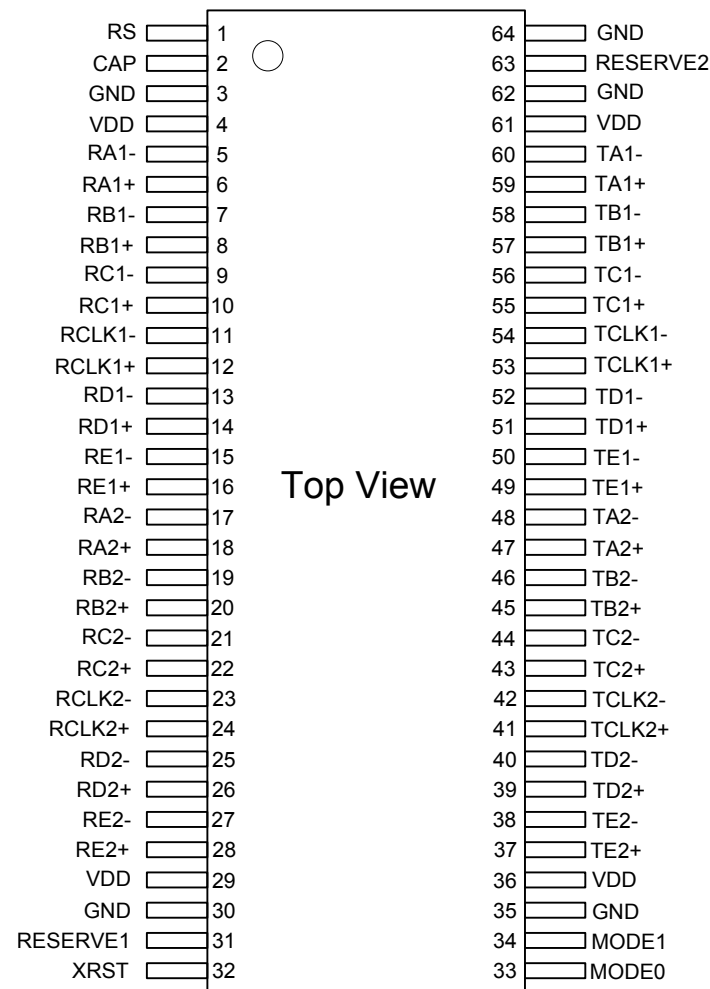


Fig.2 Pin Configuration (Top View)

## ●Pin Description

| Pin Name       | Pin No.       | Type   |          | Descriptions                 |                                                                                                                                 |       |                         |                         |
|----------------|---------------|--------|----------|------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-------|-------------------------|-------------------------|
| RA1+/-         | 5,6           | Input  | LVDS     | Link1 chA LVDS data input    |                                                                                                                                 |       |                         |                         |
| RB1+/-         | 7,8           |        |          | Link1 chB LVDS data input    |                                                                                                                                 |       |                         |                         |
| RC1+/-         | 9,10          |        |          | Link1 chC LVDS data input    |                                                                                                                                 |       |                         |                         |
| RD1+/-         | 13,14         |        |          | Link1 chD LVDS data input    |                                                                                                                                 |       |                         |                         |
| RE1+/-         | 15,16         |        |          | Link1 chE LVDS data input    |                                                                                                                                 |       |                         |                         |
| RCLK1+/-       | 11,12         |        |          | Link1 LVDS clock input       |                                                                                                                                 |       |                         |                         |
| RA2+/-         | 17,18         |        |          | Link2 chA LVDS data input    |                                                                                                                                 |       |                         |                         |
| RB2+/-         | 19,20         |        |          | Link2 chB LVDS data input    |                                                                                                                                 |       |                         |                         |
| RC2+/-         | 21,22         |        |          | Link2 chC LVDS data input    |                                                                                                                                 |       |                         |                         |
| RD2+/-         | 25,26         |        |          | Link2 chD LVDS data input    |                                                                                                                                 |       |                         |                         |
| RE2+/-         | 27,28         |        |          | Link2 chE LVDS data input    |                                                                                                                                 |       |                         |                         |
| RCLK2+/-       | 23,24         |        |          | Link2 LVDS clock input       |                                                                                                                                 |       |                         |                         |
| TA1+/-         | 59,60         | Output |          | LVDS                         | Link1 chA LVDS data output                                                                                                      |       |                         |                         |
| TB1+/-         | 57,58         |        |          |                              | Link1 chB LVDS data output                                                                                                      |       |                         |                         |
| TC1+/-         | 55,56         |        |          |                              | Link1 chC LVDS data output                                                                                                      |       |                         |                         |
| TD1+/-         | 51,52         |        |          |                              | Link1 chD LVDS data output                                                                                                      |       |                         |                         |
| TE1+/-         | 49,50         |        |          |                              | Link1 chE LVDS data output                                                                                                      |       |                         |                         |
| TCLK1+/-       | 53,54         |        |          |                              | Link1 LVDS clock output                                                                                                         |       |                         |                         |
| TA2+/-         | 47,48         |        |          |                              | Link2 chA LVDS data output                                                                                                      |       |                         |                         |
| TB2+/-         | 45,46         |        |          |                              | Link2 chB LVDS data output                                                                                                      |       |                         |                         |
| TC2+/-         | 43,44         |        |          |                              | Link2 chC LVDS data output                                                                                                      |       |                         |                         |
| TD2+/-         | 39,40         |        |          |                              | Link2 chD LVDS data output                                                                                                      |       |                         |                         |
| TE2+/-         | 37,38         |        |          |                              | Link2 chE LVDS data output                                                                                                      |       |                         |                         |
| TCLK2+/-       | 41,42         |        |          |                              | Link2 LVDS clock output                                                                                                         |       |                         |                         |
| XRST           | 32            | Input  | CMOS     |                              | Power Down<br>H : Normal operation<br>L : Power down (all outputs are Hi-Z)                                                     |       |                         |                         |
| RS             | 1             | Input  |          |                              | LVDS swing level select<br>H : TYP=350mV<br>L : TYP=200mV                                                                       |       |                         |                         |
| MODE1<br>MODE0 | 33,34         | Input  |          |                              | Pixel data mdoe                                                                                                                 |       |                         |                         |
|                |               |        |          |                              | MODE1                                                                                                                           | MODE0 | RCLK2/-                 | Description             |
|                |               |        |          |                              | L                                                                                                                               | L     | clkin                   | Dual-in/Dual-out mode   |
|                |               |        |          |                              | L                                                                                                                               | L     | Hi-z                    | Distribution mode       |
|                |               |        |          |                              | H                                                                                                                               | L     | Hi-z                    | Single-in/Dual-out mode |
|                |               |        | L        |                              | H                                                                                                                               | clkin | Dual-in/Single-out mode |                         |
| H              | H             | -      | Reserved |                              |                                                                                                                                 |       |                         |                         |
| VDD            | 4,29,36,61    | -      | -        |                              | Power supply pins.                                                                                                              |       |                         |                         |
| GND            | 3,30,35,62,64 | -      |          |                              | Ground pins                                                                                                                     |       |                         |                         |
| CAP            | 2             | -      |          |                              | Decoupling capacitor pin<br>This pin should be connected to external decoupling capacitor.<br>Recommended capacitor is 2.2μF.*1 |       |                         |                         |
| RESERVE1/2     | 31,63         | Input  | -        | Reserve pins<br>Must be open |                                                                                                                                 |       |                         |                         |

\*1. Parts list of recommended external decoupling capacitor

| Maker   | Parts Number       | Size<br>[mm] | Capacity<br>[μF] | Capacitance<br>Tolerance<br>[%] | Temperature<br>Characteristics | Reference<br>Temperature<br>[°C] | Capacitance<br>Change<br>[%] | Operating<br>Temperature<br>Range<br>[°C] | Voltage<br>[V] |
|---------|--------------------|--------------|------------------|---------------------------------|--------------------------------|----------------------------------|------------------------------|-------------------------------------------|----------------|
| Murata  | GRM155B30G225ME15D | 1.0x0.5x0.5  | 2.2              | ±20                             | B                              | 20                               | ±10%                         | -25~85                                    | 4.0            |
| Murata  | GRM155R60J225ME15D | 1.0x0.5x0.5  | 2.2              | ±20                             | X5R                            | 25                               | ±15%                         | -55~85                                    | 6.3            |
| TDK     | C1005X7R1H222KT    | 1.0x0.5x0.5  | 2.2              | ±20                             | X7R                            | 25                               | ±15%                         | -55~125                                   | 5.0            |
| Kyocera | CM05X5R225K04AH    | 1.0x0.5x0.5  | 2.2              | ±20                             | X5R                            | 25                               | ±15%                         | -55~85                                    | 4.0            |
| Kyocera | CM05X5R225M04AH    | 1.0x0.5x0.5  | 2.2              | ±20                             | X5R                            | 25                               | ±15%                         | -55~85                                    | 4.0            |

# ●DC Characteristics

 Table 1 : LVCMOS DC Characteristics( $V_{DD}=3.0V\sim 3.6V$ ,  $T_a=-20^{\circ}C\sim +85^{\circ}C$ )

| Parameter                | Symbol    | Limits             |     |                    | Unit       | Conditions                   |
|--------------------------|-----------|--------------------|-----|--------------------|------------|------------------------------|
|                          |           | Min                | Typ | Max                |            |                              |
| High Level Input Voltage | $V_{IH}$  | $V_{DD}\times 0.8$ | -   | $V_{DD}$           | V          | -                            |
| Low Level Input Voltage  | $V_{IL}$  | GND                | -   | $V_{DD}\times 0.2$ | V          | -                            |
| Input Leak Current       | $I_{INC}$ | -10                | -   | +10                | $\mu A$    | $0V \leq V_{IN} \leq V_{DD}$ |
| Pull-down resistor       | $P_{DR}$  | 20                 | 46  | 100                | K $\Omega$ | -                            |

 Table 2 : LVDS Receiver DC Characteristics( $V_{DD}=3.0V\sim 3.6V$ ,  $T_a=-20^{\circ}C\sim +85^{\circ}C$ )

| Parameter                         | Symbol         | Limits |     |      | Unit    | Conditions        |
|-----------------------------------|----------------|--------|-----|------|---------|-------------------|
|                                   |                | Min    | Typ | Max  |         |                   |
| LVDS-Rx Input Voltage             | $V_{IN\_RX}$   | 0.4    | -   | 2.1  | V       | -                 |
| LVDS-Rx Common Voltage            | $V_{IC\_RX}$   | 0.7    | 1.2 | 1.8  | V       | -                 |
| Differential Input High Threshold | $V_{TH\_RX}$   | -      | -   | +100 | mV      | $V_{IC\_RX}=1.2V$ |
| Differential Input Low Threshold  | $V_{TL\_RX}$   | -100   | -   | -    | mV      | $V_{IC\_RX}=1.2V$ |
| LVDS-Rx Differential Voltage      | $ V_{ID\_RX} $ | 100    | -   | 600  | mV      | -                 |
| LVDS-Rx Input Current             | $V_{IN\_RX}$   | -20    | -   | 20   | $\mu A$ | -                 |

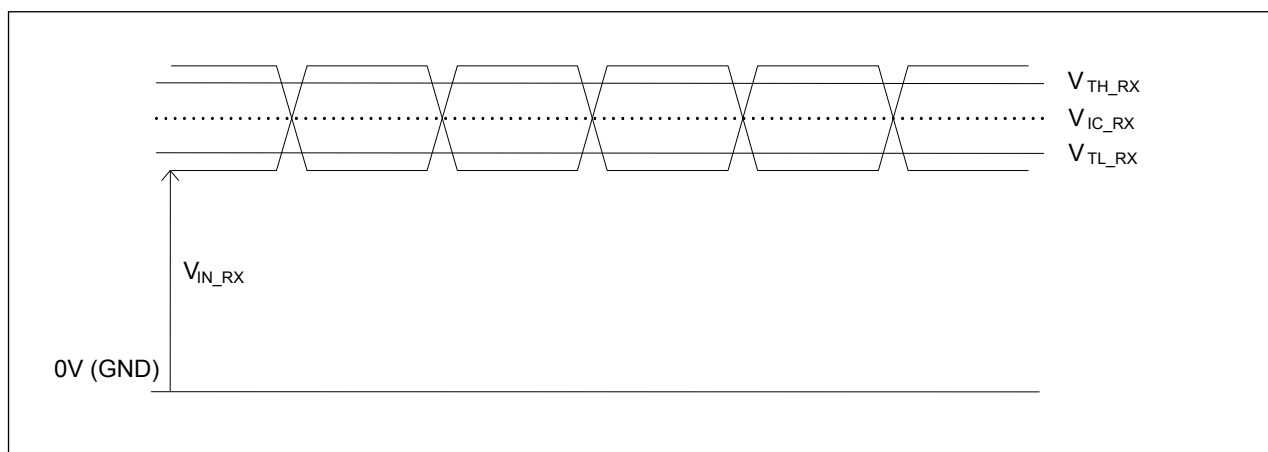


Fig.3 LVDS Receiver DC Characteristics

Table 3 : LVDS Transmitter DC Characteristics ( $V_{DD}=3.0V \sim 3.6V$ ,  $T_a=-20^{\circ}C \sim +85^{\circ}C$ )

| Parameter                                              | Symbol          | Limits |      |       | Unit    | Conditions                              |                              |
|--------------------------------------------------------|-----------------|--------|------|-------|---------|-----------------------------------------|------------------------------|
|                                                        |                 | Min    | Typ  | Max   |         |                                         |                              |
| Differential Output Voltage                            | $V_{OD}$        | 250    | 350  | 450   | mV      | $R_L=100\Omega$                         | Normal swing<br>$R_S=V_{DD}$ |
|                                                        |                 | 100    | 200  | 300   | mV      |                                         | Reduced swing<br>$R_S=GND$   |
| Change in $V_{OD}$ between complementary output states | $\Delta V_{OD}$ | -      | -    | 35    | mV      | $R_L=100\Omega$                         |                              |
| Common Voltage                                         | $V_{OC}$        | 1.125  | 1.25 | 1.375 | V       |                                         |                              |
| Change in $V_{OC}$ between complementary output states | $\Delta V_{OC}$ | -      | -    | 35    | mV      |                                         |                              |
| Output Short Circuit Current                           | $I_{OS}$        | -60    | -    | -     | mA      | $V_{OUT}=0V$                            |                              |
| Output Tri-state Current                               | $I_{OZ}$        | -10    | -    | +10   | $\mu A$ | $XRST=0V$ ,<br>$V_{OUT}=0V$ to $V_{DD}$ |                              |

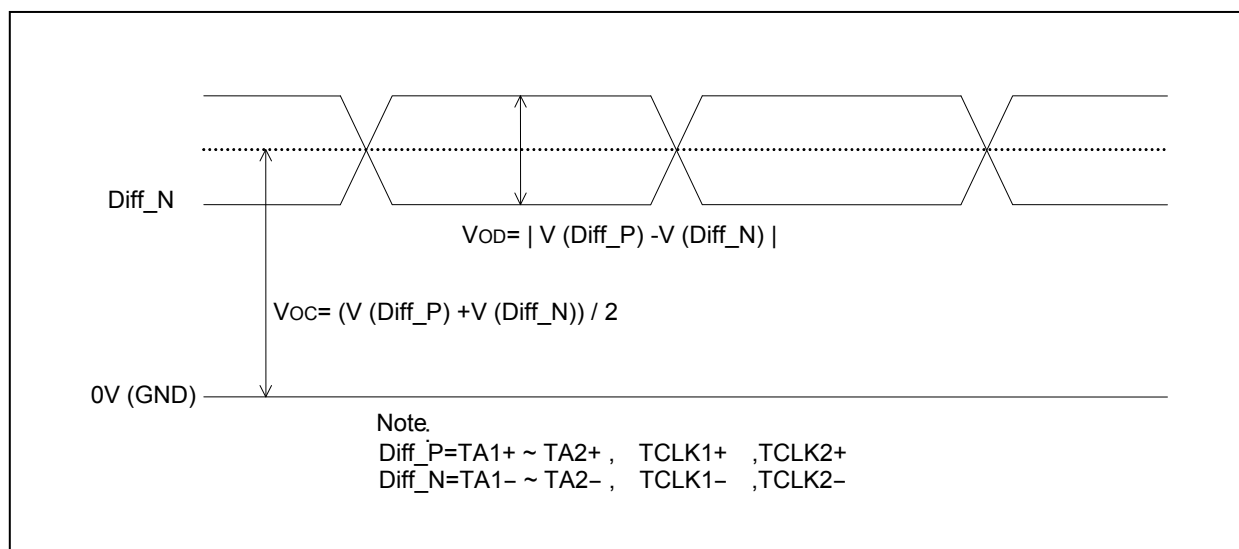


Fig.4 LVDS Transmitter DC Characteristics

# ●AC Characteristics

Table 4 : Switching Characteristics(VDD=3.3V, Ta=25°C)

| Parameter                         |                    | Symbol     | Limits         |                                    |               | Unit |
|-----------------------------------|--------------------|------------|----------------|------------------------------------|---------------|------|
|                                   |                    |            | Min            | Typ                                | Max           |      |
| Skew Time between RCLK1 and RCLK2 |                    | $t_{CK12}$ | $-0.3 t_{RCP}$ | -                                  | $0.3 t_{RCP}$ | ns   |
| Phase Lock Loop Set Time          |                    | $t_{LT}$   | -              | -                                  | 10            | ms   |
| Data Latency                      | dual-in/dual-out   | $t_{RIP6}$ | -              | $4t_{RCP}+5$                       | -             | ns   |
|                                   | distribution       |            | -              | $4t_{RCP}+5$                       | -             | ns   |
|                                   | single-in/dual-out |            | -              | $6t_{RCP}+5$                       | -             | ns   |
|                                   | dual-in/single-out |            | -              | $2.5t_{RCP}+5$                     | -             | ns   |
| DE Input High Time                |                    | $t_{DEH}$  | $2 t_{RCP}$    | -                                  | -             | ns   |
| DE Input Low Time                 |                    | $t_{DEL}$  | $2 t_{RCP}$    | -                                  | -             | ns   |
| DE Input Period                   |                    | $t_{DEL}$  | $4 t_{RCP}$    | Must be $2nt_{RCP}$<br>(n=integer) | -             | ns   |

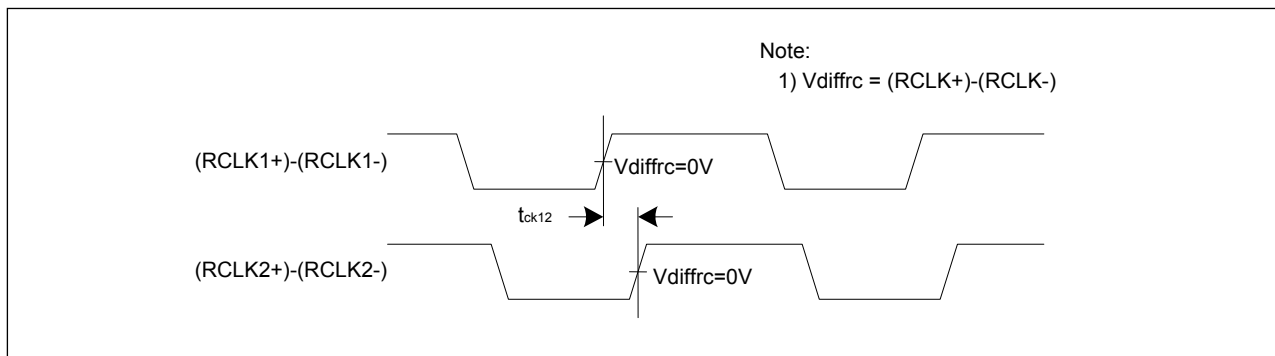


Fig.5 Skew Time between RCLK1 and RCLK2

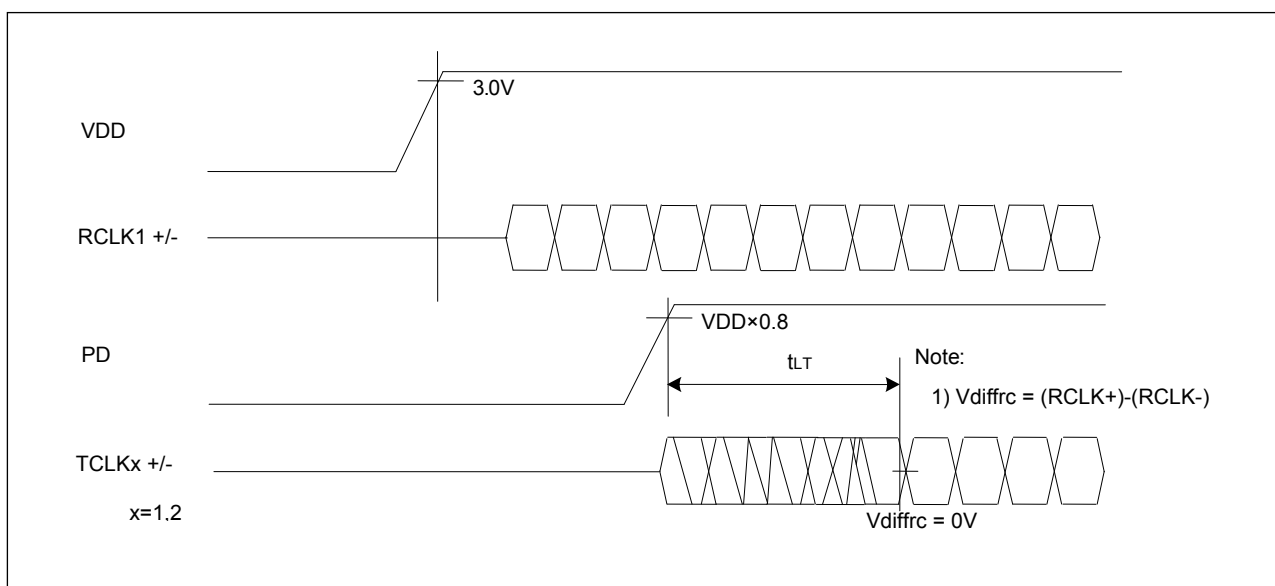


Fig.6 Phase Lock Loop Set Time

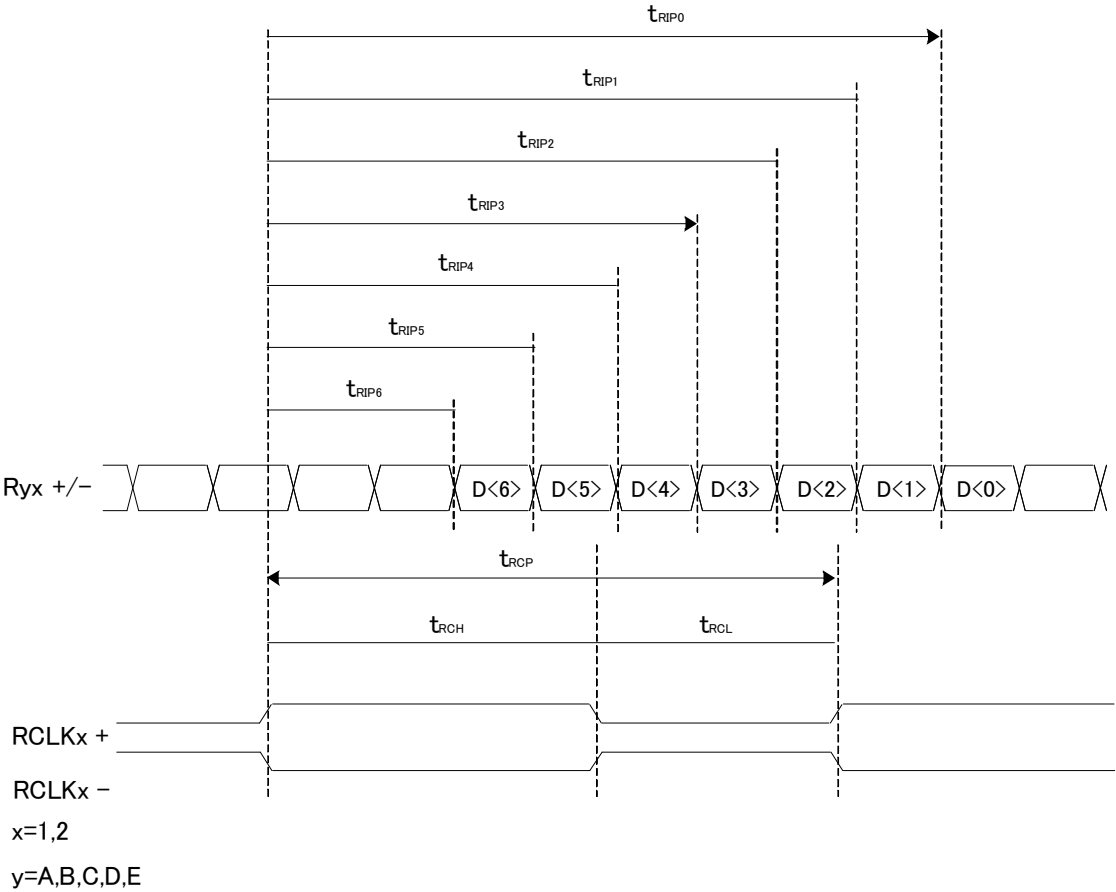


## ●LVDS Receiver AC Characteristics

Table 5 : Switching Characteristics(VDD=3.3V, Ta=25°C)

| Parameter                            |               | Symbol     | Limits                           |                       |                                  | Unit |
|--------------------------------------|---------------|------------|----------------------------------|-----------------------|----------------------------------|------|
|                                      |               |            | Min                              | Typ                   | Max                              |      |
| Input Clock Period                   | dual /dual    | $t_{RCP}$  | 7.4                              | -                     | 50                               | ns   |
|                                      | distribution  |            | 7.4                              | -                     | 50                               | ns   |
|                                      | single/dual   |            | 7.4                              | -                     | 25                               | ns   |
|                                      | dual/single   |            | 16                               | -                     | 50                               | ns   |
| Differential Input Data Setup Margin | CLKIN= 75MHz  | $t_{RSUP}$ | 480                              | -                     | -                                | ps   |
|                                      | CLKIN= 112MHz |            | 250                              | -                     | -                                | ps   |
|                                      | CLKIN= 135MHz |            | 220                              | -                     | -                                | ps   |
| Differential Input Data Hold Margin  | CLKIN= 75MHz  | $t_{RHLD}$ | 480                              | -                     | -                                | ps   |
|                                      | CLKIN= 112MHz |            | 250                              | -                     | -                                | ps   |
|                                      | CLKIN= 135MHz |            | 220                              | -                     | -                                | ps   |
| Differential Input Data Position 6   |               | $t_{RIP6}$ | $2 \frac{t_{RCP}}{7} - t_{RHLD}$ | $2 \frac{t_{RCP}}{7}$ | $2 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |
| Differential Input Data Position 5   |               | $t_{RIP5}$ | $3 \frac{t_{RCP}}{7} - t_{RHLD}$ | $3 \frac{t_{RCP}}{7}$ | $3 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |
| Differential Input Data Position 4   |               | $t_{RIP4}$ | $4 \frac{t_{RCP}}{7} - t_{RHLD}$ | $4 \frac{t_{RCP}}{7}$ | $4 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |
| Differential Input Data Position 3   |               | $t_{TOP3}$ | $5 \frac{t_{RCP}}{7} - t_{RHLD}$ | $5 \frac{t_{RCP}}{7}$ | $5 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |
| Differential Input Data Position 2   |               | $t_{RIP2}$ | $6 \frac{t_{RCP}}{7} - t_{RHLD}$ | $6 \frac{t_{RCP}}{7}$ | $6 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |
| Differential Input Data Position 1   |               | $t_{RIP1}$ | $7 \frac{t_{RCP}}{7} - t_{RHLD}$ | $7 \frac{t_{RCP}}{7}$ | $7 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |
| Differential Input Data Position 0   |               | $t_{RIP0}$ | $8 \frac{t_{RCP}}{7} - t_{RHLD}$ | $8 \frac{t_{RCP}}{7}$ | $8 \frac{t_{RCP}}{7} + t_{RSUP}$ | ns   |

●AC Timing Diagram



Ry1 +/- skew margin is the one between RCLK1 +/- and Ry1 +/-  
Ry2 +/- skew margin is the one between RCLK2 +/- and Ry2 +/-

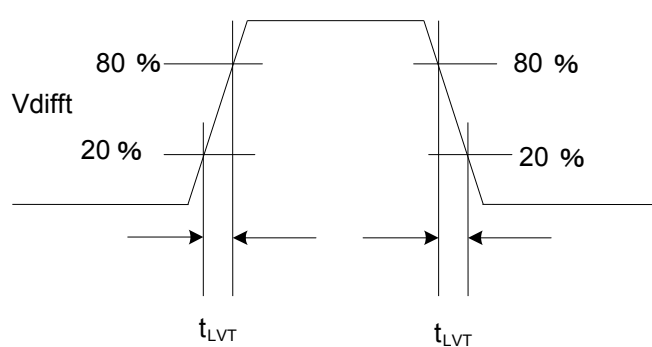
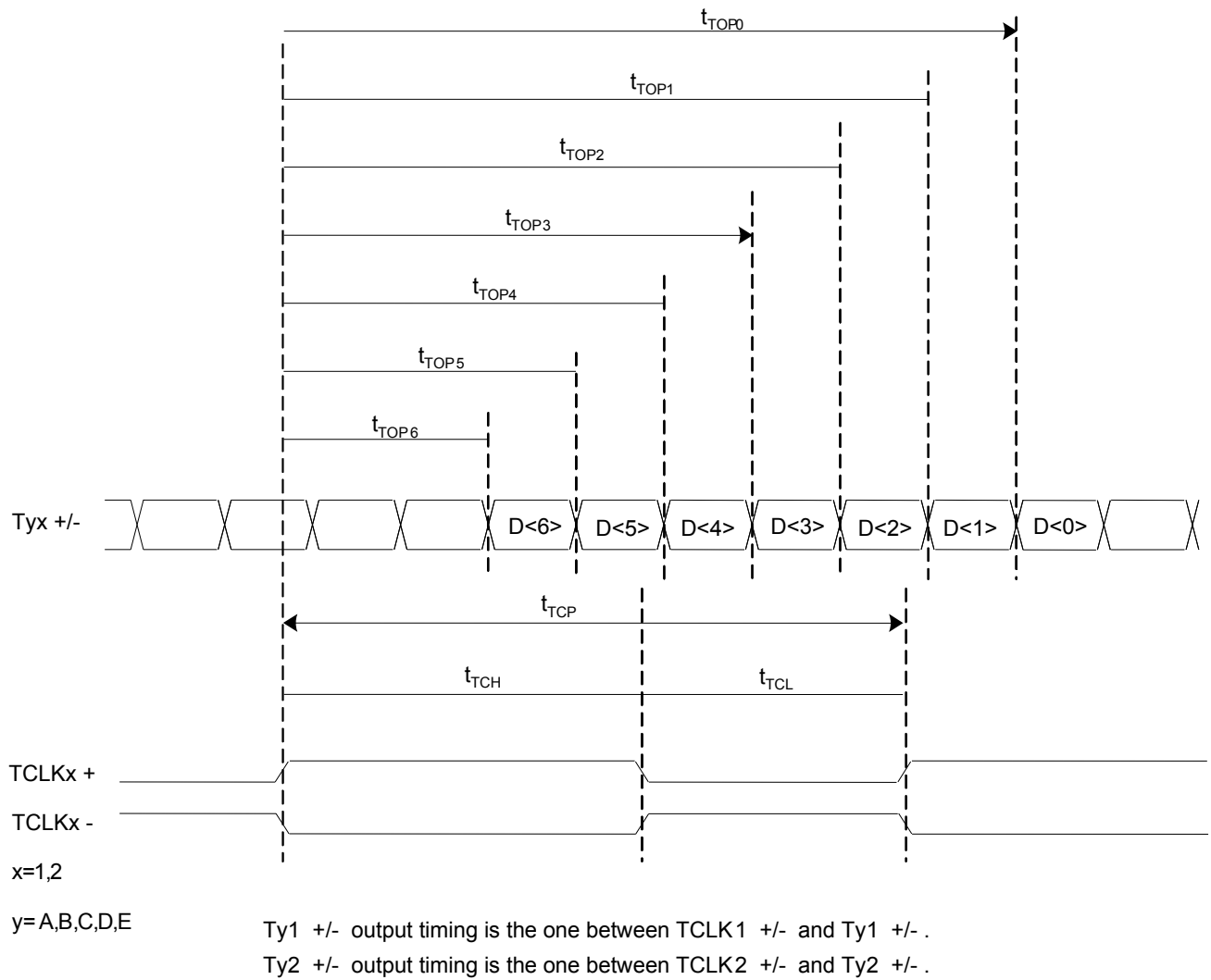
Fig.7 AC Timing Diagram (1)

## ●LVDS Transmitter AC Characteristics

Table 6 : Switching Characteristics(VDD=3.3V, Ta=25°C)

| Parameter                           |               | Symbol     | Limits                           |                       |                                  | Unit |
|-------------------------------------|---------------|------------|----------------------------------|-----------------------|----------------------------------|------|
|                                     |               |            | Min                              | Typ                   | Max                              |      |
| Output Clock Period                 | dual /dual    | $t_{TCP}$  | 7.4                              | -                     | 50                               | ns   |
|                                     | distribution  |            | 7.4                              | -                     | 50                               | ns   |
|                                     | single/dual   |            | 16                               | -                     | 50                               | ns   |
|                                     | dual/single   |            | 7.4                              | -                     | 25                               | ns   |
| Differential Output Transition Time |               | $t_{LVT}$  | -                                | 0.6                   | 1.5                              | ns   |
| Differential Output Setup Time      | CLKOUT=75MHz  | $T_{TSUP}$ | -                                | -                     | 250                              | ps   |
|                                     | CLKOUT=112MHz |            | -                                | -                     | 200                              | ps   |
|                                     | CLKOUT=135MHz |            | -                                | -                     | 170                              | ps   |
| Differential Output Hold Time       | CLKOUT=75MHz  | $T_{THLD}$ | -                                | -                     | 250                              | ps   |
|                                     | CLKOUT=112MHz |            | -                                | -                     | 200                              | ps   |
|                                     | CLKOUT=135MHz |            | -                                | -                     | 170                              | ps   |
| Differential Output Position 6      |               | $t_{TOP6}$ | $2 \frac{t_{TCP}}{7} - T_{THLD}$ | $2 \frac{t_{TCP}}{7}$ | $2 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |
| Differential Output Position 5      |               | $t_{TOP5}$ | $3 \frac{t_{TCP}}{7} - T_{THLD}$ | $3 \frac{t_{TCP}}{7}$ | $3 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |
| Differential Output Position 4      |               | $t_{TOP4}$ | $4 \frac{t_{TCP}}{7} - T_{THLD}$ | $4 \frac{t_{TCP}}{7}$ | $4 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |
| Differential Output Position 3      |               | $t_{TOP3}$ | $5 \frac{t_{TCP}}{7} - T_{THLD}$ | $5 \frac{t_{TCP}}{7}$ | $5 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |
| Differential Output Position 2      |               | $t_{TOP2}$ | $6 \frac{t_{TCP}}{7} - T_{THLD}$ | $6 \frac{t_{TCP}}{7}$ | $6 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |
| Differential Output Position 1      |               | $t_{TOP1}$ | $7 \frac{t_{TCP}}{7} - T_{THLD}$ | $7 \frac{t_{TCP}}{7}$ | $7 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |
| Differential Output Position 0      |               | $t_{TOP0}$ | $8 \frac{t_{TCP}}{7} - T_{THLD}$ | $8 \frac{t_{TCP}}{7}$ | $8 \frac{t_{TCP}}{7} + T_{TSUP}$ | ns   |

●AC Timing Diagram



Note

1)  $V_{diff} = (Ty+) - (Ty-)$   
 $= A, B, C, CLK, D, E$   
 $y=1,2$

Fig.8 AC Timing Diagram (2)

●LVDS Data Mapping(1)  
Dual-in / Dual-out mode

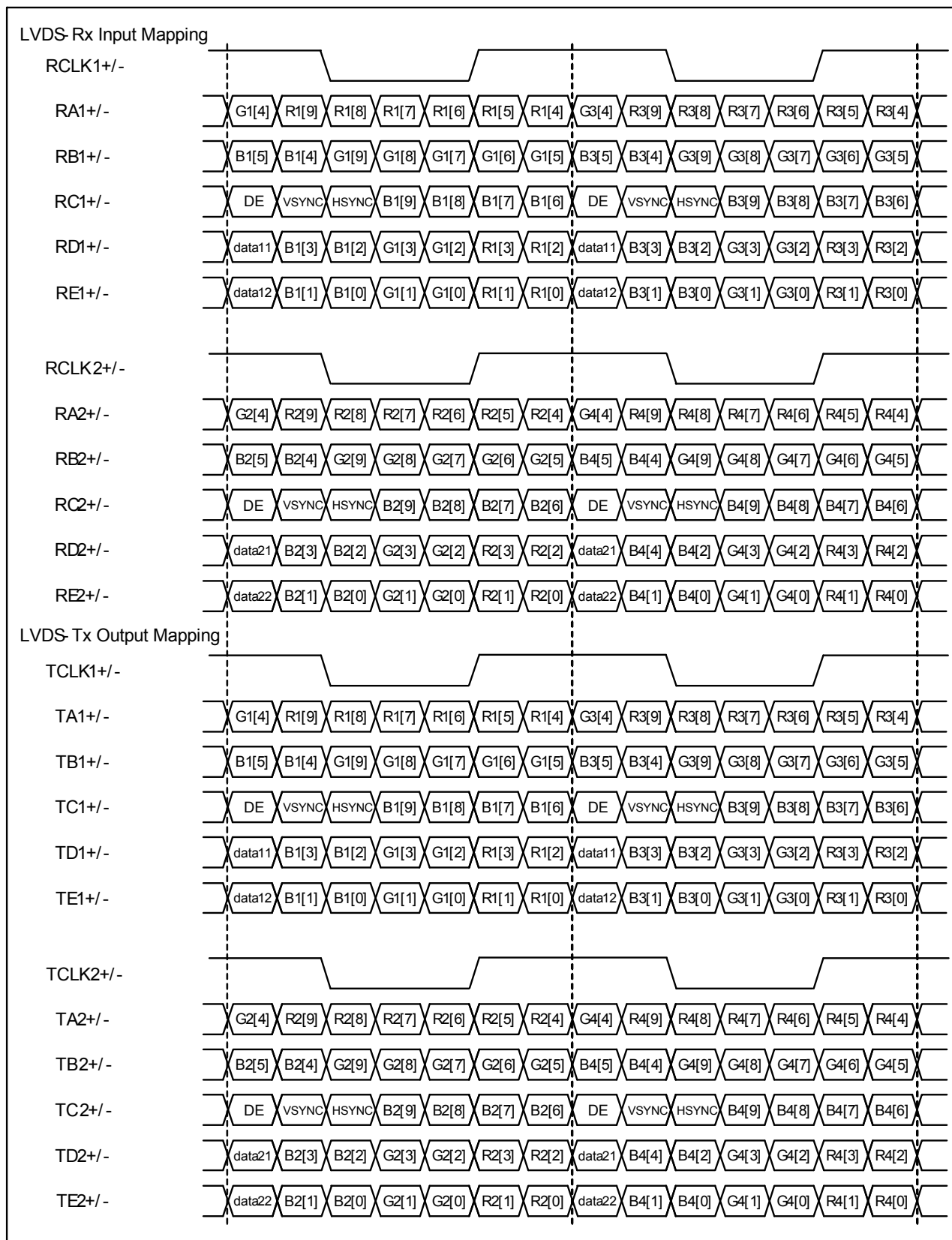


Fig.9 LVDS Data Mapping(1)

# ●LVDS Data Mapping(2)

Distribution Mode

Distribution mode,RCLK2+/- must be High-z.

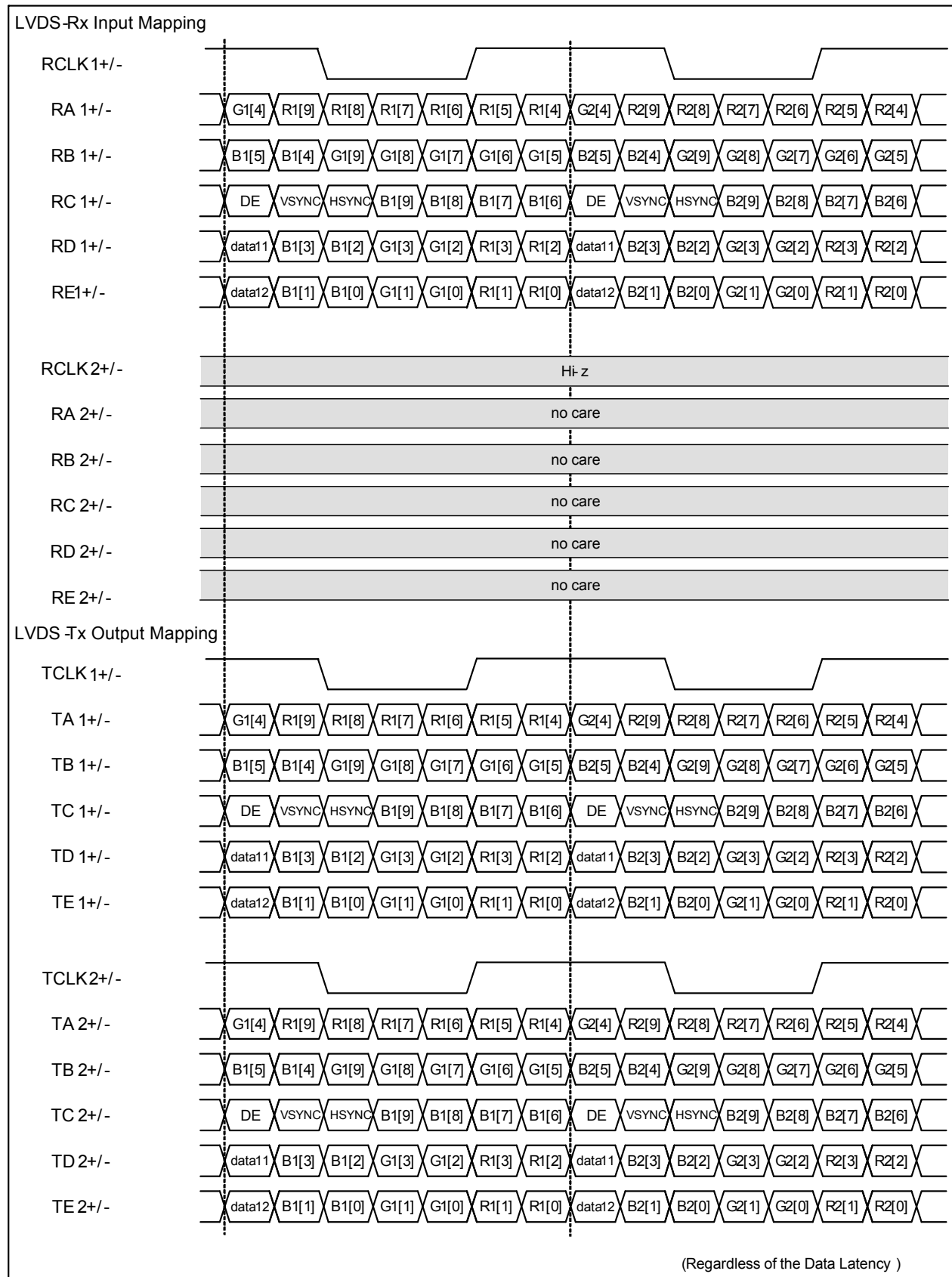


Fig.10 LVDS Data Mapping(2)

### ●LVDS Data Mapping(3)

Single-in / Dual-out mode

Single-in / Dual-out mode, RCLK2+/- must be High-z.

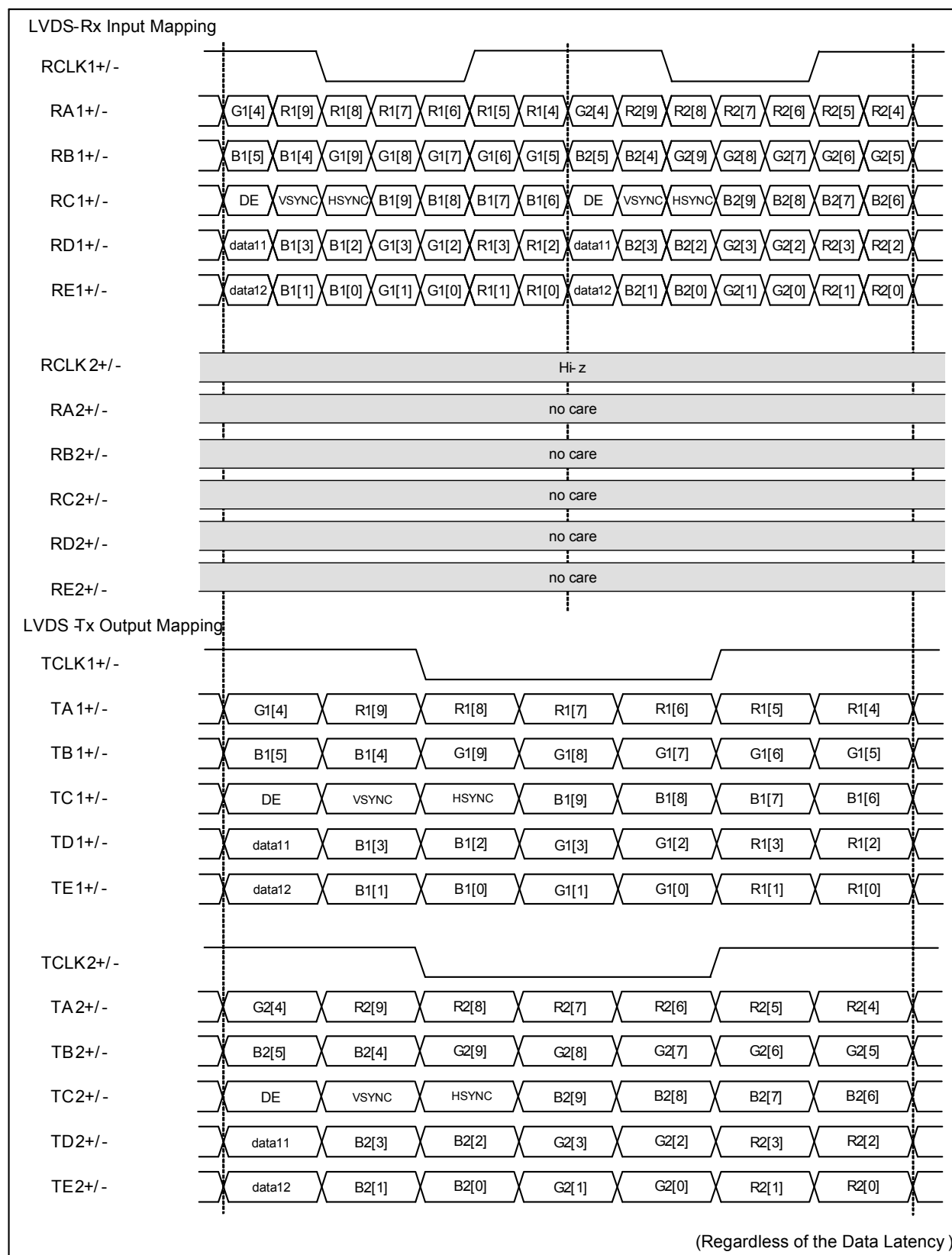


Fig.11 LVDS Data Mapping (3)

# ●LVDS Data Mapping(4)

Dual-in / Single-out mode

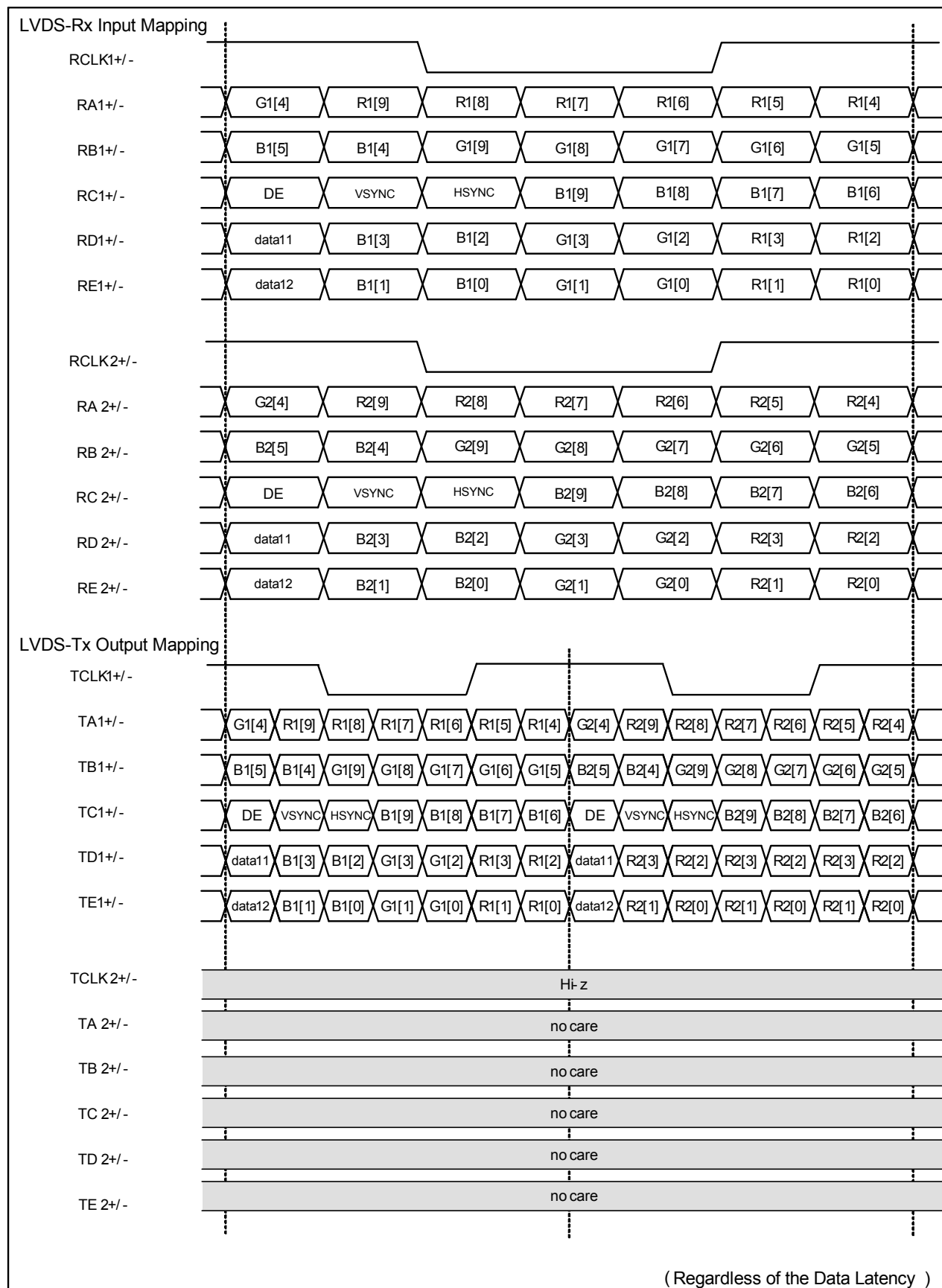


Fig.12 LVDS Data Mapping(4)



●Application Circuit

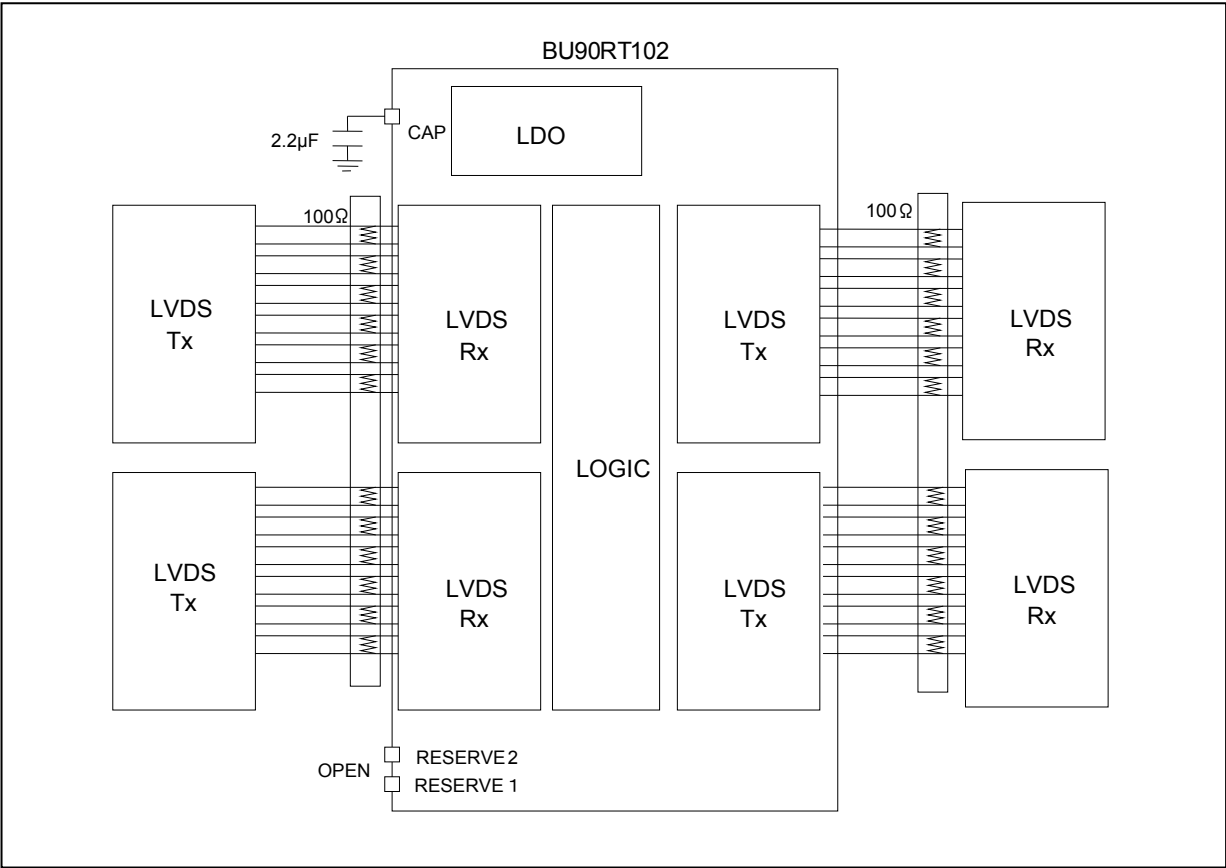


Fig.13 Application circuit example

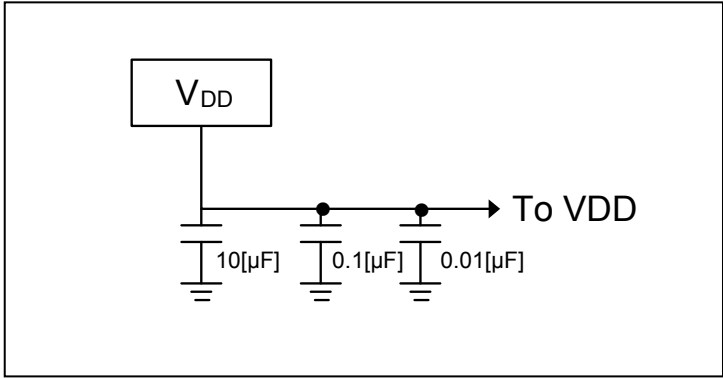
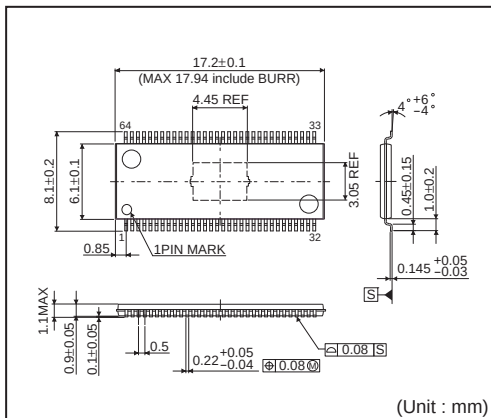


Fig.14 Filtering capacitor of power line

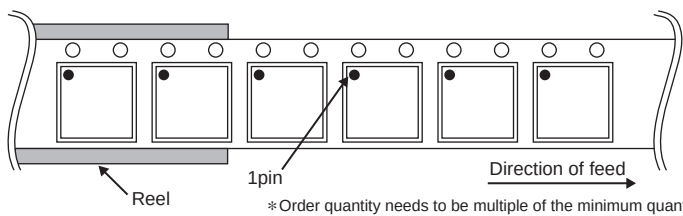
### ●Ordering part number

|          |   |            |   |   |   |   |   |   |   |                                     |   |
|----------|---|------------|---|---|---|---|---|---|---|-------------------------------------|---|
| B        | U | 9          | 0 | R | T | 1 | 0 | 2 | - | E                                   | 2 |
| Part No. |   | Part No.   |   |   |   |   |   |   |   | Packaging and forming specification |   |
|          |   | 90RT102    |   |   |   |   |   |   |   | E2: Embossed tape and reel          |   |
|          |   | Package    |   |   |   |   |   |   |   |                                     |   |
|          |   | HTSSOP-C64 |   |   |   |   |   |   |   |                                     |   |

**HTSSOP-C64**

<Tape and Reel information>

|                   |                                                                                                                                                   |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Tape              | Embossed carrier tape (with dry pack)                                                                                                             |
| Quantity          | 2000pcs                                                                                                                                           |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



## Notes

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