POWER MANAGEMENT SYSTEM DEVICE

RN5T614x

Product Specifications

Rev. 1.0

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Electronic Devices Company

This specification is subject to change without notice.

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1. Outline

RN5T614 is the power management IC for GPS-PND/MID and Smart-Phone.

It integrates three high-efficiency step-down DCDC controllers, eight low dropout regulators, power control logic, Li-ion Battery Charger, I2C-Bus Interface, voltage detections, thermal shut-down, UVLO and etc.

2. Feature

●System
- ✓ Thermal Shutdown Function
- ✓ Reset Detector Function
- ✓ UVLO Function
- ✓ I2C-Bus Interface @400kHz (Input voltage range: 1.7V-3.4V)

●High Efficiency Step-down DC/DC Converters
- ✓ DC/DC1: 1.20V (0.9V to 1.5V/12.5mV steps) @1200mA with RAMP control (For Core)
- ✓ DC/DC2: 1.15V (0.9V to 1.5V/12.5mV steps and 1.8V) @1000mA with RAMP control (For Logic)
- ✓ DC/DC3: 1.8V (1.8V to 3.3V by external resistors) @500mA (For Memory)
- ✓ DC/DC on/off control pin for DC/DC1 and DC/DC2

●Low Drop Voltage Regulators
- ✓ LDO1:3.0V (Always-on) @10mA
- ✓ LDO2:1.2V (0.9V/1.0V/1.1V/1.2V/1.3V) @30mA
- ✓ LDO3:1.2V (0.9V/1.0V/1.1V/1.2V/1.3V) @30mA
- ✓ LDO4:3.3V (1.8V/2.5V/2.6V/2.8V/2.85V/3.0V/3.3V) @300mA
- ✓ LDO5:1.8V (1.8V/2.5V/2.6V/2.8V/2.85V/3.0V/3.3V) @300mA
- ✓ LDO6:2.6V (1.2V/1.8V/2.5V/2.6V/2.8V/2.85V/3.0V/3.3V) @150mA
- ✓ LDO7:3.0V (1.2V/1.8V/2.5V/2.6V/2.8V/2.85V/3.0V/3.3V) @150mA
- ✓ LDO8:3.3V (1.8V/2.5V/2.6V/2.8V/2.85V/3.0V/3.3V) @150mA

●Li-ion Battery Charger
- ✓ Support AC adapter charging
- ✓ With the current limit protection and charge current control, the limited power can be efficiently supplied to the system and the battery.
- ✓ The system can power on even when Li-ion Battery is low voltage or open.
- ✓ The device can withstand up to 6.5V on VCHG pin. However, it can withstand high voltage by combining a high voltage protection IC (up to 28V by using BD6040 of ROHM).
- ✓ Rapid timer and Trickle timer integrated.
- ✓ Monitor for the battery thermistor built in.
- ✓ No external MOSFET required.
- ✓ If system loads over AC adapter current rating, the battery will supply the current to the system.
- ✓ Chip temperature detection circuit for over temperature protection integrated.

●Package QFN0606-48

●Process CMOS

◎Version List

Version No	DC/DC Preset	LDO Setting	DCDCEN* Valid Condition	Sequence
RN5T614A	DC/DC1: 1.25V DC/DC2: 1.20V	LDO1: 3.0V LDO2: Power-on LDO3-5: Initial On LDO5: 3.0V LDO8: 3.0V VREF: Power-on	DCDCEN12 : 2ms after the start of power-on DCDCEN3 : Invalid by trimming	Sequence1
RN5T614B	DC/DC1: 1.25V DC/DC2: 1.20V	LDO1: 3.0V LDO2: Power-on LDO3-5: Initial On LDO5: 3.0V LDO8: 3.0V VREF: Power-on	DCDCEN12 : After RESETO is released DCDCEN3 : Invalid by trimming	Sequence2
RN5T614C	DC/DC1: 1.20V DC/DC2: 1.80V	LDO1: 3.0V LDO2: Power-on LDO3-5: Initial On LDO5: 1.8V LDO8: 3.3V VREF: Power-on	DCDCEN12 : After RESETO is released DCDCEN3 : Invalid by trimming	Sequence2
RN5T614D	DC/DC1: 1.20V DC/DC2: 1.80V	LDO1: 1.8V LDO2: Always-on LDO3-5: Initial Off LDO5: 1.8V LDO8: 3.3V VREF: Always-on	DCDCEN12 : After RESETO is released DCDCEN3 : After RESETO is released	Sequence4
RN5T614E	DC/DC1: 1.20V DC/DC2: 1.15V	LDO1: 3.0V LDO2: Power-on LDO3-5: Initial On LDO5: 1.8V LDO8: 3.3V VREF: Power-on	DCDCEN12 : After RESETO is released DCDCEN3 : Invalid by trimming	Sequence2
RN5T614F	DC/DC1: 1.25V DC/DC2: 1.20V	LDO1: 3.0V LDO2: Power-on LDO3-5: Initial On LDO5: 3.0V LDO8: 3.3V VREF: Power-on	DCDCEN12 : After RESETO is released DCDCEN3 : Invalid by trimming	Sequence3

Note*: For the trimming of regulators, refer to Chapter 8.1 Regulator Table.
For the detail of Sequence, refer to Appendix.

The initial value of the following pages is based on RN5T614E!!

3. Pin Configuration

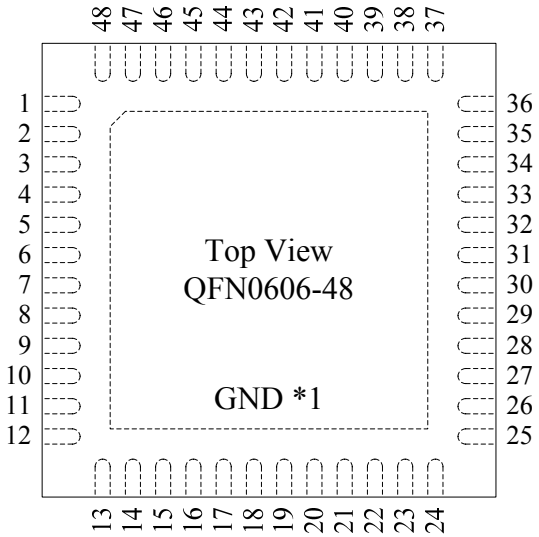
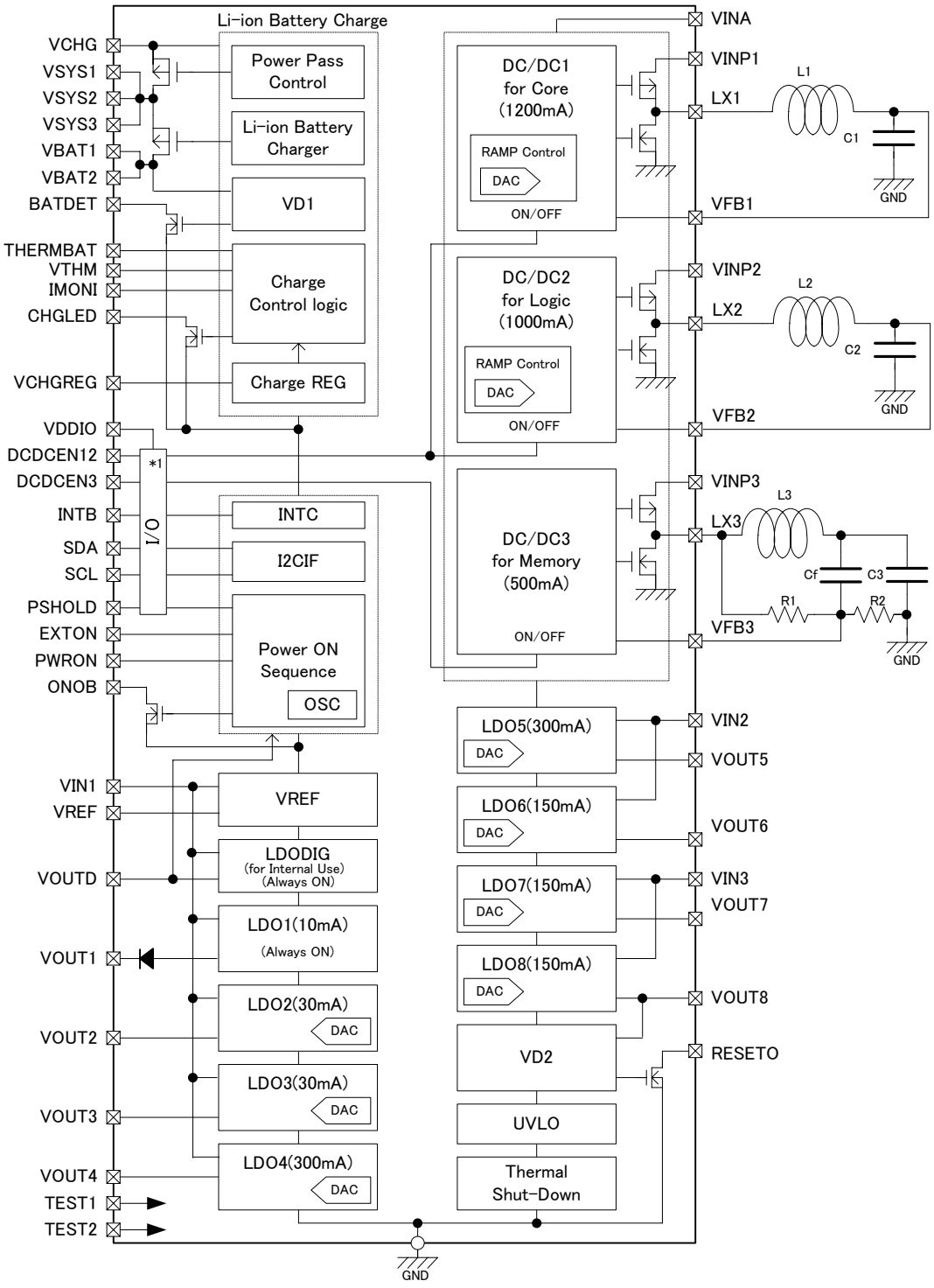


Fig 3-1 Package Information (QFN0606-48pin)

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
1	VOUT5	13	TEST1	25	DCDCEN12	37	VSYS1
2	VIN2	14	TEST2	26	INTB	38	VSYS2
3	VOUT6	15	VFB1	27	PSHOLD	39	VSYS3
4	VOUT7	16	LX1	28	VDDIO	40	VCHG
5	VIN3	17	VINP1	29	SDA	41	CHGLED
6	VOUT8	18	VINP2	30	SCL	42	VOUTD
7	VINA	19	LX2	31	THERMBAT	43	VREF
8	RESETO	20	VFB2	32	VTHM	44	VOUT3
9	BATDET	21	VINP3	33	VCHGREG	45	VOUT2
10	EXTON	22	LX3	34	IMONI	46	VIN1
11	PWRON	23	VFB3	35	VBAT1	47	VOUT4
12	ONOB	24	DCDCEN3	36	VBAT2	48	VOUT1

Note*1: Tab on the bottom side must be connected to GND.

4. Block Diagram



Note*1 : Input pins become valid after RESETO is released. DCDCEN3 pin is invalid.

Fig 4-1 Block Diagram

5. Pin Description

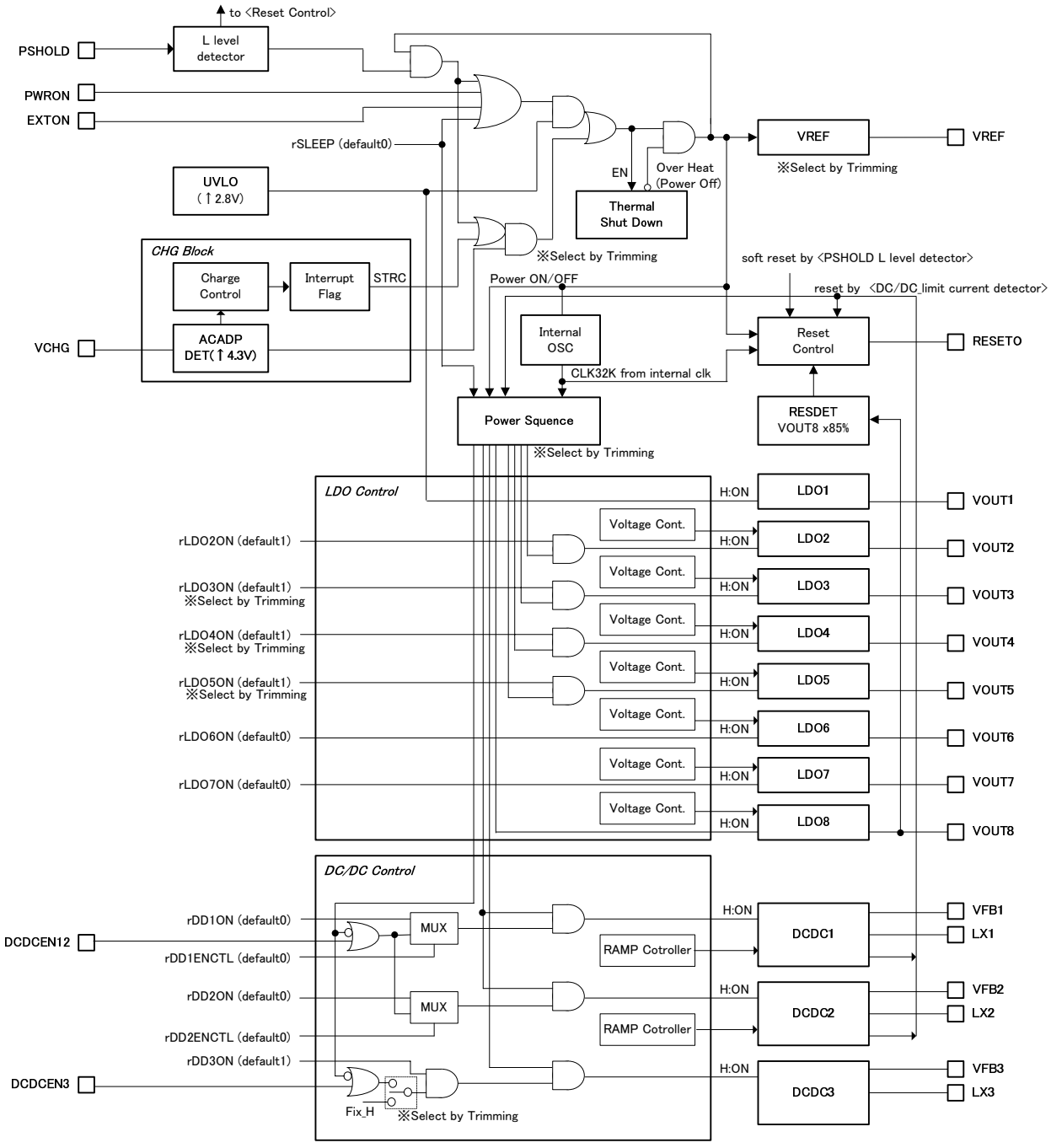
No.	Name	I/O	Function	I/F Level	Notes
1	VOUT5	O	LDO5 output	-	
2	VIN2	PWR	Power supply for LDOs	VIN	
3	VOUT6	O	LDO6 output	-	
4	VOUT7	O	LDO7 output	-	
5	VIN3	PWR	Power supply for LDOs	VIN	
6	VOUT8	O	LDO8 output	-	
7	VINA	PWR	Power supply for DC/DC's Analog Block & Interface IO	VIN	
8	RESETO	O	Reset output. Voltage detection of VOUT8 output	VIN	Nch Open Drain
9	BATDET	O	Battery monitor output	VIN	Nch Open Drain
10	EXTON	I	External power on signal input	VIN	
11	PWRON	I	External power on signal input	VIN	
12	ONOB	O	PWRON monitor. Inverted open-drain output signal of PWRON	VIN	Nch Open Drain
13	TEST1	-	For TEST	-	Connect to GND
14	TEST2	-	For TEST	-	Connect to GND
15	VFB1	I	DC/DC1 Output voltage feedback input	-	
16	LX1	O	DC/DC1 switch output	-	
17	VINP1	PWR	Power supply for DC/DC1	VIN	
18	VINP2	PWR	Power supply for DC/DC2	VIN	
19	LX2	O	DC/DC2 switch output	-	
20	VFB2	I	DC/DC2 Output voltage feedback input	-	
21	VINP3	PWR	Power supply for DC/DC3	VIN	
22	LX3	O	DC/DC3 switch output	-	
23	VFB3	I	DC/DC3 Output voltage feedback input	-	
24	DCDCEN3	I	DC/DC3 ON/OFF input	VDDIO	
25	DCDCEN12	I	DC/DC1,2 ON/OFF input	VDDIO	
26	INTB	O	Interrupt request output	VDDIO	Nch Open Drain
27	PSHOLD	I	Power on maintenance signal input	VDDIO	
28	VDDIO	PWR	Power supply for Interface IO Note*: Supply the power before the point where 2ms after the power-on sequence starts.	VDDIO	
29	SDA	I/O	I2C-Bus Data I/O	VDDIO	Nch Open Drain

No.	Name	I/O	Function	I/F Level	Notes
30	SCL	I	I2C-Bus Clock input	VDDIO	
31	THERMBAT	I	Battery thermistor input	-	
32	VTHM	O	Thermistor temperature detection output & phase compensation	-	
33	VCHGREG	O	Capacitor connection for built-in Regulator	-	Connect only Capacitor load
34	IMONI	O	SW2 current monitor	-	
35	VBAT1	PWR	Li-ion battery input/output1	VBAT	
36	VBAT2	PWR	Li-ion battery input/output2	VBAT	
37	VSYS1	PWR	System power supply1	VSYS	
38	VSYS2	PWR	System power supply2	VSYS	
39	VSYS3	PWR	System power supply3	VSYS	
40	VCHG	PWR	Connected to AC Adapter	VCHG	
41	CHGLED	O	Charge status indicator	VSYS	Nch Open Drain
42	VOUTD	O	Capacitor connection for built-in Regulator	-	Connect only Capacitor load
43	VREF	O	Bypass capacitor connecting pin	-	Connect only Capacitor load
44	VOUT3	O	LDO3 output	-	
45	VOUT2	O	LDO2 output	-	
46	VIN1	PWR	Power supply for LDOs	VIN	
47	VOUT4	O	LDO4 output	-	
48	VOUT1	O	LDO1 output	-	
-	GND	GND	Tab Ground. Tab on the bottom side must be connected to GND.	-	

Table 5-1 Pin Description

6. Power Control

6.1 Power Control Block Diagram



6.2 Power on and off

RN5T614 can be powered on by factors as below.

1. PWRON (external pin)
2. EXTON (external pin)
3. Charging (Shift to Rapid-Charge state)

(a) Power-on by external signal: PWRON (or EXTON) pin

When PWRON pin becomes "H", the power-on sequence starts synchronizing with the internal clock (32 kHz). At the same time, ONOB pin becomes "L".

VREF, DCDC3, LDO2, DCDC1/2, LDO8, LDO5, LDO3, and LDO4 power on following the power-on sequence in the timing chart below. RESETO released 120ms after LDO8 turns on. After RESETO is released, PSHOLD is turned to "H" and the power-on state is maintained while PWRON is "H".

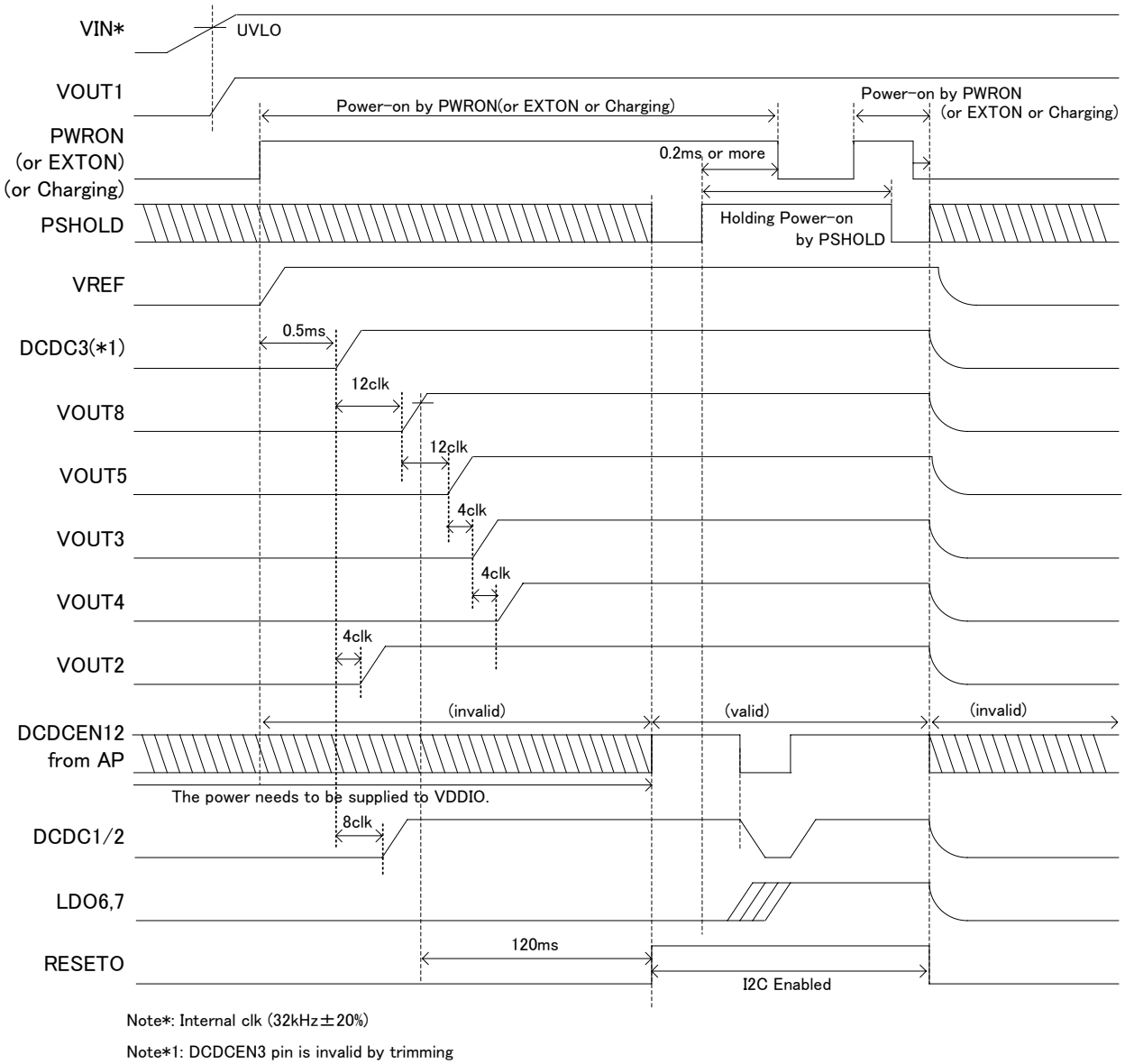
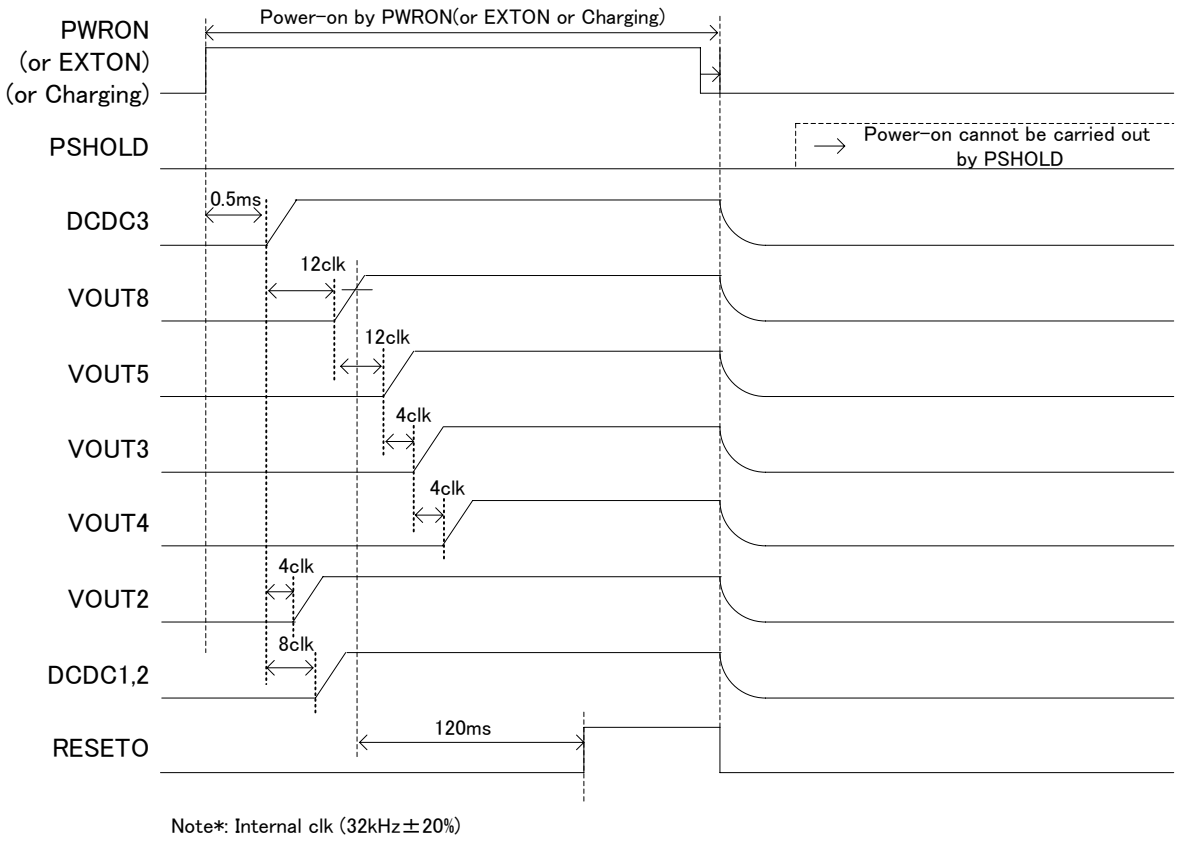


Fig 6-1 Power-on/off Timing (Sequence2)

PSHOLD can only hold PMIC powered-on but cannot turn on at the timing shown below.



(b) Power-off operation

When power-on factor and PSHOLD become "L", all DC/DC and LDO turn off except LDO1 and LDODIG.

6.3 Soft Reset Operation

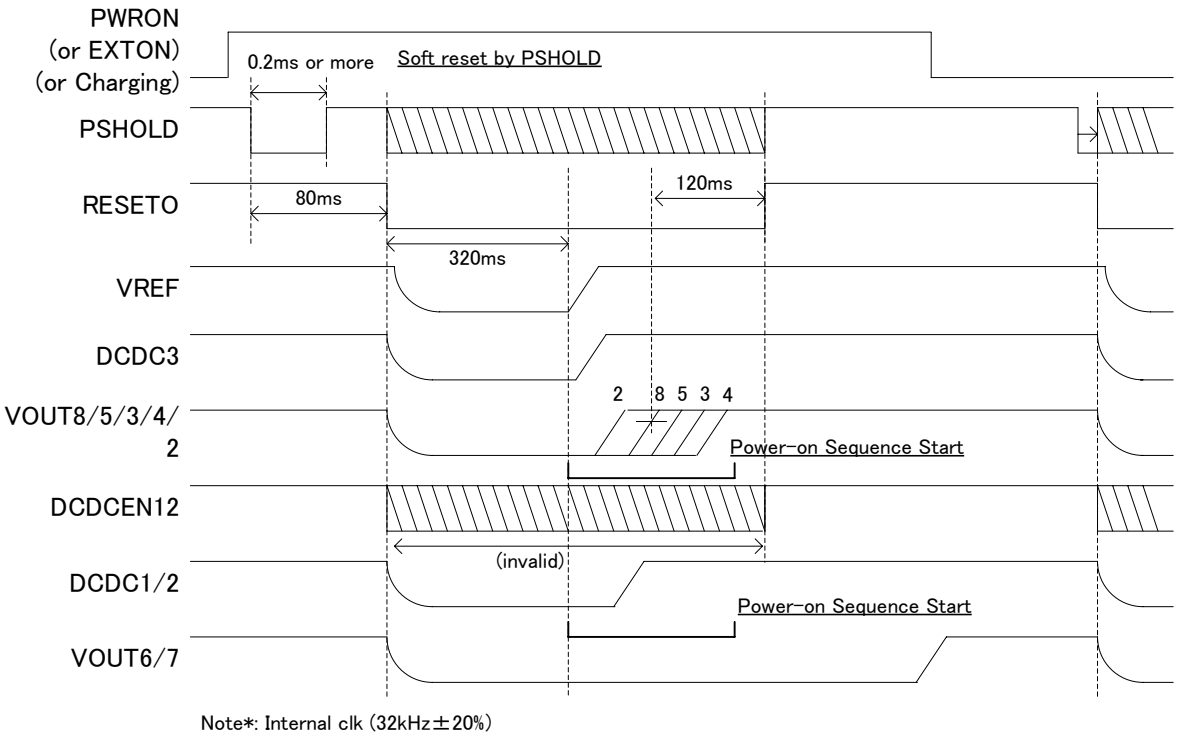


Fig 6-2 Soft Reset Timing

When PWRON becomes “H”, soft reset can be performed by turning PSHOLD to “L”.
When PSHOLD becomes “L”, RESETO outputs “L” after 80ms. And then, all DC/DC and LDO turn off except LDO1 and LDODIG. DC/DC3 turns on again after 320ms. Then after that, each LDO turns on as the normal power-on sequence.

6.4 Stand-by Operation

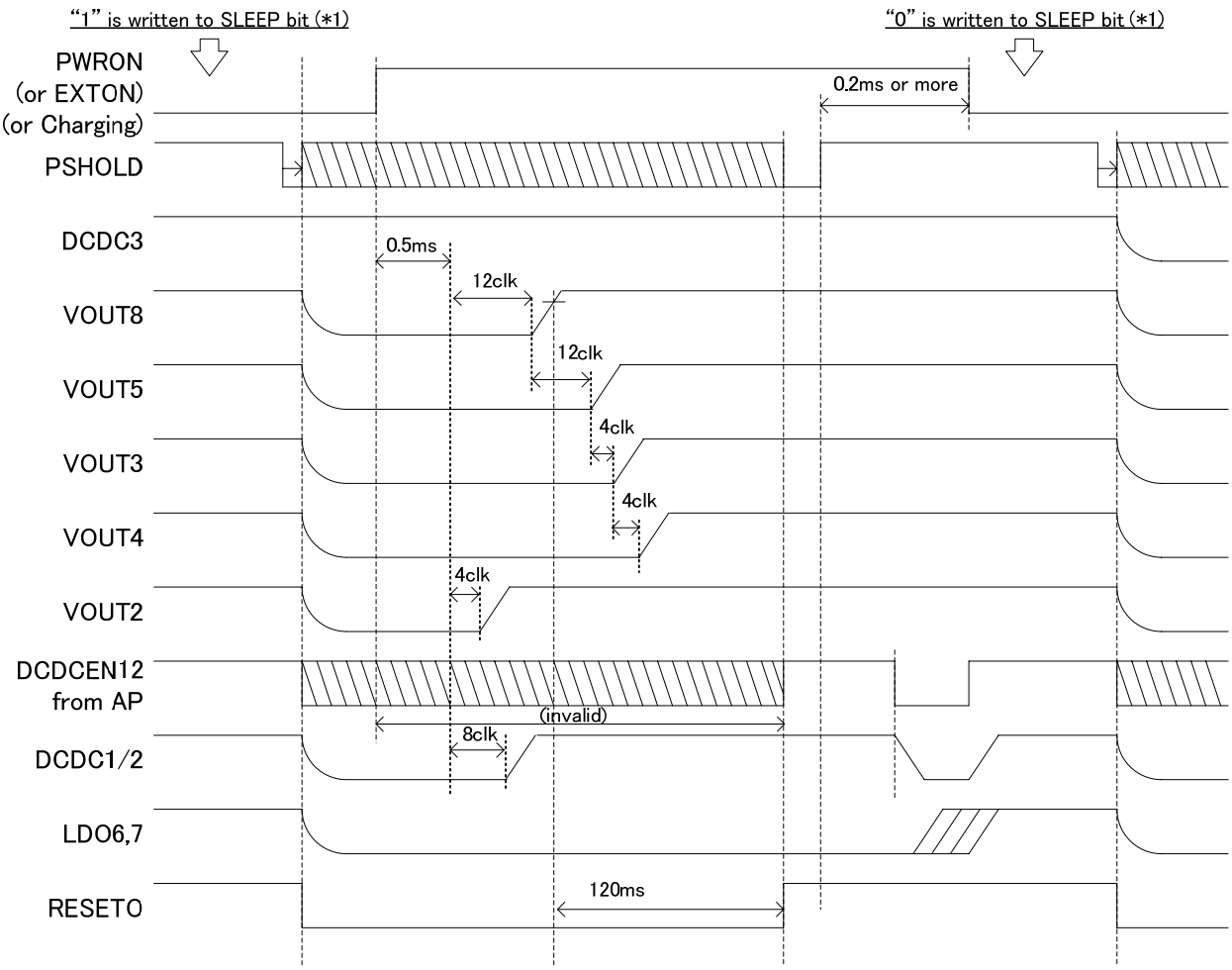


Fig 6-3 Stand-by Timing

When SLEEP bit is "1", and power-on factor and PSHOLD become "L", all DC/DC and LDO turn off (except LDO1 and LDODIG) with maintaining DC/DC3 turned on. (Note*)
When "H" signal is input to PWRON pin or EXTON pin, the normal power-on sequence starts. SLEEP bit is reset by UVLO.

Note*: Stand-by operation will not be executed at the following conditions: Soft Reset, RESDET detection, and latch protection of DC/DC.

6.5 UVLO (Under Voltage Lock Out) Electrical Characteristics

When the system cannot operate due to the low battery voltage, UVLO turns off the system (SLEEP bit is reset by UVLO).

Operating Conditions (unless otherwise specified) T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{Release}$	Under voltage lock out threshold	VIN rising		2.8		V
V_{Detect}	Under voltage lock out threshold	VIN falling	-3%	2.7	+3%	V
V_{HYS}	UVLO Hysteresis	-		100		mV

Table 6-1 UVLO Electrical Characteristics

6.6 TSHUT (Thermal Shutdown Circuit) Electrical Characteristics

The thermal shutdown circuit turns off the system and prevents the chip from damaging when overheating is detected. When the temperature changes back to Return Temperature, the power-on sequence is started again if there is power-on factor. If there is no power-on factor, the state remains power-off.

Operating Conditions (unless otherwise specified) VIN = 3.6V

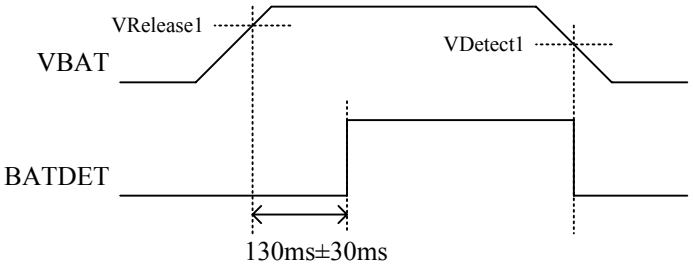
Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DET}	Detected Temperature	-		135		degrees C
T_{RET}	Return Temperature	-		110		degrees C
I_{SS}	Supply Current	-		7		μA

Table 6-2 Thermal Shutdown Circuit Electrical Characteristics

7. Voltage Detector

7.1 VBAT Detector (VD1) Electrical Characteristics

After VBAT pin rises, BATDET signal turns to "H" after 100ms (Min.) from the VBAT Detector is released.
The default is 3.3V, but it can be changed by the register.
BATDET is Nch-opendrain output pin, and if it is used, pull up the pin with the voltage not exceeding VIN power.



Operating Conditions (unless otherwise specified) T_a = 25 degrees C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{Release1}$	VD1 Threshold Voltage	VBAT rising	-3%	3.3 (*1)	+3%	V
$V_{Detect1}$	VD1 Threshold Voltage	VBAT falling		3.1		V
V_{Hys1}	VD1 Hysteresis	-		0.2		V

Note*1: The threshold voltage is set by setting the register.

Table 7-1 VD1 Electrical Characteristics

7.2 RESDET Detector (VD2) Electrical Characteristics

The RESDET Detector detects LDO8 voltage.
At the RESDET, "L" is output from RESETO pin. 120ms after RESDET is released, "H" is output.
After RESDET is released, DC/DC and LDO turn off except LDO1 and LDODIG when LDO8 voltage drops lower than the detection voltage. After DC/DC and LDO are turned off, the power-on sequence is started again if there is power-on factor. If there is no power-on factor, the state remains power-off.

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{Release2}$	VD2 Threshold Voltage	Vout8 rising	-3%	Vout8 × 85% (*1)	+3%	V
V_{Hys2}	VD2 Hysteresis	-		100		mV

Note*1: The threshold voltage is set by setting the register.

Table 7-2 RESDET Electrical Characteristics

8. Regulator

8.1 Regulator Table

	DC/DC1	DC/DC2	DC/DC3
Initial Value	1.20V (*1)	1.15V (*2)	1.8V
Output Voltage Range	0.9～1.5V 12.5mVstep	0.9～1.5V,1.8V 12.5mVstep	1.8～3.3V
Output Current (MAX)	1200mA	1000mA	500mA
External Inductor (*4)	2.2µH	2.2µH	2.2µH
External Capacitor Spec-B(*4)	10µF	10µF	4.7µF
Output Control	I2C (with RAMP Control)	I2C (with RAMP Control)	External R
ON/OFF Control	I2C or DCDCEN12	I2C or DCDCEN12	I2C or DCDCEN3 (*3)
Initial State	ON	ON	ON
For use	(Core)	(Logic)	(Memory)

Note*1: Selected by trimming (Initial Value:1.00/1.10/1.20/1.25/1.30V/1.425V)
Note*2: Selected by trimming (Initial Value:0.95/1.05/1.15/1.20/1.50/1.80V)
Note*3: Selected by trimming (DCDCEN3 pin is valid or invalid)
Note*4: Recommended component

Bypass Capacitors for DC/DC1,2	10uF : C1608JB0J106M(TDK)
Bypass Capacitors for DC/DC3	4.7uF : C1608JB1A475KT(TDK)
Inductor For DCDC1,2	2.2uH : NRH2410T2R2MN(TAIYO-YUDEN)
Inductor For DCDC3	2.2uH : MLP2012S2R2M(TDK)
Input Capacitors for DC/DC	2.2uF : LMK107BJ225KA-T(TAIYO-YUDEN)

Table 8-1 Regulator Table (DC/DC)

	LDO1	LDO2	LDO3	LDO4	LDO5	LDO6	LDO7	LDO8
Initial Value	3.0V (*1)	1.2V	1.2V	3.3V	1.8V (*1)	2.6V	3.0V	3.3V (*1)
Output Voltage Range	-	0.9～1.3V	0.9～1.3V	1.8～3.3V	1.8～3.3V	1.2～3.3V	1.2～3.3V	1.8～3.3V
Output Current (MAX)	10mA	30mA	30mA	300mA	300mA	150mA	150mA	150mA
External Capacitor Spec-B(*4)	1.0µF	1.0µF	1.0µF	1.0µF	1.0µF	1.0µF	1.0µF	1.0µF
Output Control	-	I2C	I2C	I2C	I2C	I2C	I2C	I2C
ON/OFF	-	I2C	I2C	I2C	I2C	I2C	I2C	-
Initial State	Keep ON	ON (*2)	ON (*3)	ON (*3)	ON (*3)	OFF	OFF	ON
For use	(RTC)	(Alive) (PLL)	(USB OTG)	(Memory) (Peripheral)	(USB) (MMC)	(Host I/F)	(LCD)	(System)

Note*1: Selected by trimming (LDO1:3.0/1.8V, LDO5:3.0V/1.8V, LDO8:3.0V/3.3V)
Note*2: Selected by trimming (Initial State:Power_on or Keep ON)
Note*3: Selected by trimming (Initial State:Power_on or OFF)
Note*4: Recommended component

Bypass Capacitors for LDO	1uF : GRM155B31A105KE15

Table 8-2 Regulator Table (LDO)

8.2 Step-down DC/DC Converter

RN5T614 has two PWM/PFM/PSM step-down DC/DC converters and one One-shot PWM DC/DC converter. They employ external inductor and capacitor for smoothing output voltage. DC/DC3 sets output voltage by the external resistance.

8.2.1 Step-down DC/DC1 and DC/DC2 Converter

RN5T614 has CMOS-based PWM/PFM/PSM step-down DC/DC1 (DC/DC2) converter with a low supply current. PWM/PFM/PSM mode is controlled in two methods. One is AUTO mode that automatically switches PWM/PFM, and the other is the register setting that sets AUTO/PWM/PSM through I2C. The output voltage is also programmable by DD1DAC (DD2DAC) register.
Since DD1MODE (DD2MODE) bit and DD1DAC (DD2DAC) are reset when DC/DC1 (DC/DC2) turns off, the next activation starts at 1.20V that is the default of DD1DAC (1.15V that is the default of DD2DAC).

DC/DC1 and DC/DC2 converters have RAMP control function.

RN5T614 integrates the latch protection function to avoid any malfunctions by over current. The current limit circuit monitors over current with LX1 (LX2) clock cycle.
When over current is detected and continues for a certain time (10ms), RESETO outputs “L”. And then, all DC/DC and LDO turn off except LDO1 and LDODIG.
After DC/DC and LDO are turned off, the power-on sequence is started again if there is power-on factor. If there is no power-on factor, the state remains power-off.

DC/DC1 and DC/DC2 converters can be easily composed with only few external components such as inductor, capacitor and etc. For the output capacitor, the ceramic type should be used for reducing the ripple voltage.

8.2.1.1 Step-down DC/DC1 and DC/DC2 Converters Block Diagram

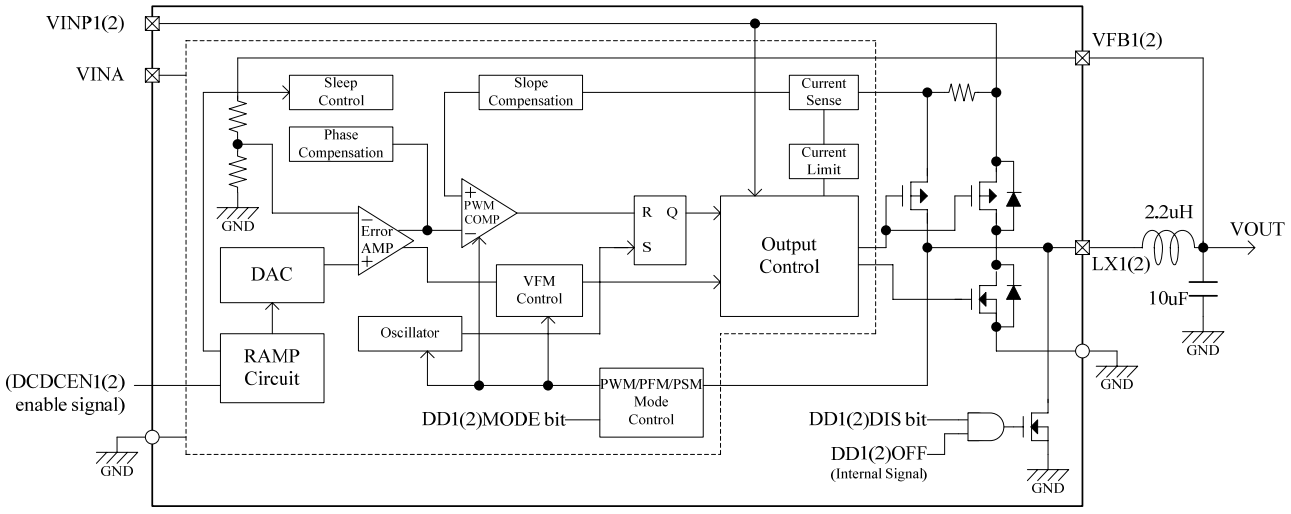


Fig 8-1 Step-down DC/DC1 and DC/DC2 Converter Block Diagram

8.2.1.2 RAMP Control Operation

This function starts by setting DD1(2)DAC register. The ramp rate is controllable by RAMP1(2)SLOP bit.

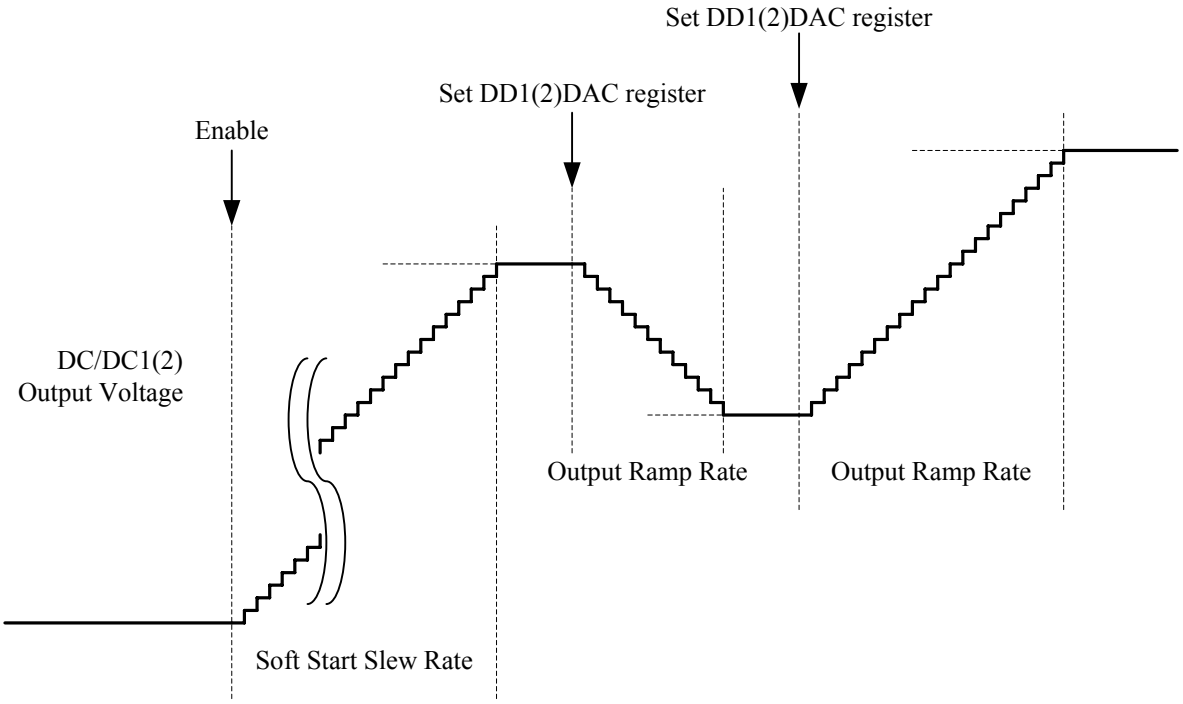


Fig 8-2 Ramp up/down Control Timing Chart

8.2.1.3 Step-down DC/DC1 and DC/DC2 Converter Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, L=2.2µH, C_{OUT} = 10µF, T_a = 25 degrees C

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{IN}	Input voltage range	-		3.1	3.6	5.5	V
V_{OUT}	Range of output voltage	DC/DC1	1mA < I_{OUT} < 1200mA	0.9	1.20	1.5	V
		DC/DC2	1mA < I_{OUT} < 1000mA	0.9	1.15	1.8	
	Voltage setting step width	-			12.5		mV
Vaccu	Output voltage accuracy 1mA < I_{OUT} < Ilx, 3.1V < V_{IN} < 5.5V -40 degrees C < T_a < 85 degrees	PFM/PSM Mode	V_{OUT} =0.9V~1.0V	-27	8.5	44	mV
			V_{OUT} =1.0V~1,5V,1.8V	-2.5	1	4.5	%
		PWM Mode	V_{OUT} =0.9V~1.0V	-35		35	mV
			V_{OUT} =1.0V~1.5V,1.8V	-3.5		3.5	%
Vrip	Output ripple voltage	PFM/PSM Mode Iout=1mA			25		mV
$\Delta V_{OUT}/\Delta T_a$	Output voltage temperature coefficient	-40 degrees C < T_a < 85 degrees C			±100		ppm/ degreesC
Fosc	Switching frequency	-			2.2		MHz
Ilx	Maximum output current	DC/DC1(AUTO/PWM Mode)		1200			mA
		DC/DC2(AUTO/PWM Mode)		1000			mA
		DC/DC1,2(PSM Mode)		10			mA
Ilim	Limit current	DC/DC1			1800		mA
		DC/DC2			1500		mA
Vpeak	Output transition response	10→500mA@ΔT=1µs, V_{OUT} =1.2V			50		mV
Tprot	Protection delay time	-			10		ms
Iss	Consumption current	AUTO Mode	I_{OUT} =0mA		50		µA
		PSM Mode	I_{OUT} =0mA		25		µA
H1	Efficiency peak	V_{OUT} = 1.20V, I_{OUT} =1mA			75		%
		V_{OUT} = 1.20V, Iout =η_peak			85		%

Table 8-3 DC/DC1 and DC/DC2 Electrical Characteristics

8.2.2 Step-down DC/DC3 Converter Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, L=2.2µH, C_{OUT} = 4.7µF, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		3.1		5.5	V
V_{OUT}	Output Voltage Range		1.8		3.3	V
Ilx	Maximum output current	3.1V≦VIN≦5.5V	500			mA
Iss	Consumption Current	V_{IN} = V_{FB} =3.6V Ilx =0mA, no switching		70		µA
I_{OFF}	Standby Current	OFF state			1	µA
Ilim	Limit detection Current	-	800			mA
V_{FB}	FB Voltage	V_{IN} = V_{FB} =3.6V, Ilx =1mA	-1.5%	0.608	+1.5%	V
$\Delta V_{FB}/\Delta V_{IN}$	FB Line Regulation	V_{OUT} +0.5≦V_{IN}≦5.5V, Ilx = Ilxmax / 2		10		mV
$\Delta V_{FB}/\Delta Ilx$	FB Load Regulation	1mA≦Ilx≦500mA		2		mV
$\Delta V_{FB}/\Delta Ta$	FB Voltage Temperature Coefficient	-40 degrees C≦Ta≦+85 degrees C		±100		ppm/ degrees C
tr	Soft-start Time	-		120		µs

Table 8-4 DC/DC3 Electrical Characteristics

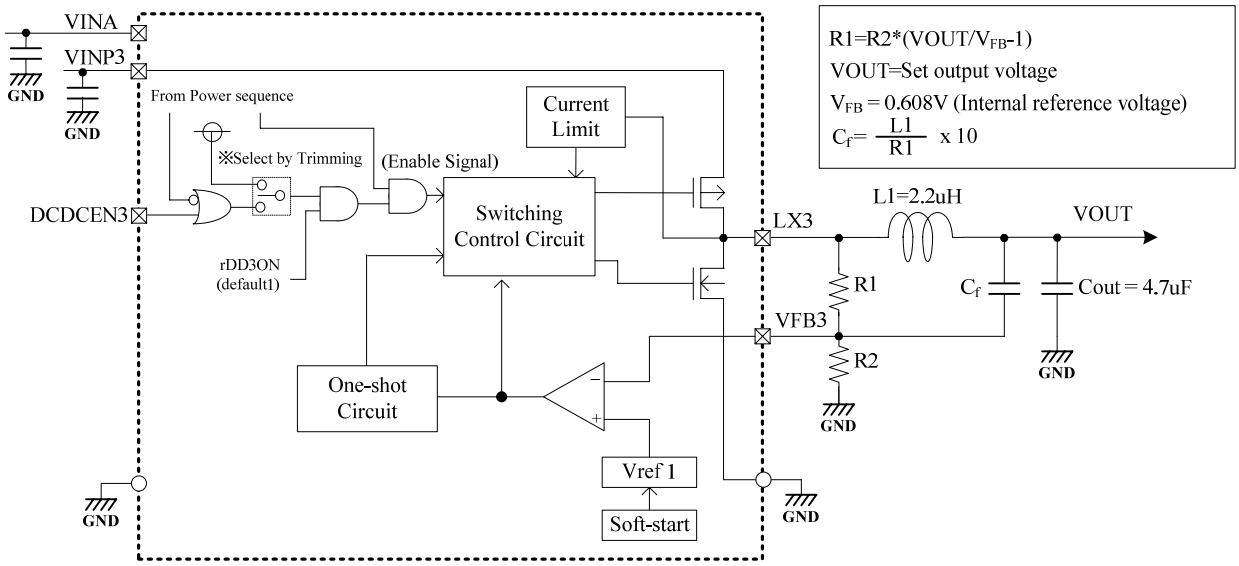


Fig 8-3 DC/DC3 Block Diagram

Output Voltage	R1	R2	Cf	Notes
3.3V	120kΩ	27kΩ	180pF	
2.5V	150kΩ	47kΩ	150pF	
1.8V	220kΩ	110kΩ	100pF	

Table 8-5 DC/DC3 External Components Example

8.3 LDO

RN5T614 has eight LDOs. LDO1 for RTC is always on, and it has the reverse-current prevention circuit.
VREF circuit is only for the internal reference voltage, so it cannot be used as the external reference voltage.
For optimized phase compensation, the bypass capacitor must be the ceramic type.

8.3.1 LDO Electrical Characteristics

8.3.1.1 LDO1 Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, C_{OUT} = 1.0µF, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	-	3.1	3.6	5.5	V
V_{OUT}	Output Voltage (*2)	3.1V≦V_{IN}≦5.5V 50µA≦I_{OUT}≦10mA	-3%	3.0 / 1.8	+3%	V
I_{OUT}	Output Current	-			10	mA
I_{SHT}	Short Current	V_{OUT}=0V		30		mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{OUT}+0.2V≦V_{IN}≦5.5V I_{OUT}=I_{OUTMAX} /2		3		mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	50µA≦I_{OUT}≦10mA		30		mV
$\Delta V_{OUT}/\Delta T_a$	Output Voltage Temperature Coefficient	-40 degrees C≦T_a≦85 degrees C		±100		ppm/ degrees C
I_{SS}	Supply Current (*1)	ON		1	3	µA
I_{RR}	Reverse Current	V_{OUT}=3.0V & V_{IN} =0V		0.15		µA

Table 8-6 LDO1 Electrical Characteristics

Note*: Bypass capacitor: 1.0µF, in mounted state.
For optimized phase compensation, the bypass capacitor must be the ceramic type.
Note*1: The consumption current of the reverse protection is not included.
Note*2: Initial value selected by trimming (3.0V or 1.8V)

8.3.1.2 LDO2 and LDO3 Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, C_{OUT} = 1.0µF, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	-	3.1	3.6	5.5	V
V_{OUT}	Output Voltage Range	3.1V≦V_{IN}≦5.5V, 50µA≦I_{OUT}≦I_{OUTMAX}	-3%	0.9 ～1.3	+3%	V
I_{OUT}	Output Current	-			30	mA
I_{SHT}	Short Current	V_{OUT}=0V		65		mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	3.1V≦V_{IN}≦5.5V, I_{OUT}= I_{OUTMAX} /2			10	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	50µA≦I_{OUT}≦I_{OUTMAX}			30	mV
ΔV_{OUT}	Transient Response	50µA⇔I_{OUTMAX} /2 (⊿t=1us)		50		mV
$\Delta V_{OUT}/\Delta T_a$	Output Voltage Temperature Coefficient	-40 degrees C≦T_a≦85 degrees C		±100		ppm/ degrees C
RR	Ripple Rejection	f=10kHz, I_{OUT}= I_{OUTMAX} / 2		60		dB
EN	Output Noise (RMS)	BW=100Hz-100kHz, I_{OUT}= I_{OUTMAX} / 2		50		µVrms
I_{SS}	Supply Current	I_{OUT}=0mA		20		µA
I_{OFF}	Standby Current	I_{OUT}=0mA			1	µA
T_r	Rising Time	V_{OUT}≧0.7×V_{OUT}, I_{OUT} =0mA			200	µs
T_f	Falling Time	V_{OUT}≦0.3×V_{OUT}, I_{OUT} =0mA			500	µs
V_{SET}	Programmable Output Voltage	I_{OUT}= I_{OUTMAX} /2	-3%	0.9 1.0 1.1 1.2 1.3	+3%	V

Table 8-7 LDO2 and LDO3 Electrical Characteristics

Note*: Bypass capacitor: 1.0µF, in mounted state.
For optimized phase compensation, the bypass capacitor must be the ceramic type.

8.3.1.3 LDO4 and LDO5 Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, C_{OUT} = 1.0µF, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	-	3.1	3.6	5.5	V
V_{OUT}	Output Voltage Range	V_{OUT} +0.3V≦V_{IN}≦5.5V & 3.1V≦V_{IN}≦5.5V, 50µA≦I_{OUT}≦I_{OUTMAX}	-3%	1.8 ～3.3	+3%	V
I_{OUT}	Output Current	-			300	mA
I_{SHT}	Short Current	V_{OUT} = 0V		75		mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{OUT} +0.3V≦V_{IN}≦5.5V & 3.1V≦V_{IN}≦5.5V, I_{OUT}= I_{OUTMAX} /2			10	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	50µA≦I_{OUT}≦I_{OUTMAX}			60	mV
ΔV_{OUT}	Transient Response	50µA⇔I_{OUTMAX} /2(⊿t=1us)		100		mV
V_{IN} -V_{OUT}	Voltage difference	V_{IN} >3.1V, V_{IN} = V_{SET}, I_{OUT}= I_{OUTMAX}			0.3	V
$\Delta V_{OUT}/\Delta T_a$	Output Voltage Temperature Coefficient	-40 degrees C≦T_a≦85 degrees C		±100		ppm/ degrees C
RR	Ripple Rejection	V_{OUT}≦3.0V, f=10kHz, I_{OUT}= I_{OUTMAX} / 2		60		dB
EN	Output Noise (RMS)	BW=100Hz-100kHz, I_{OUT}= I_{OUTMAX} / 2		75		µVrms
I_{SS}	Supply Current	I_{OUT}=0mA		20		µA
I_{OFF}	Standby Current	I_{OUT}=0mA			1	µA
T_r	Rising Time	V_{OUT}≧0.7×V_{OUT}, I_{OUT} =0mA			200	µs
T_f	Falling Time	V_{OUT}≦0.3×V_{OUT}, I_{OUT} =0mA			500	µs
V_{SET}	Programmable Output Voltage	I_{OUT}= I_{OUTMAX} /2	-3%	1.80 2.50 2.60 2.80 2.85 3.00 3.30	+3%	V

Table 8-8 LDO4 and LDO5 Electrical Characteristics

Note*: Bypass capacitor: 1.0µF, in mounted state.
For optimized phase compensation, the bypass capacitor must be the ceramic type.

8.3.1.4 LDO6, LDO7 and LDO8 Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{IN} = 3.6V, C_{OUT} = 1.0µF, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	-	3.1	3.6	5.5	V
V_{OUT}	Output Voltage Range (*1)	V_{OUT}+0.3V≦V_{IN}≦5.5V & 3.1V≦V_{IN}≦5.5V, 50µA≦I_{OUT}≦I_{OUTMAX}	-3%	1.2 ～3.3	+3%	V
I_{OUT}	Output Current	-			150	mA
I_{SHT}	Short Current	V_{OUT} = 0V		75		mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{OUT} +0.3V≦V_{IN}≦5.5V & 3.1V≦V_{IN}≦5.5V, I_{OUT}= I_{OUTMAX} /2			10	mV
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	50µA≦I_{OUT}≦I_{OUTMAX}			40	mV
ΔV_{OUT}	Transient Response	50µA⇔I_{OUTMAX} /2(⊿t=1us)		50		mV
V_{IN} -V_{OUT}	Voltage difference	V_{IN} >3.1V, V_{IN} = V_{SET}, I_{OUT}= I_{OUTMAX}			0.3	V
$\Delta V_{OUT}/\Delta T_a$	Output Voltage Temperature Coefficient	-40 degrees C≦T_a≦85 degrees C		±100		ppm/ degrees C
RR	Ripple Rejection	V_{OUT}≦3.0V, f=1kHz, I_{OUT}= I_{OUTMAX} / 2		60		dB
EN	Output Noise (RMS)	BW=100Hz-100kHz, I_{OUT}= I_{OUTMAX} / 2		85		µVrms
I_{SS}	Supply Current	I_{OUT}=0mA		20		µA
I_{OFF}	Standby Current	I_{OUT}=0mA			1	µA
T_r	Rising Time	V_{OUT}≧0.7×V_{OUT}, I_{OUT} =0mA			200	µs
T_f	Falling Time	V_{OUT}≦0.3×V_{OUT}, I_{OUT} =0mA			500	µs
V_{SET}	Programmable Output Voltage (*1)	I_{OUT}= I_{OUTMAX} /2	-3%	1.20 1.80 2.50 2.60 2.80 2.85 3.00 3.30	+3%	V

Table 8-9 LDO6, LDO7 and LDO8 Electrical Characteristics

Note*: Bypass capacitor: 1.0µF, in mounted state.
For optimized phase compensation, the bypass capacitor must be the ceramic type.
Note*1: 1.2V setteing except LDO8

9. Li-ion Battery Charger

RN5T614 integrates a Li-ion Battery charger.

---It supports AC adapter charging.

---With the current limit protection and charge current control, the limited power can be efficiently supplied to the system and the battery.

---The system can power on even when Li-ion Battery is low voltage or open.

---The device can withstand up to 6.5V on VCHG pin. However, it can withstand high voltage by combining a high voltage protection IC (up to 28V by using BD6040 of ROHM).

---Rapid timer and Trickle timer integrated.

---Monitor for the battery thermistor built in.

---No external MOSFET required.

---If the system loads over AC adapter current rating, the battery will supply the current to the system.

---Chip temperature detection circuit for over temperature protection integrated.

---Ibat maximum tolerant current: 1.2A

9.1 Li-ion Battery Charger Block Diagram

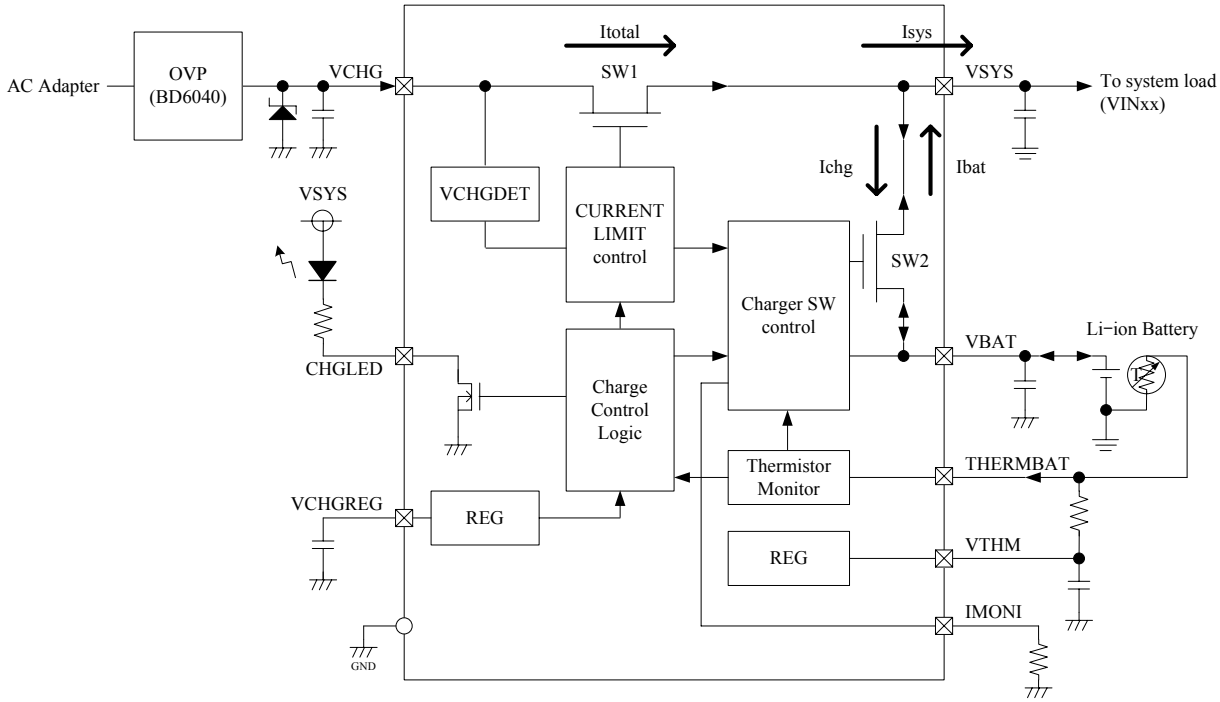


Fig 9-1 Li-ion Battery Charger Block Diagram

9.2 Explanation of Charge Block Operating

If AC adapter is connected to VCHG pin, the charger detects the voltage on VCHG pin.

$4.3V < V_{VCHG} < 6.2V$ (1)

If the voltage is as above, the charger will operate.
If the voltage is other than the above, the charger will not operate.

When (1), the charger switches the power source between VCHG and VBAT when it is in the state of Charge-Ready or Trickle Charge or Rapid-Charge and also it satisfies the following conditions.

Temperature < 125 degrees C (Programmable)

The charger implements the means of checking the presence of the battery. If it detects no battery, the power of VSYS is supplied by VCHG until the battery is detected.

It is assumed that AC adapter voltage is 5V within 10%. Other values of voltage are not recommended because the die temperature rises due to the generated heat by increasing the voltage of AC adapter.

The current limit of SW1 is set by the register as below.

Ilim > Ichg

The value of the register set for the current limit of SW1 is set lower than the current capacity of AC Adapter.

Note*: Initial value of current limit of SW1 is 720mA.

CHGLED pin is the Nch-open-drain output.
It turns on at the Rapid-Charge state and turns off at the Charge Complete.
At the Trickle-Charge or Abnormal state, it flashes on and off at 1-2Hz.

Li-ion Battery Charger state Diagram

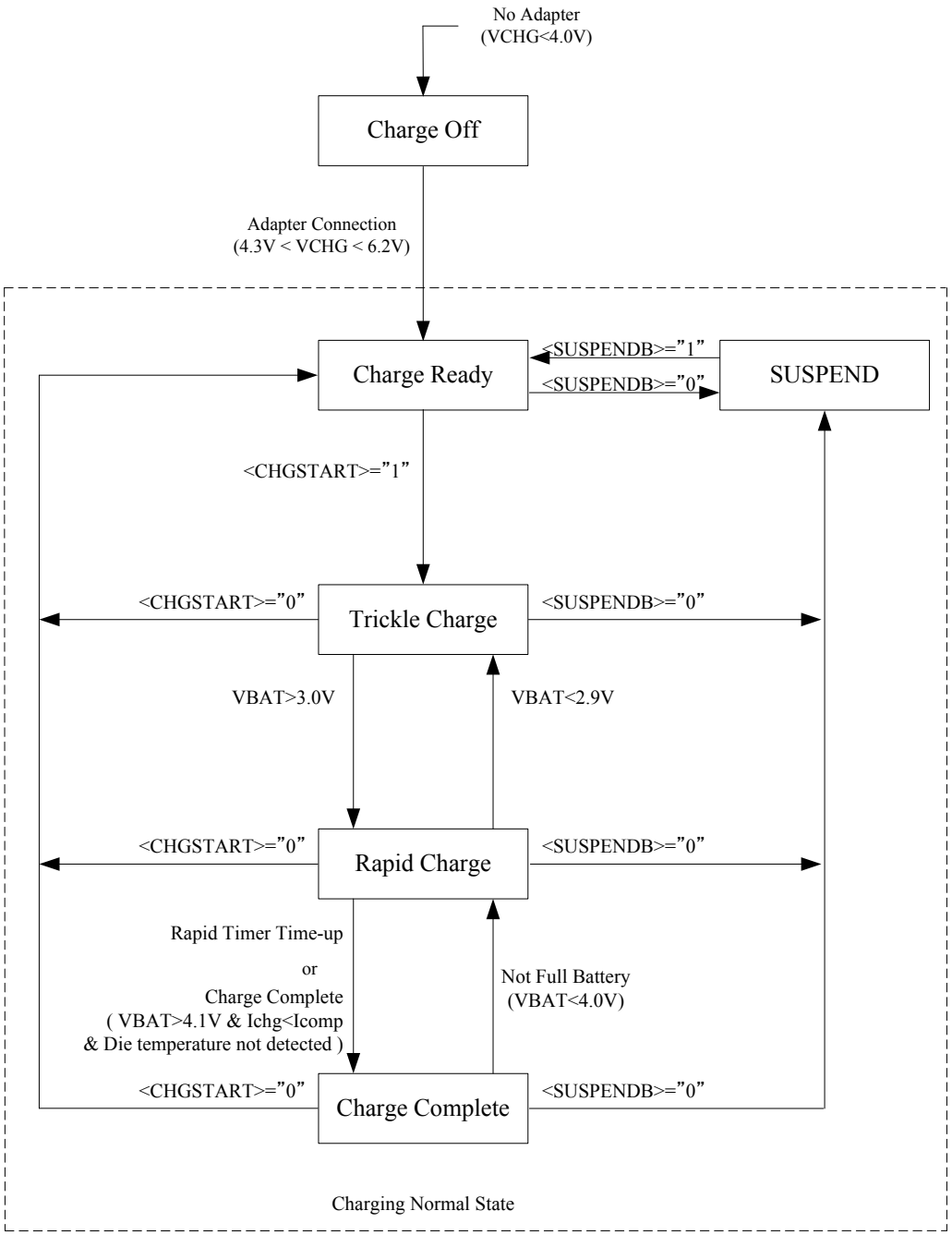


Fig 9-2 Li-ion Battery Charger State Flow (Normal State)

Li-ion Battery Charger state Diagram (Abnormal)

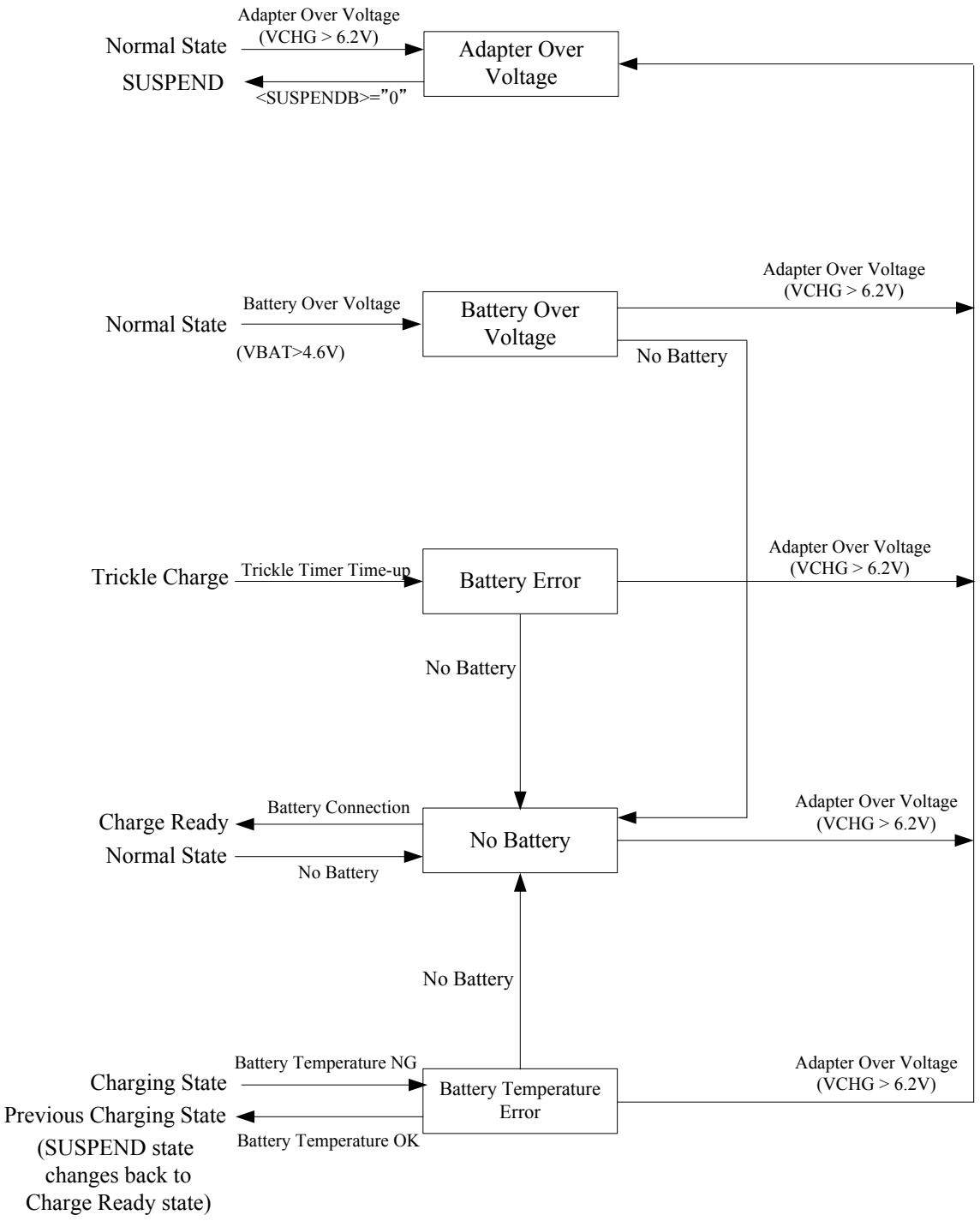


Fig 9-3 Li-ion Battery Charger State Flow (Abnormal State)

[Charge-Off]
The power is supplied by battery through VSYS pin:

- When a power supply device is not connected to VCHG pin.
- When V_{VCHG} is lower than 4.3V.

[SUSPEND]
The state changes to SUSPEND by writing "0" into SUSPENDB bit when the state is Charge Ready, Trickle charge, Rapid Charge, or Charge Complete. When the state is SUSPEND, the battery is not charged and VSYS is supplied by the current from the battery.
The state changes to Charge Ready by writing "1" into SUSPENDB bit.
SUSPENDB bit is set to "1" automatically and unable to set to "0" except when the state is Charge-Off, Adapter-Over-Voltage, SUSPEND, Charge-Ready, Trickle-Charge, Rapid-Charge and Charge-Complete.

[Charge-Ready]
When VCHG pin voltage exceeds 4.3V, the state shifts from Charge-Off to Charge-Ready.
When "0" is set to CHGSTART bit at Trickle-Charge, Rapid-Charge, or Charge-Complete state, it returns to Charge-Ready state, and the charging stops.

[Trickle-Charge]
When CHGSTART bit is “1”, the state shifts form Charge-Ready to Trickle-Charge.
If the battery voltage is less than 3.0V in Rapid-Charge, the state shifts to Trickle-Charge.
In Trickle-Charge state, Ichg is limited to 100mA.
The battery charging continues until V_{VBAT} becomes over 3.0V or Trickle-Timer is up. If the battery voltage becomes over 3.0V, the state shifts to Rapid-Charge. If Trickle-Timer is up before completing the trickle charge, the state shifts to Battery-Error, and the charger outputs the interrupt signal.

[Rapid-Charge]
Even when the power is supplied to the system through VCHG pin, the battery charging is still performed. The battery charge current is adjusted depending on the system load. If Itotal is lower than Ilim, the charger automatically increases Ichg gradually to the value set by register. On the other hand, if Itotal is higher than Ilim, the charger decreases Ichg immediately. The battery charging continues until three conditions as below are all met or Rapid-Timer is up.

1. Ichg < Icomp
2. V_{VBAT} > 4.1V
3. Die temperature not detected

In Rapid-Charge state, the battery charging is automatically performed.
When the charger detects the die temperature higher than the setting value during charging, Ichg is decreased to the lowest current.

[Charge-Complete]
When the charging is completed, the state shifts to Charge-Complete.
When V_{VBAT} becomes under 4.0V, the state shifts to Rapid-Charge.
In the state of Charge-Complete, the power is supplied to VSYS pin only by VCHG pin.

[Battery-Error]
User must confirm whether the connection situation of battery is right or not.

[No-Battery]
In any states except Adapter-Over-Voltage and Charge-Off state, when the thermistor monitoring circuit detects no battery, the state shifts to No-Battery, and the power is supplied only through VCHG pin until the battery is detected.

[Adapter-Over-Voltage]
The charger integrates a detector for the power supply device voltage. If the charger detects that V_{VCHG} is higher than 6.2V at any states, it supplies the power only from the battery to VSYS pin until V_{VCHG} becomes lower than 4.0V.
However, if the conditions for the transition to Battery-Over-Voltage, Battery-Error, No-Battery, and Battery-Temperature-Error state are satisfied at the same time, the power is supplied only through VCHG pin. And SUSPENDB bit is set to "1" automatically and unable to set to "0".

[Battery-Over-Voltage]
The charger integrates a detector for the battery voltage. If the charger detects that V_{VBAT} is higher than 4.6V at any states except Charge-Off, it supplies the power only through VCHG pin until the battery is disconnected.

[Battery-Temperature-Error]
The voltage of THERMBAT pin is always monitored. If the voltage becomes over 73% or under 23% of VTHM voltage set by VBTEMP, the battery temperature is determined as abnormal, and the state shifts to Battery-Temperature-Error.
In Battery-Temperature-Error state, except Charge-Off and Adapter-Over-Voltage, both charging for the battery and power supply from the battery to VSYS stop and the current supply for VSYS is only from the adapter.
If the voltage of THERMBAT pin recovers to the normal range, the state shifts to the one before the transition to Battery-Temperature-Error state.

9.3 Charge Interrupt Request

The charger outputs INTB pin. All interrupt requests can be masked/unmasked by setting the register.

Interrupt request list and details

- ADPDET Adapter insert & remove
- DIEOT Die abnormal temperature by SW1 or SW2 in charger
- VBTERR Battery abnormal temperature
- NOBATT No Battery detect
- VCOV Adapter over voltage (V_{VCHG}>6.2V)
- VBOV Battery over voltage (V_{VBAT} > 4.6V)
- STCR Shift to Charge-Ready state
- STRC Shift to Rapid-Charge state
- CHGCMP Charge complete
- TIMEOUT Time out of Trickle Time or Rapid Timer

Note*: DIEOT, VBTERR and NOBATT are Level interrupt requests.
On the other hand, the other interrupts are generated only when the interrupts appear.

For the details of interrupt, refer to Chapter 10 Interrupt Controller (INTC).

9.4 Li-ion Battery Charger Electrical Characteristics

Operating Conditions (unless otherwise specified) V_{VCHG} = 5.0V, V_{VSYS} = 4.8V, V_{VBAT} = 3.6V, T_a = -40～85 degrees C

Symbol	Parameter	Setting	Condition	Min	Typ	Max	Unit
POWER INPUT							
V_{VCHG}	AC Adapter Input Voltage		Operating voltage	4.3		6.2	V
			Recommended voltage	4.5	5	5.5	V
V_{VSYS}	VSYS Regulation Voltage		V_{VCHG} =5.5V, Itotal=500mA, Ta=-10～60 degrees C	4.65	4.8	4.95	V
Ilim	Current Limit	120mA	V_{VCHG} =5V, V_{VSYS} =4V, Ta=-10～60 degrees C	84	102	120	mA
		240mA		192	216	240	
		360mA		288	324	360	
		480mA		384	432	480	
		600mA		480	540	600	
		720mA *		576	648	720	
		840mA		672	756	840	
		960mA		768	864	960	
		1080mA		864	972	1080	
		1200mA		960	1080	1200	
V_{ADET}	AC Adapter Detection Voltage	Rising	-	4.15	4.3	4.45	V
		Hysteresis			0.3		
V_{AOV}	AC Adapter Over Voltage detection		-	5.8	6.2	6.5	V
R_{SW1}	Dropout Resistance		V_{VCHG} =4.7V, Itotal=500mA, Ta=-10～60 degrees C		200	500	mohm
V_{OL}	CHGLED “L” Output Voltage		I_{SINK}= 10mA			0.4	V
I_{OZ}	Off Leakage Current		VIN=0～V_{VSYS}, Pin= CHGLED	-3		3	µA

Table 9-1 Battery Charger Electrical Characteristics (POWER INPUT)

Note*: “*” is the initial value. The set value is changed by setting the register.

Operating Conditions (unless otherwise specified) V_{VCHG} = 5.0V, V_{VSYS} = 4.8V, V_{VBAT} = 3.6V, T_a = -40～85 degrees C

Symbol	Parameter	Setting	Condition	Min	Typ	Max	Unit
BATTERY CHARGER							
V_{BCHG}	Battery Charge Voltage	4.2V *	Ta=-10～60 degrees C, Ichg=25mA	4.17	4.2	4.23	V
		4.12V		4.085	4.12	4.155	V
		4.07V		4.035	4.07	4.105	V
Ichg	Rapid Charge Current	100mA	Ta=-10～60 degrees C	70	85	100	mA
		200mA		100	150	200	mA
		300mA		200	250	300	mA
		400mA		300	350	400	mA
		500mA *		400	450	500	mA
		600mA		400	500	600	mA
		700mA		500	600	700	mA
		800mA		600	700	800	mA
		900mA		700	800	900	mA
Itri	Trickle Charge Current	100mA	Ta=-10～60 degrees C	70	85	100	mA
Icomp	Charging Completion Current	25mA *	Ta=-10～60 degrees C		25		mA
		50mA			50		mA
		75mA			75		mA
		100mA			100		mA
		125mA			125		mA
		150mA			150		mA
		175mA			175		mA
		200mA			200		mA
V_{RCHG}	Rapid Charging Threshold Voltage	Rising	Ta=-10～60 degrees C	2.9	3	3.1	V
		Hysteresis			0.1		
V_{CCMP}	Charging Completion Voltage (Re-Charging Voltage)	Rising	Ta=-10～60 degrees C	4.05	4.1	4.15	V
		Hysteresis			0.1		
V_{BOV}	Battery Over Voltage detection		-	4.5	4.6	4.7	V
V_{BTEMP}	THERMBAT Threshold	Low Temperature	Ratio of VTHM Voltage		73		%
		High Temperature			23		%
T_{DTEMP}	Die Temperature Control Threshold		Detection Temperature (Programmable)		105 115 125 135		degrees C
			Hysteresis		20		
R_{SW2}	On Resistance		V_{VBAT} =4.2V, Ibat=1A		60	120	mohm
Ttri	Timer	Trickle Timer	Ta=-10～60 degrees C		40		min
Trap		Rapid Timer			120 *		min
Ibatmax	Ibat maximum tolerant current	Power supply current from Li-ion battery	3.4V < V_{VBAT} < 4.2V			1.2	A

Table 9-2 Battery Charger Electrical Characteristics (BATTERY CHARGE)

Note*: "*" is the initial value. The set value is changed by setting the register.

10. Interrupt Controller (INTC)

RN5T614 has an interrupt controller (INTC).
CPU can read all the permitted interrupt request flags coming from different functional blocks. When an interrupt occurs, CPU is informed by asserting INTB pin and reading Monitor register (MON_***) to identify which block is producing the interrupt. Monitor register is read-only. OR gate signal of each permitted interrupt request flag (IR_***) will be output from INTB pin.
CPU can figure out the current state of RN5T614 by reading Monitor register at power-on. To enable interrupt output through INTB pin, it is necessary to write "1" in Enable register (EN_***).

10.1 Interrupt Controller Block Diagram

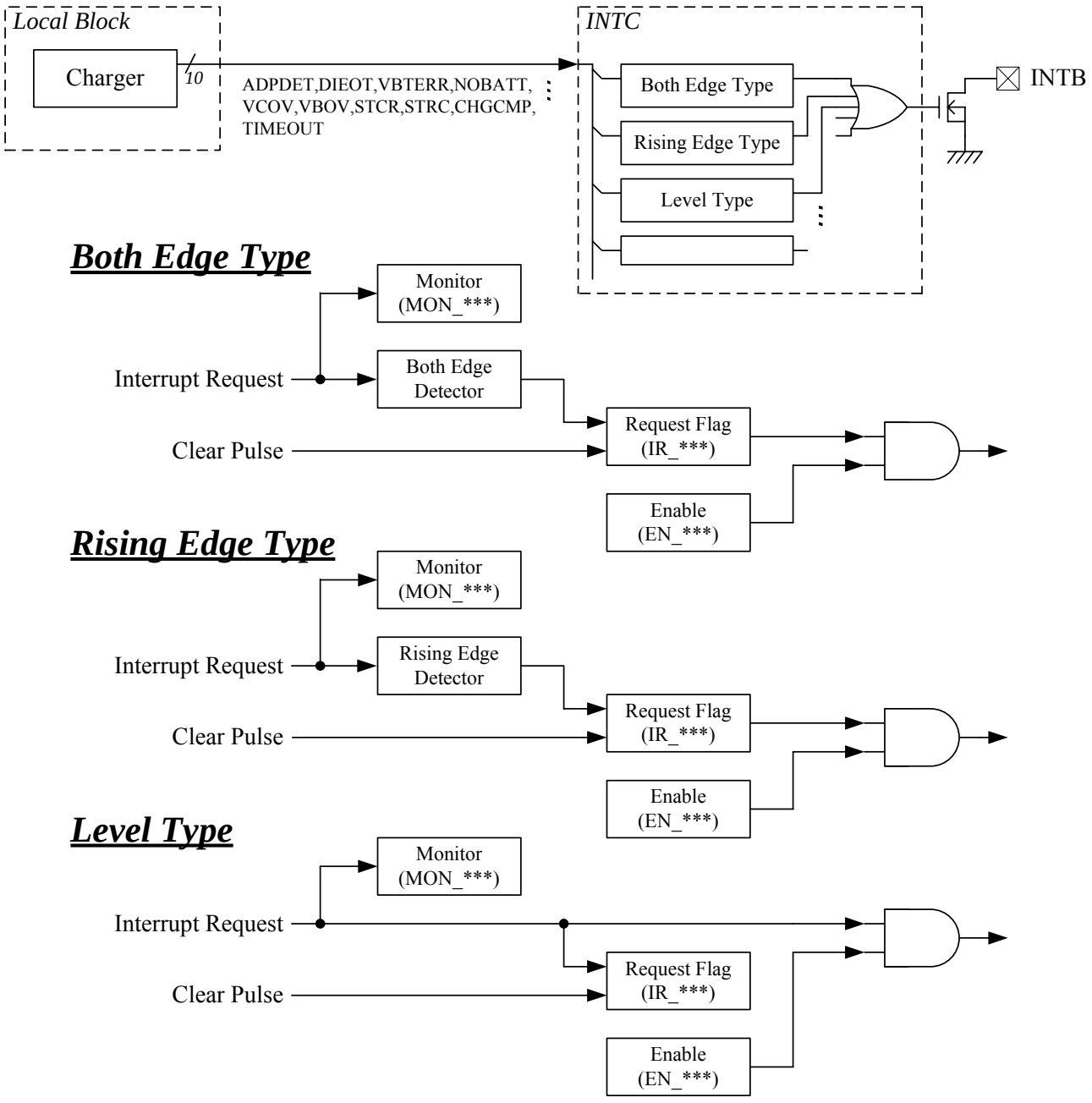


Fig 10-1 INTC Block Diagram

10.2 Interrupt Timing Chart

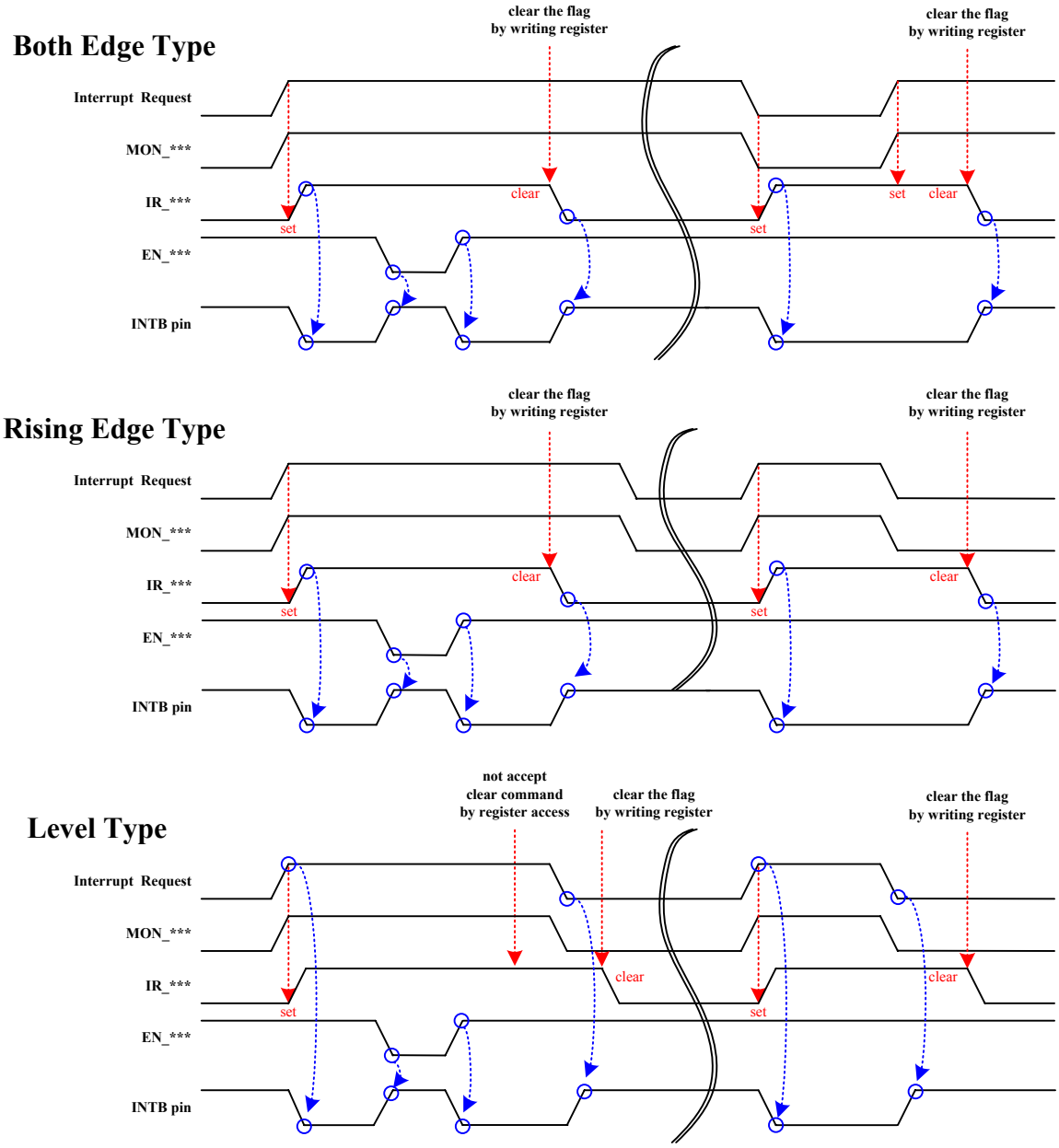


Fig 10-2 Interrupt Timing Chart

10.3 Interrupt Request List

Block	Interrupt Request	Detect condition Level/Edge	Enable (EN_***)	Monitor (MON_***)	Request Flag (IR_***)
CHARGER	ADPDET	Both Edge	EN_ADPDET	MON_ADPDET	IR_ADPDET
	DIEOT	Level	EN_DIEOT	MON_DIEOT	IR_DIEOT
	VBTERR	Level	EN_VBTERR	MON_VBTERR	IR_VBTERR
	NOBATT	Level	EN_NOBATT	MON_NOBATT	IR_NOBATT
	VCOV	Rising Edge	EN_VCOV	MON_VCOV	IR_VOOV
	VBOV	Rising Edge	EN_VBOV	MON_VBOV	IR_VBOV
	STCR	Rising Edge	EN_STCR	---	IR_STCR
	STRC	Rising Edge	EN_STRC	---	IR_STRC
	CHGCMP	Rising Edge	EN_CHGCMP	---	IR_CHGCMP
	TIMEOUT	Rising Edge	EN_TIMEOUT	---	IR_TIMEOUT

Table 10-1 Interrupt Request List

11. CPU Interface

RN5T614 uses I2C-Bus system for CPU connection through two wires. Connection and transfer system of I2C-Bus are described in the following sections.

11.1 I2C-Bus Operation

Within the procedure of I2C-Bus, unique situations arise which are defined as Start and Stop conditions.

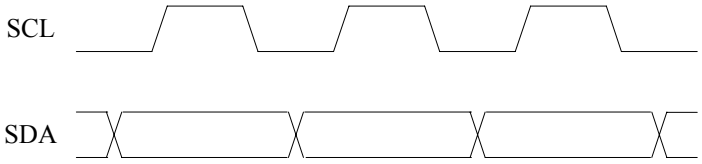


Fig 11-1 I2C-Bus Data Transmission

An “H” to “L” transition on SDA line while SCL is “H” indicates a Start condition. An “L” to “H” transition on SDA line while SCL is “H” defines a Stop condition. Start and Stop conditions are always generated by master (refer to the figure below). The bus is considered to be busy after Start condition. The bus is considered to be free again a certain time after the stop condition.

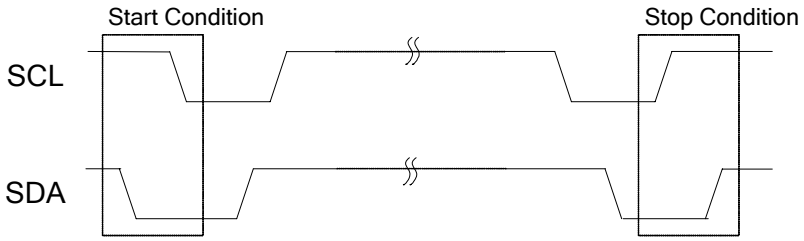


Fig 11-2 I2C-Bus Start and Stop Condition

11.2 I2C-Bus Data Transmission and its Acknowledge

After start condition, data is transmitted by 1byte (8bits). The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit.
Data transmission with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmitter releases SDA line during the acknowledge clock pulse.
The receiver must pull down SDA line during the acknowledge clock pulse so that SDA line remains stable "L" during the "H" period of the acknowledge clock pulse.
If a master–receiver is involved in a transfer, it must signal the end of the data to the slave-transmitter by not generating acknowledge on the last byte that was clocked out of the slave. The slave-transmitter must release the data line to allow the master to generate a Stop condition.

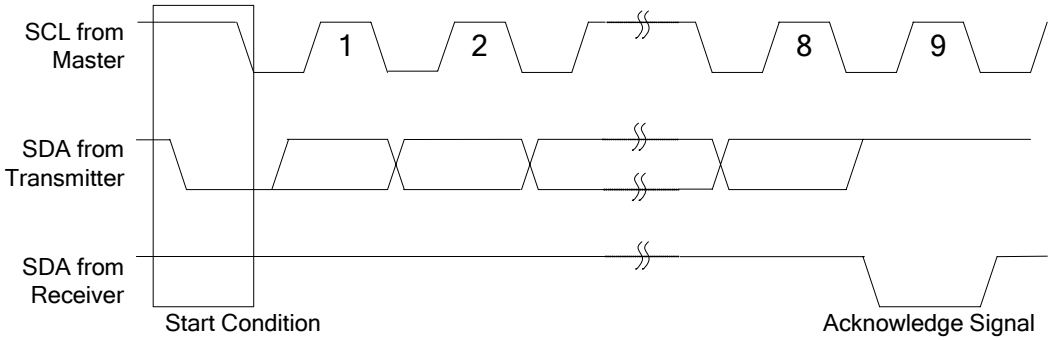


Fig 11-3 I2C-Bus Data Transmission and its Acknowledge

11.3 I2C-Bus Slave Address

After Start condition, a slave address is sent. The address is 7 bits long followed by an 8th bit which is data direction bit (Read/Write). The slave address of RN5T614 is specified at "0110010b".

	A7	A6	A5	A4	A3	A2	A1
Setting value	0	1	1	0	0	1	0

A7～A1: Slave Address

Table 11-1 Slave Address of RN5T614

11.4 I2C-Bus Data Transmission Read Format

In order to read the internal register data:

- Specify an internal address pointer (8bit).
- Generate the repeated Start condition to change the data transmission direction to read.

With a Start of read mode, automatic increment in address pointers will be made. Read-mode is repeated until Stop condition is initiated.

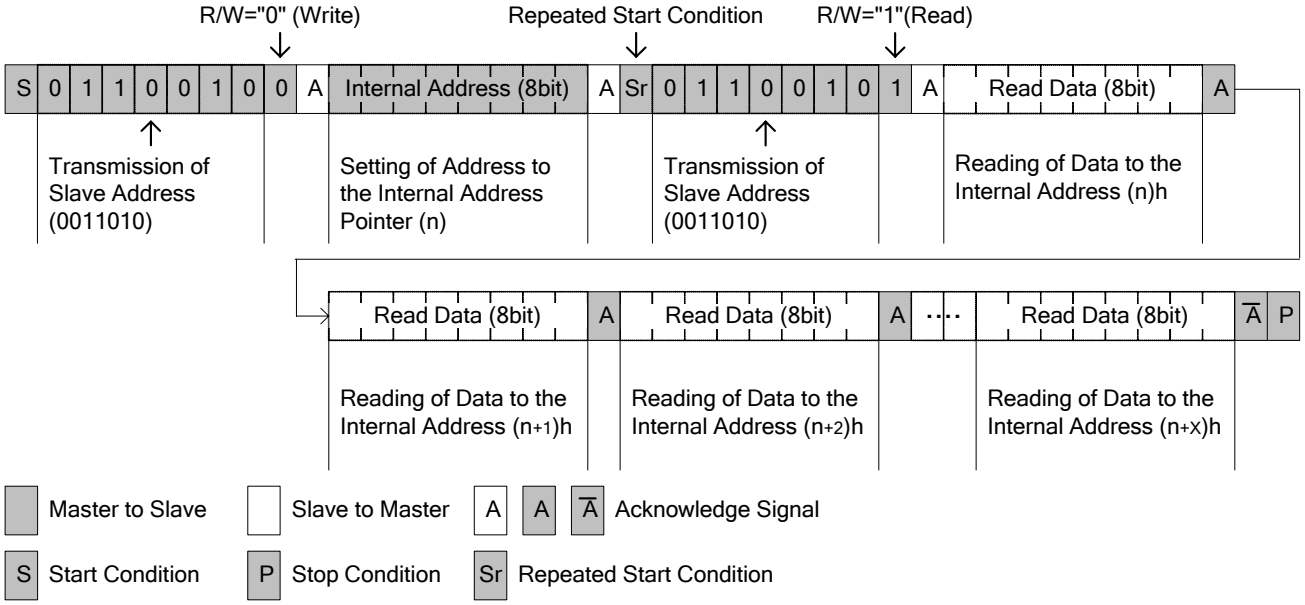


Fig 11-4 I2C-Bus Data Transmission Read Format

11.5 I2C-Bus Data Transmission Write Format

The transmission format for the slave address allocated to each IC is defined by I2C-Bus standard. However transmission method of address information of each IC is not defined. RN5T614 transmits command data. For the data transmission, please transmit MSB first from Master and following data in sequence.

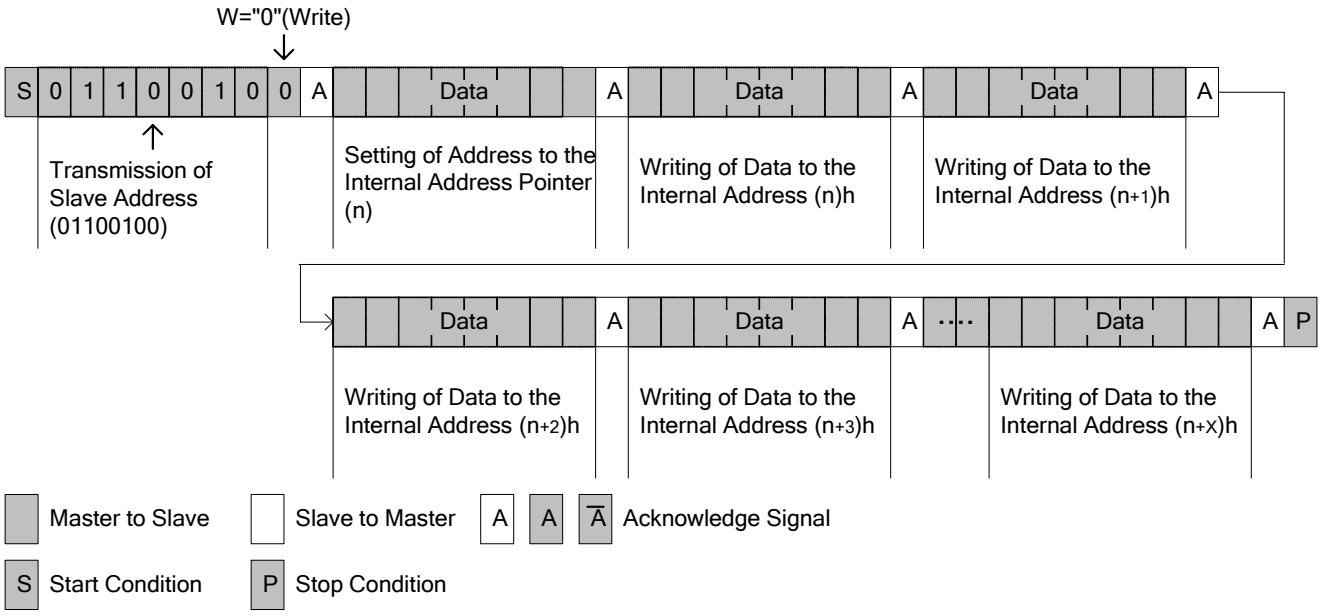


Fig 11-5 I2C-Bus Data Transmission Write Format

11.6 I2C-Bus Internal Register Write-in Timing

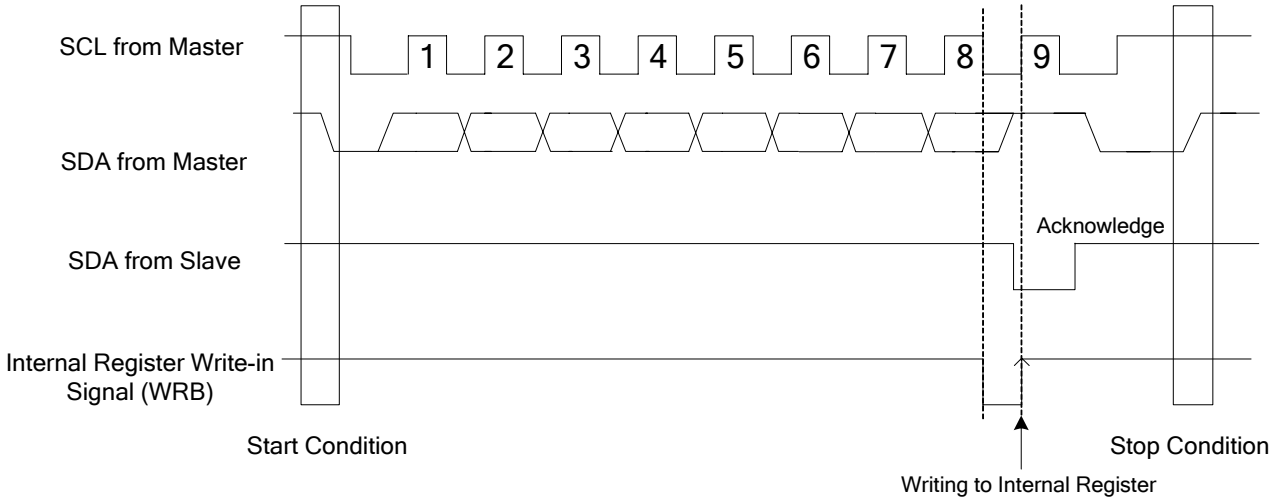


Fig 11-6 I2C-Bus Internal Register Write-in Timing

11.7 AC Characteristics of I2C-Bus

Operating Conditions (unless otherwise specified) VDDIO = 1.7～3.4V, T_a = 25 degrees C

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	-			400	kHz
t_{BUF}	Bus Free Time Between a Precedent and Start	-	1.3		-	µs
t_{Low}	SCL Clock "L" Time	-	1.3		-	µs
t_{HIGH}	SCL Clock "H" Time	-	0.6		-	µs
$t_{SU;STA}$	Start Condition Setup Time	-	0.6		-	µs
$t_{HD;STA}$	Start Condition Hold Time	-	0.6		-	µs
$t_{SU;STO}$	Stop Condition Setup Time	-	0.6		-	µs
$t_{HD;DAT}$	Data Hold Time	-	0			µs
$t_{SU;DAT}$	Data Setup Time	-	100 (*1)		-	ns
t_R	Rising Time of SCL and SDA (Input)	-			300	ns
t_F	Falling Time of SCL and SDA (Input)	-			300	ns

Table 11-2 I2C-Bus AC Characteristics

Note*: All the above-mentioned values are corresponding to V_{IH} min and V_{IL} max level.

Note*1: Standard mode is allowed in I2C-bus standard. For Standard mode, it needs to satisfy the condition; $t_{SU;DAT}$>=250ns.

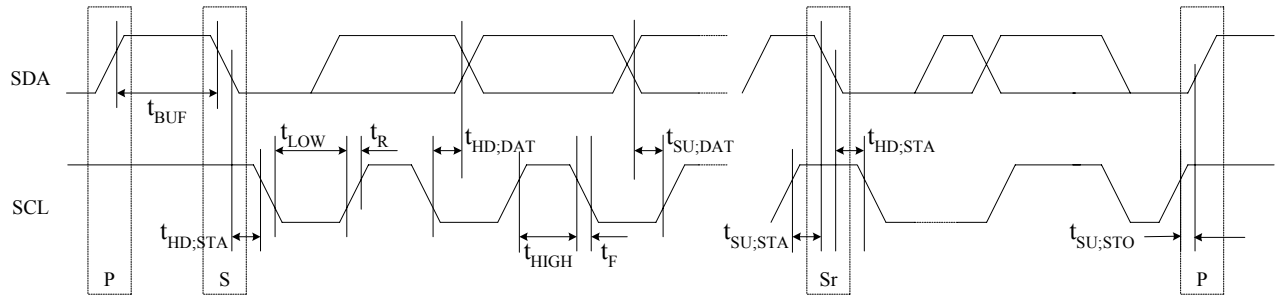


Fig 11-7 I2C-Bus Interface Timing Chart

12. Registers

	Address	Register	R/W	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Initial value (*1)
Power Control	00	PCCNT	R/W	---	---	---	---	---	---	---	SLEEP	0000 0000
	01	PCST	R	---	---	---	---	---	---	EXTONMON	PWRONMON	0000 00--
DET	02	VDCTRL	R/W	---	VD2SEL[2:0]			---	---	VD1SEL[1:0]		011* 0010
LDO	03	LDOON	R/W	---	LDO7ON	LDO6ON	LDO5ON	LDO4ON	LDO3ON	LDO2ON	---	000* **10
	04	LDO2DAC	R/W	---	---	---	---	---	LDO2DAC[2:0]			0000 0011
	05	LDO3DAC	R/W	---	---	---	---	---	LDO3DAC[2:0]			0000 0011
	06	LDO4DAC	R/W	---	---	---	---	---	LDO4DAC[2:0]			0000 0110
	07	LDO5DAC	R/W	---	---	---	---	---	LDO5DAC[2:0]			0000 0*0*
	08	LDO6DAC	R/W	---	---	---	---	---	LDO6DAC[2:0]			0000 0011
	09	LDO7DAC	R/W	---	---	---	---	---	LDO7DAC[2:0]			0000 0110
	0A	LDO8DAC	R/W	---	---	---	---	---	LDO8DAC[2:0]			0000 011*
	0B	---	---	---	---	---	---	---	---	---	---	---- ----
	0C	---	---	---	---	---	---	---	---	---	---	---- ----
	0D	---	---	---	---	---	---	---	---	---	---	---- ----
	0E	---	---	---	---	---	---	---	---	---	---	---- ----
	0F	---	---	---	---	---	---	---	---	---	---	---- ----
DCDC	10	DDCTL1	R/W	---	---	---	---	---	DD3ON	DD2ON	DD1ON	0000 0100
	11	DDCTL2	R/W	---	---	---	---	---	---	DD2DIS	DD1DIS	0000 0011
	12	RAMP1CTL	R/W	---	---	RAMP1SLOP[1:0]		DD1MODE[1:0]		DD1ENCTL	---	0001 1000
	13	RAMP2CTL	R/W	---	---	RAMP2SLOP[1:0]		DD2MODE[1:0]		DD2ENCTL	---	0001 1000
	14	DD1DAC	R/W	---	DD1DAC[6:0]							00** ***0
	15	DD2DAC	R/W	---	DD2DAC[6:0]							0*** **00
	16	---	---	---	---	---	---	---	---	---	---	---- ----
	17	---	---	---	---	---	---	---	---	---	---	---- ----
	18	---	---	---	---	---	---	---	---	---	---	---- ----
	19	---	---	---	---	---	---	---	---	---	---	---- ----
	1A	---	---	---	---	---	---	---	---	---	---	---- ----
	1B	---	---	---	---	---	---	---	---	---	---	---- ----
	1C	---	---	---	---	---	---	---	---	---	---	---- ----
	1D	---	---	---	---	---	---	---	---	---	---	---- ----
	1E	---	---	---	---	---	---	---	---	---	---	---- ----
	1F	---	---	---	---	---	---	---	---	---	---	---- ----
CHARGER	20	CHGSTART	R/W	---	---	---	---	---	---	---	CHGSTART	0000 0001
	21	FET1CNT	R/W	---	---	---	---	ILIM[3:0]				0000 **0*
	22	FET2CNT	R/W	---	CVSET[1:0]		---	ICHGSET[3:0]				0000 **00
	23	TSET	R/W	---	---	TEMPSET[1:0]		RTIMSET[1:0]		---	---	0010 0000
	24	CMPSET	R/W	---	---	---	---	---	CMPSET[2:0]			0000 0000
	25	SUSPEND	R/W	---	---	---	CRCC2	---	---	---	SUSPENDB	0000 0001
	26	CHGSTATE	R	---	---	---	---	RDSTATE[3:0]				0000 0000
	27	---	---	---	---	---	---	---	---	---	---	---- ----
INTC	28	CHGEN1	R/W	EN_VBOV	EN_VCOV	EN_NOBATT	---	---	EN_VBTERR	EN_DIEOT	EN_ADPDET	0000 0001
	29	CHGIR1	R/W	IR_VBOV	IR_VCOV	IR_NOBATT	---	---	IR_VBTERR	IR_DIEOT	IR_ADPDET	0000 0000
	2A	CHGMONI	R	MON_VBOV	MON_VCOV	MON_NOBATT	---	---	MON_VBTERR	MON_DIEOT	MON_ADPDET	---0 0---
	2B	---	---	---	---	---	---	---	---	---	---	---- ----
	2C	CHGEN2	R/W	---	---	---	EN_TIMEOUT	EN_CHGCMP	EN_STRC	---	EN_STCR	0000 0000
	2D	CHGIR2	R/W	---	---	---	IR_TIMEOUT	IR_CHGCMP	IR_STRC	---	IR_STCR	0000 0000
	2E	---	---	---	---	---	---	---	---	---	---	---- ----
	2F	---	---	---	---	---	---	---	---	---	---	---- ----

Note*: Do not set "1" to reserved bits. Do not write "1" or "0" to undefined registers.

Note*1: Reset condition of register:

- PCCNT register (00h) and CHGIR1-2 registers (29h, 2Dh) are reset by UVLO or TSHUT.
- When VCHG power supply is turned off, CHARGER's registers (20h-26h) and CHGIR1-2 registers (29h, 2Dh) except IR_ADPDET bit are cleared.
- Other registers are reset by RESETO="L".

  Also, when DC/DC1(2) turns off, DD1(2)MODE[1:0] bits and DD1(2)DAC[6:0] bits are reset.

"*" selected by trimming .

12.1 Power Control

12.1.1 PCCNT: Power Control Register (Address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	SLEEP
R/W	R	R	R	R	R	R	R	R/W
Default	0	0	0	0	0	0	0	0

Bit 0: SLEEP bit

"0": Stand-by Operation is invalid

"1": Stand-by Operation is valid

Note*: SLEEP bit is reset by UVLO or THSUT.

12.1.2 PCST: Power Control Status Register (Address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	EXTON MON	PWRON MON
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	-	-

Bit 1: EXTON pin input monitor bit

"0": EXTON="L"

"1": EXTON="H"

Bit 0: PWRON pin input monitor bit

"0": PWRON="L"

"1": PWRON="H"

12.2 Voltage Detector

12.2.1 VDCTRL: Detection Circuit Control Register (Address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	VD2SEL[2:0]			-	-	VD1SEL[1:0]	
R/W	R	R/W	R/W	R/W	R	R	R/W	R/W
Default	0	1	1	1	0	0	1	0

Bit 6 ～ Bit 4: VD2SEL [2:0] bit

The release voltage setting of VD2

The release voltage table of VD2

VD2SEL [2:0]	Release voltage [V]
000 (0h)	Prohibit
001 (1h)	1.53
010 (2h)	2.13
011 (3h)	2.21
100 (4h)	2.38
101 (5h)	2.42
110 (6h)	2.55
111 (7h)	**2.81 (Default)**

Note*: Initial value selected by trimming (2.55V or 2.81V)

Note*: Hysteresis of VD2 is 100mV.

The detection voltage is determined by this register setting.

Bit 1 ～ Bit 0: VD1SEL[1:0] bit

The release voltage setting of VD1

The release voltage table of VD1

VD1SEL [1:0]	Release voltage [V]
00 (0h)	3.1
01 (1h)	3.2
10 (2h)	**3.3 (Default)**
11 (3h)	3.5

Note*: Hysteresis of VD1 is 0.2V.

The detection voltage is determined by this register setting.

12.3 Regulator

12.3.1 LDOON: LDO Output Control Register (Address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	LDO7ON	LDO6ON	LDO5ON	LDO4ON	LDO3ON	LDO2ON	-
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	1	1	1	1	0

Bit 7-1: LDOnON bit (n=2, 3, 4, 5, 6, 7)

LDOn on/off control bit

"0": off

"1": on

Note*: Initial value selected by trimming (LDO3, 4, 5)

12.3.2 LDO2DAC: LDO2 Output Voltage Control Register (Address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO2DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

Bit 2 ～ Bit 0: LDO2DAC [2:0] bit

Set the output voltage to LDO2

The output voltage table of LDO2

LDO2DAC [2:0]	Output voltage [V]
000 (00h)	0.90
001 (01h)	1.00
010 (02h)	1.10
011 (03h)	**1.20 (Default)**
100 (04h)	1.30
101 (05h)	Prohibit
110 (06h)	Prohibit
111 (07h)	Prohibit

12.3.3 LDO3DAC: LDO3 Output Voltage Control Register (Address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO3DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

Bit 2 ～ Bit 0: LDO3DAC [2:0] bit

Set the output voltage to LDO3

The output voltage table of LDO3

LDO3DAC [2:0]	Output voltage [V]
000 (00h)	0.90
001 (01h)	1.00
010 (02h)	1.10
011 (03h)	**1.20 (Default)**
100 (04h)	1.30
101 (05h)	Prohibit
110 (06h)	Prohibit
111 (07h)	Prohibit

12.3.4 LDO4DAC: LDO4 Output Voltage Control Register (Address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO4DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	0

Bit 2 ～ Bit 0: LDO4DAC [2:0] bit

Set the output voltage to LDO4

The output voltage table of LDO4

LDO4DAC [2:0]	Output voltage [V]
000 (00h)	1.80
001 (01h)	2.50
010 (02h)	2.60
011 (03h)	2.80
100 (04h)	2.85
101 (05h)	3.00
110 (06h)	**3.30 (Default)**
111 (07h)	Prohibit

12.3.5 LDO5DAC: LDO5 Output Voltage Control Register (Address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO5DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 2 ～ Bit 0: LDO5DAC [2:0] bit

Set the output voltage to LDO5

The output voltage table of LDO5

LDO5DAC [2:0]	Output voltage [V]
000 (00h)	**1.80 (Default)**
001 (01h)	2.50
010 (02h)	2.60
011 (03h)	2.80
100 (04h)	2.85
101 (05h)	3.00
110 (06h)	3.30
111 (07h)	Prohibit

Note*: Initial value selected by trimming (3.0V or 1.8V)

12.3.6 LDO6DAC: LDO6 Output Voltage Control Register (Address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO6DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	1	1

Bit 2 ～ Bit 0: LDO6DAC [2:0] bit

Set the output voltage to LDO6

The output voltage table of LDO6

LDO6DAC [2:0]	Output voltage [V]
000 (00h)	1.20
001 (01h)	1.80
010 (02h)	2.50
011 (03h)	**2.60 (Default)**
100 (04h)	2.80
101 (05h)	2.85
110 (06h)	3.00
111 (07h)	3.30

12.3.7 LDO7DAC: LDO7 Output Voltage Control Register (Address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO7DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	0

Bit 2 ～ Bit 0: LDO7DAC [2:0] bit

Set the output voltage to LDO7

The output voltage table of LDO7

LDO7DAC [2:0]	Output voltage [V]
000 (00h)	1.20
001 (01h)	1.80
010 (02h)	2.50
011 (03h)	2.60
100 (04h)	2.80
101 (05h)	2.85
110 (06h)	**3.00 (Default)**
111 (07h)	3.30

12.3.8 LDO8DAC: LDO8 Output Voltage Control Register (Address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	LDO8DAC [2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	1	1	1

Bit 2 ～ Bit 0: LDO8DAC [2:0] bit

Set the output voltage to LDO8

The output voltage table of LDO8

LDO8DAC [2:0]	Output voltage [V]
000 (00h)	Prohibit
001 (01h)	1.80
010 (02h)	2.50
011 (03h)	2.60
100 (04h)	2.80
101 (05h)	2.85
110 (06h)	3.00
111 (07h)	**3.30 (Default)**

Note*: Initial value selected by trimming (3.0V or 3.3V)

12.3.9 DDCTL1: DC/DC Control Register1 (Address 10h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	DD3ON	DD2ON	DD1ON
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	0

Bit 2-0: DDnON bit (n=1,2,3)

DC/DCn on/off bit

"0": off

"1": on

12.3.10 DDCTL2: DC/DC Control Register2 (Address 11h)

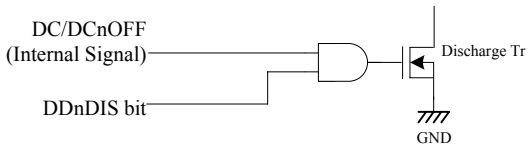
Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	DD2DIS	DD1DIS
R/W	R	R	R	R	R	R	R/W	R/W
Default	0	0	0	0	0	0	1	1

Bit 2-0: DDnDIS bit (n=1, 2)

DC/DCn Discharge control bit

"0": off

"1": on (This bit is invalid when DC/DCn state is on.)



12.3.11 RAMP1CTL: DC/DC1 RAMP Control Register (Address 12h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	RAMP1SLOP [1:0]		DD1MODE [1:0]		DD1ENCTL	-
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	1	1	0	0	0

Bit 5-4: RAMP1SLOP [1:0] bit

DC/DC1 RAMP up/down slope setting bit

RAMP1SLOP[1:0]	Voltage Slope
00	15 mV /µs
01	**30 mV /µs (Default)**
10	60 mV /µs
11	Prohibit

Bit 3-2: DD1MODE bit

DC/DC1 AUTO(PWM/PFM) / PWM / PSM mode setting bit

DD1MODE [1:0]	Operation Mode
00	PSM
01	PWM
10	**AUTO (Default)**
11	AUTO

DD1MODE bit is reset when DC/DC1 turns off and changed to AUTO mode.

Bit 1: DD1ENCTL bit

DC/DC1 Control select bit

"0": DCDCEN12 pin is valid

"1": DD1ON bit is valid

12.3.12 RAMP2CTL: DC/DC2 RAMP Control Register (Address 13h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	RAMP2SLOP [1:0]		DD2MODE [1:0]		DD2ENCTL	-
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R
Default	0	0	0	1	1	0	0	0

Bit 5-4: RAMP2SLOP [1:0] bit

DC/DC2 RAMP up/down slope setting bit

RAMP2SLOP[1:0]	Voltage Slope
00	15 mV /μs
01	**30 mV /μs (Default)**
10	60 mV /μs
11	Prohibit

Bit 3-2: DD2MODE bit

DC/DC2 AUTO(PWM/PFM)/PWM / PSM mode setting bit

DD2MODE [1:0]	Operation Mode
00	PSM
01	PWM
10	**AUTO (Default)**
11	AUTO

DD2MODE bit is reset when DC/DC2 turns off and changed to AUTO mode.

Bit 1: DD2ENCTL bit

DC/DC2 Control select bit

"0": DCDCEN12 pin is valid

"1": DD2ON bit is valid

12.3.13 DD1DAC: DC/DC1 Output Voltage Control Register (Address 14h)

DD1DAC (14h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	DD1DAC [6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	1	0	0	0

Note*: The register value is reset when DC/DC1 turns off. (Initial value selected by trimming)

The output voltage table of DC/DC1 (Step=12.5mV)

DD1DAC [6:0]	Output voltage [V]
0000000 (00h)	0.9000
0000001 (01h)	0.9125
0000010 (02h)	0.9250
~	~
0001000 (08h)	1.00
~	~
0010000 (10h)	1.10
~	~
0011000 (18h)	**1.20 (Default)**
~	~
0011100 (1Ch)	1.25
~	~
0100000 (20h)	1.3
~	~
0101010 (2Ah)	1.4250
~	~
0101110 (2Eh)	1.4750
0101111 (2Fh)	1.4875
0110000 (30h)	1.5000
~	Prohibit
1111111 (7Fh)	Prohibit

12.3.14 DD2DAC: DC/DC2 Output Voltage Control Register (Address 15h)

DD2DAC (15h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	DD2DAC [6:0]						
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	1	0	1	0	0

Note*: The register value is reset when DC/DC2 turns off. (Initial value selected by trimming)

The output voltage table of DC/DC2 (Step=12.5mV)

DD2DAC [6:0]	Output voltage [V]
0000000 (00h)	0.9000
0000001 (01h)	0.9125
0000010 (02h)	0.9250
~	~
0000100 (04h)	0.95
~	~
0001100 (0Ch)	1.05
~	~
0010100 (14h)	**1.15 (Default)**
~	~
0011000 (18h)	1.20
~	~
0101110 (2Eh)	1.4750
0101111 (2Fh)	1.4875
0110000 (30h)	1.5000
~	Prohibit
1001000 (48h)	1.8
~	Prohibit
1111111 (7Fh)	Prohibit

12.4 Li-ion Battery Charger

12.4.1 CHGSTART: Charging Start Setting Register (Address 20h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	CHGSTART
R/W	R	R	R	R	R	R	R	R/W
Default	0	0	0	0	0	0	0	1

Bit 0: CHGSTART bit

Battery Charging enables

"0": Disable charging

"1": Enable charging (default)

12.4.2 FET1CNT: SW1 Limit Current Setting Register (Address 21h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	ILIM[3:0]			
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	1

Bit 3 ～ Bit 0: ILIM bit

SW1 Limit Current Selection

Control Bit				SW1 Limit Current [mA]
D3	D2	D1	D0	
0	0	0	0	120
0	0	0	1	240
0	0	1	0	360
0	0	1	1	480
0	1	0	0	600
0	**1**	**0**	**1**	**720 (default)**
0	1	1	0	840
0	1	1	1	960
1	0	0	0	1080
other				1200

Note*: Initial value selected by trimming (120mA or 720mA or 1200mA)

12.4.3 FET2CNT: SW2 Control Setting Register (Address 22h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	CVSET[1:0]		-	ICHGSET[3:0]			
R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	1	0	0

Bit 6 ～ Bit 5: CVSET bit

Battery Charge Voltage Selection

Control Bit		Charge voltage [V]
D1	D0	
0	**0**	**4.2 (default)**
0	1	4.12
1	0	4.07
1	1	4.07

Bit 3 ～ Bit 0: ICHGSET bit

Rapid Current Selection

Control Bit				Rapid Current [mA]
D3	D2	D1	D0	
0	0	0	0	100
0	0	0	1	200
0	0	1	0	300
0	0	1	1	400
0	**1**	**0**	**0**	**500 (default)**
0	1	0	1	600
0	1	1	0	700
0	1	1	1	800
other				900

Note*: Initial value selected by trimming (100mA or 500mA or 900mA)

12.4.4 TSET: Temperature and Charging Timer Setting Register (Address 23h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	TEMPSET[1:0]		RTIMSET[1:0]		-	-
R/W	R	R	R/W	R/W	R	R	R	R
Default	0	0	1	0	0	0	0	0

Bit 5 ～ Bit 4: TEMPSET bit

Die over temperature threshold value selection

Control Bit		Die Temperature [degrees C]	
D5	D4	Detection	Recovery
0	0	105	85
0	1	115	95
1	**0**	**125（default）**	**105**
1	1	135	115

Bit 3 ～ Bit 2: RTIMSET bit

Rapid Timer setting

Control Bit		Rapid Timer [min]
D3	D2	
0	**0**	**120 (default)**
0	1	180
1	0	240
1	1	300

12.4.5 CMPSET: Charge Complete Current Setting Register (Address 24h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	CMPSET[2:0]		
R/W	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 2 ～ Bit 0: CMPSET bit

Charge complete Current selection

Control Bit			Charge Complete Current [mA]
D2	D1	D0	
0	**0**	**0**	**25 (default)**
0	0	1	50
0	1	0	75
0	1	1	100
1	0	0	125
1	0	1	150
1	1	0	175
1	1	1	200

12.4.6 SUSPEND: Charge Ready Current / Suspend Setting Register (Address 25h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	CRCC2	-	-	-	SUSPENDB
R/W	R	R	R	R/W	R	R	R	R/W
Default	0	0	0	0	0	0	0	1

Bit 4: CRCC2 bit

Charge Ready Current Selection

"0": 0mA (default)

"1": 10mA

In Charge-Ready state, if the power source switches from the adapter to the battery, the transient under-shoot might appear on VSYS pin because SW2 is fully off.

This under-shoot is able to be reduced by setting "1" to CRCC2 as SW2 is on even in Charge-Ready state.

Bit 0: SUSPENDB bit

Suspend Selection

"0": Suspend

"1": Not suspend (default)

(This bit is automatically set depending on the charge state).

SUSPENDB bit is set to "1" automatically and unable to set to "0" except when the state is Charge-Off, Adapter-Over-Voltage, SUSPEND, Charge-Ready, Trickle-Charge, Rapid-Charge and Charge-Complete.

12.4.7 CHGSTATE: Current Charger State Register (Address 26h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	RDSTATE[3:0]			
R/W	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0

Bit 0 ～ Bit 3: RDSTATE bit

Charger current state (read only)

Control Bit				Charger current state
D3	D2	D1	D0	
0	0	0	0	Charge-Off
0	0	0	1	Charge-Ready
0	0	1	0	-
0	0	1	1	-
0	1	0	0	Rapid-Charge
0	1	0	1	Charge-Complete
0	1	1	0	Battery-Error
0	1	1	1	Battery-Over-Voltage
1	0	0	0	Adapter-Over-Voltage
1	0	0	1	No-Battery
1	0	1	0	Battery-Temperature-Error
1	0	1	1	SUSPEND
other				-

12.5 Interrupt Controller

12.5.1 CHGEN1: Charge Interrupt Request Output Enable Register (Address 28h)

Bit	7	6	5	4	3	2	1	0
Symbol	EN_VBOV	EN_VCOV	EN_NOBATT	-	-	EN_VBTERR	EN_DIEOT	EN_ADPDET
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	1

Bit 7: EN_VBOV bit

Battery over voltage interrupt enable (VVBAT > 4.6V)

"0": Disable

"1": Enable

Bit 6: EN_VCOV bit

Adapter over voltage interrupt enable (VVCHG>6.2V)

"0": Disable

"1": Enable

Bit 5: EN_NOBATT bit

No Battery detect interrupt enable

"0": Disable

"1": Enable

Bit 2: EN_VBTERR bit

Battery abnormal temperature interrupt enable

"0": Disable

"1": Enable

Bit 1: EN_DIEOT bit

Die abnormal temperature by SW1 or SW2 in charger interrupt enable

"0": Disable

"1": Enable

Bit 0: EN_ADPDET bit

Adapter insert & remove interrupt enable

"0": Disable

"1": Enable

12.5.2 CHGIR1: Charge Interrupt Request Register (Address 29h)

Bit	7	6	5	4	3	2	1	0
Symbol	IR_VBOV	IR_VCOV	IR_NOBATT	-	-	IR_VBTERR	IR_DIEOT	IR_ADPDET
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Bit 7: IR_VBOV bit

Battery over voltage (VVBAT > 4.6V)

"0": None

"1": Requested

Bit 6: IR_VCOV bit

Adapter over voltage (VVCHG>6.2V)

"0": None

"1": Requested

Bit 5: IR_NOBATT bit

No Battery detect

"0": None

"1": Requested

Bit 2: IR_VBTERR bit

Battery abnormal temperature

"0": None

"1": Requested

Bit 1: IR_DIEOT bit

Die abnormal temperature by SW1 or SW2 in charger

"0": None

"1": Requested

Bit 0: IR_ADPDET bit

Adapter insert & remove

"0": None

"1": Requested

Note*: Each bit can be cleared by writing "0", but cannot be set by writing "1".

These bits are not cleared by RESETO="L".

These bits are cleared by UVLO or TSHUT.

Also, these bits are cleared when VCHG power supply is turned off.

12.5.3 CHGMONI: Charge Interrupt Monitor Signal Read Register (Address 2Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	MON_ VBOV	MON_ VCOV	MON_ NOBATT	-	-	MON_ VBTERR	MON_ DIEOT	MON_ ADPDET
R/W	R	R	R	R	R	R	R	R
Default	-	-	-	0	0	-	-	-

Bit 7: MON_VBOV bit

Battery over voltage (VVBAT > 4.6V) (Read Current Value)

"0": Normal voltage

"1": Over voltage

Bit 6: MON_VCOV bit

Adapter over voltage (VVCHG>6.2V) (Read Current Value)

"0": Normal voltage

"1": Over voltage

Bit 5: MON_NOBATT bit

No Battery detect (Read Current Value)

"0": Battery is connected

"1": Battery has come off

Bit 2: MON_VBTERR bit

Battery abnormal temperature (Read Current Value)

"0": Normal temperature

"1": Abnormal temperature

Bit 1: MON_DIEOT bit

Die abnormal temperature by SW1 or SW2 in charger (Read Current Value)

"0": Normal temperature

"1": Abnormal temperature

Bit 0: MON_ADPDET bit

Adapter insert & remove (Read Current Value)

"0": Adapter has come off

"1": Adapter is connected

12.5.4 CHGEN2: Charge Interrupt Request Output Enable Register (Address 2Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	EN_TIMEOUT	EN_CHGCMP	EN_STRC	-	EN_STCR
R/W	R	R	R	R/W	R/W	R/W	R	R/W
Default	0	0	0	0	0	0	0	0

Bit 4: EN_TIMEOUT bit

Timer time out interrupt enable

"0": Disable

"1": Enable

Bit 3: EN_CHGCMP bit

Charge complete interrupt enable

"0": Disable

"1": Enable

Bit 2: EN_STRC bit

Shift to Rapid-Charge state interrupt enable

"0": Disable

"1": Enable

Bit 0: EN_STCR bit

Shift to Charge-Ready state interrupt enable

"0": Disable

"1": Enable

12.5.5 CHGIR2: Charge Interrupt Request Register (Address 2Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	IR_TIMEOUT	IR_CHGCMP	IR_STRC	-	IR_STCR
R/W	R	R	R	R/W	R/W	R/W	R	R/W
Default	0	0	0	0	0	0	0	0

Bit 4: IR_TIMEOUT bit

Timer time out

"0": None

"1": Requested

Bit 3: IR_CHGCMP bit

Charge complete

"0": None

"1": Requested

Bit 2: IR_STRC bit

Shift to Rapid-Charge state

"0": None

"1": Requested

Bit 0: IR_STCR bit

Shift to Charge-Ready state

"0": None

"1": Requested

Note*: Each bit can be cleared by writing "0", but cannot be set by writing "1".

These bits are not cleared by RESETO="L".

These bits are cleared by UVLO or TSHUT.

Also, these bits are cleared when VCHG power supply is turned off.

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Exposure to the condition exceeded Absolute Maximum Ratings may cause the permanent damages and affects the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

$VDD=V_{IN}$, V_{DDIO}

Symbol	Parameter	Condition	Rated value	Units
V_{IN}	Power Supply Voltage	VIN1-3 pins	-0.3～6.0	V
V_{VSYS}	Power Supply Voltage	VSYS1-2 pins	-0.3～6.0	V
V_{VCHG}	Power Supply Voltage	VCHG1-2 Pins	-0.3～6.5	V
V_{DDIO}	Power Supply Voltage	VDDIO pin	-0.3～4.5	V
Vin	Input Voltage Range	All Input Pins	-0.3～VDD+0.3	V
Vout	Output Voltage Range		-0.3～VDD+0.3	V
PD	Package Allowable Dissipation	JEDEC substrate mounting state, Wind velocity 0m/s Ta=25degrees C Linear derating coefficient = 0.03 W/ degrees C	3.0	W
T_{stg}	Storage Temperature	-	-55～+125	degrees C
Tj	Junction Temperature		125	degrees C

Table 13-1 Absolute Maximum Ratings

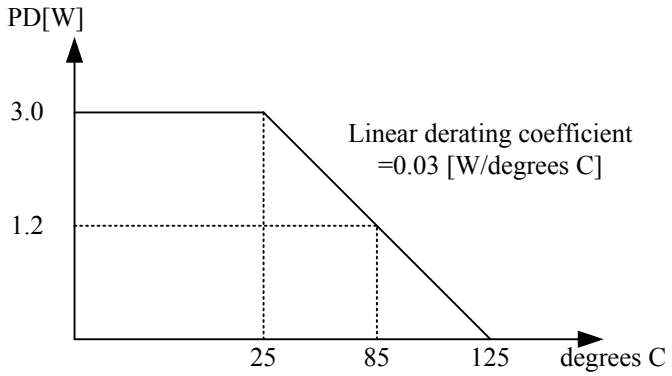


Fig 13-1 Maximum Package Allowable Dissipation

13.2 Recommendation of Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Power Supply Voltage	VIN1-3 pins	3.1	3.6	5.5	V
V_{VSYS}	Power Supply Voltage	VSYS1-2 pins	4.65	4.8	4.95	V
V_{VCHG}	Power Supply Voltage	VCHG1-2 Pins	4.5	5.0	5.5	V
V_{DDIO}	Power Supply Voltage	VDDIO pin	1.7		3.4	V
Ta	Temperature of Operation	-	-40		+85	degrees C

Table 13-2 Recommendation of Operation Conditions

13.3 DC Characteristics

Digital part I/O

Operating Conditions (unless otherwise specified) T_a = 25 degrees C, VDD = V_{IN}/V_{DDIO}

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	"H" input voltage (CMOS)	Pin=DCDCEN12, DCDCEN3	VDD×0.7			V
V_{IL}	"L" input voltage (CMOS)	Pin=DCDCEN12, DCDCEN3			VDD×0.3	V
V_{IH1}	"H" input rising threshold voltage1 (CMOS Schmitt)	Pin=PWRON,EXTON,PSHOLD	VDD×0.5		VDD×0.8	V
V_{IL1}	"L" input rising threshold voltage1 (CMOS Schmitt)	Pin=PWRON,EXTON, PSHOLD	VDD×0.2		VDD×0.5	V
V_{HIS1}	Schmitt hysteresis voltage1	Pin=PWRON,EXTON, PSHOLD	VDD×0.15			V
V_{IH2}	"H" input rising threshold voltage2 (CMOS Schmitt)	Pin=SCL, SDA			VDD×0.7	V
V_{IL2}	"L" input rising threshold voltage2 (CMOS Schmitt)	Pin=SCL, SDA	VDD×0.3			V
V_{HIS2}	Schmitt hysteresis voltage2 (SCL, SDA)	VDD>2.0V	VDD×0.05			V
		VDD<2.0V	VDD×0.1			
V_{OL1}	"L" Output Voltage1	I_{OL}= 2mA, Pin=ONOB, BATDET, RESETO, INTB			0.4	V
V_{OL2}	"L" Output Voltage2 (SDA)	I_{OL}= 3mA			0.4	V
		I_{OL}= 6mA			0.6	V
I_{IL}	Input Leakage Current	VIN=0～VDD	-3		3	µA
I_{OZ}	Off Leakage Current	VIN=0～VDD, Pin=ONOB, BATDET, RESETO, INTB	-3		3	µA

Table 13-3 DC Characteristics

Consumption Current

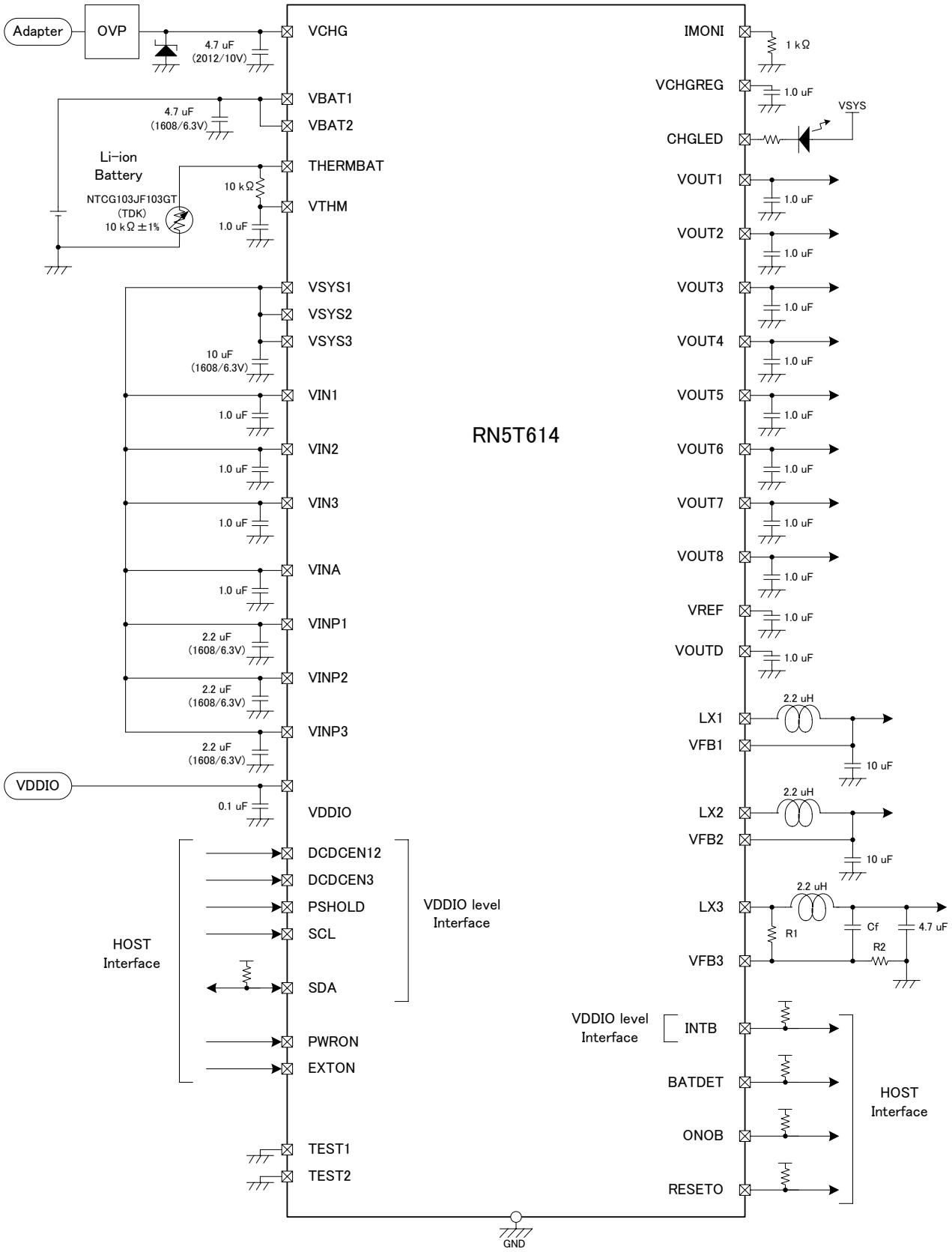
Operating Conditions (unless otherwise specified) T_a = 25 degrees C, V_{IN} =3.6V, No-load

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{ST1}	Standby current1	Not powered – on (UVLO,VD1,LDO1,LDODIG=ON)		5		µA
I_{ST2}	Standby current2	powered – on (Standby mode) (UVLO,VD1,2,VREF,LDO1,LDODIG,DCDC3,TSHUT=ON)		100		µA
I_{OP}	Operating current1	powered – on (Normal mode) (LDO,DC/DC = all ON)		320		µA

Table 13-4 Consumption Current

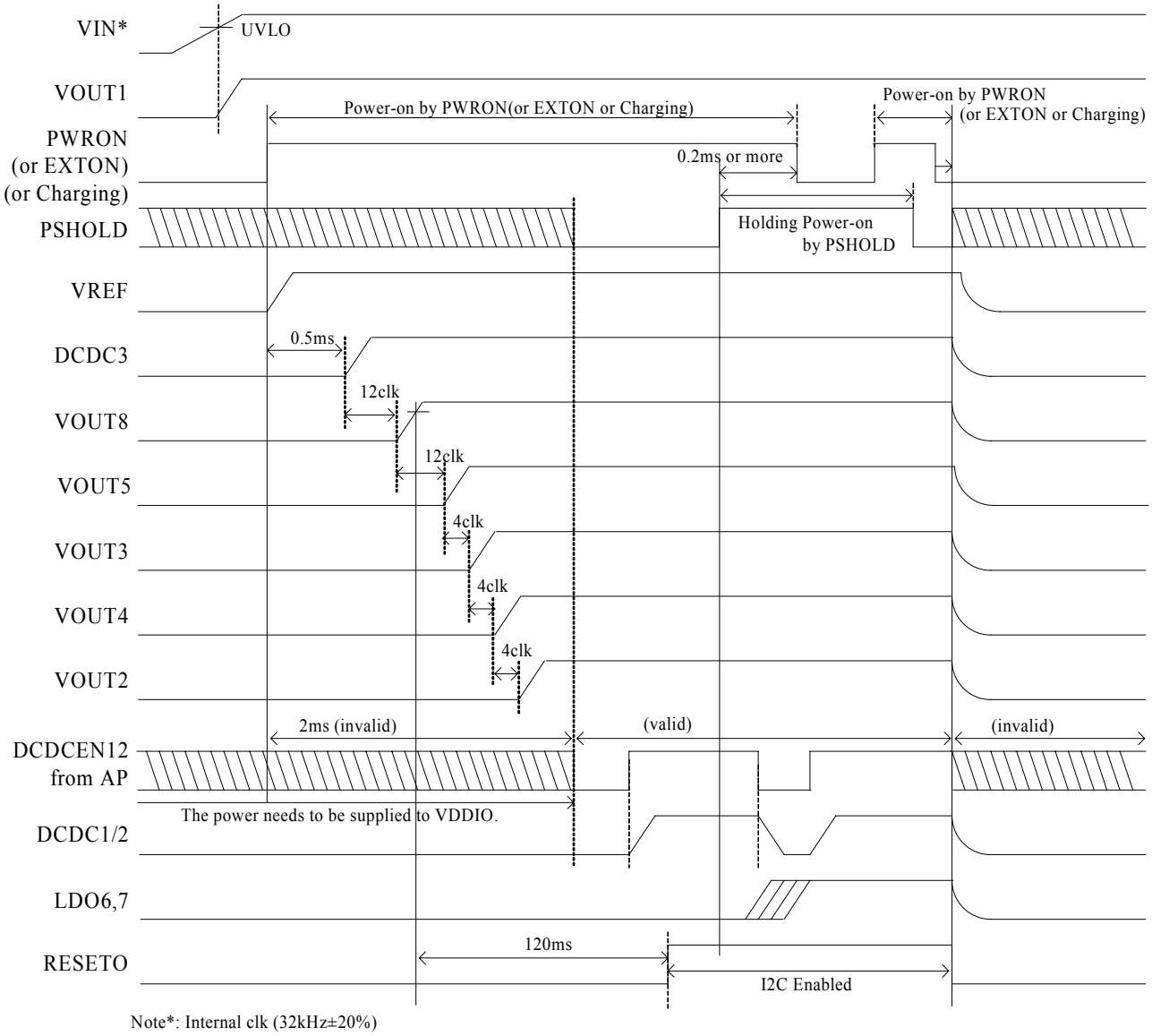
14. Appendix

◎External Components



◎Selectable by Trimming(Sequence1～4)

・Sequence1

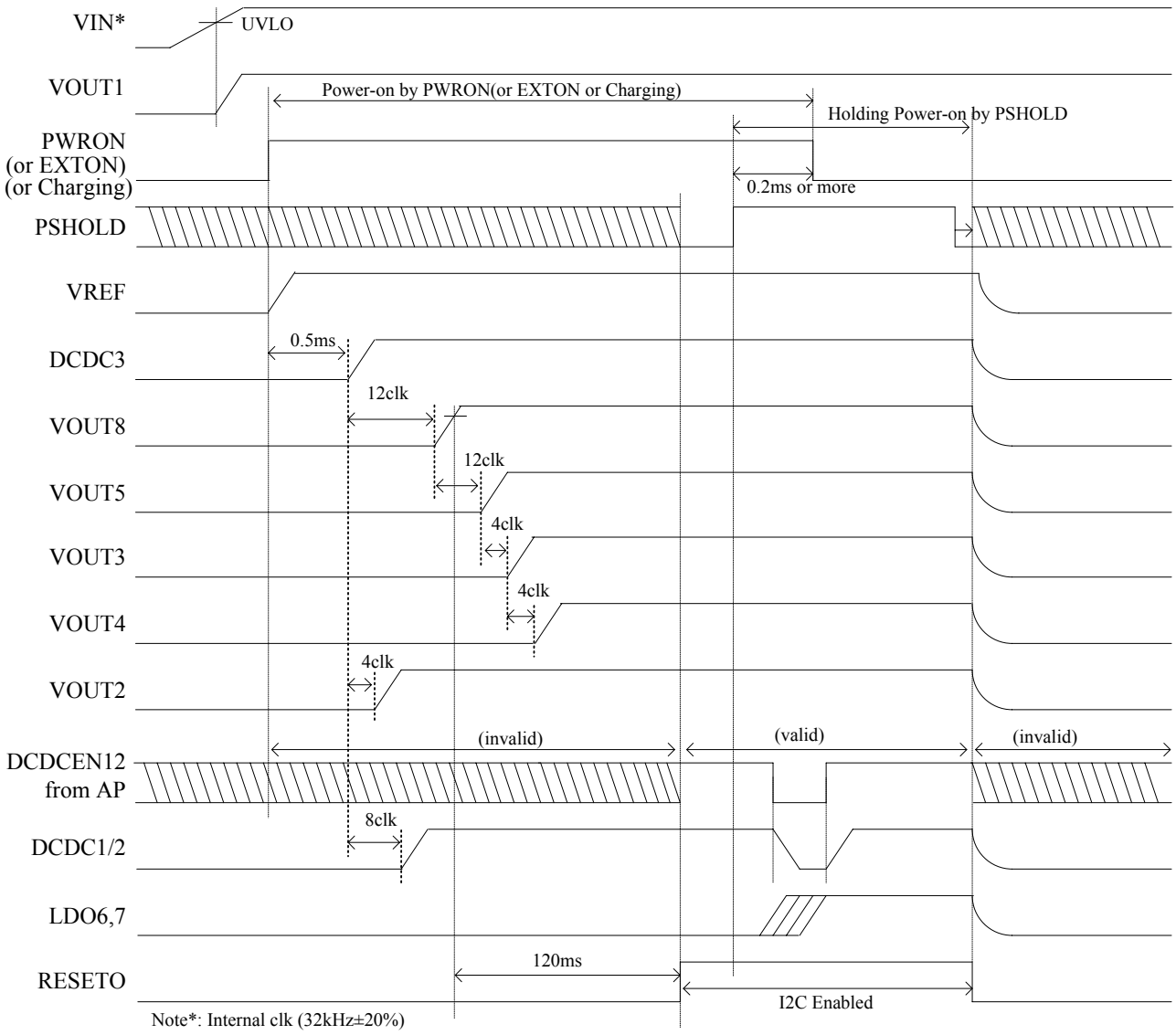


Note*: Internal clk (32kHz±20%)

Note*: The trimming setting of this sequence:

- DCDCEN12 pin is valid 2ms after the start of power-on. DCDCEN3 pin is invalid.
- LDO2 and VREF turn on following the power-on sequence.
- Default of LDOnON bit is “on”. (n=3, 4, 5)
- Power-on by Charging is valid.
  (Initial value of ILIM[3:0] bits is 720mA.)
  (Initial value of ICHGSET[3:0] bits is 500mA.)

・Sequence2



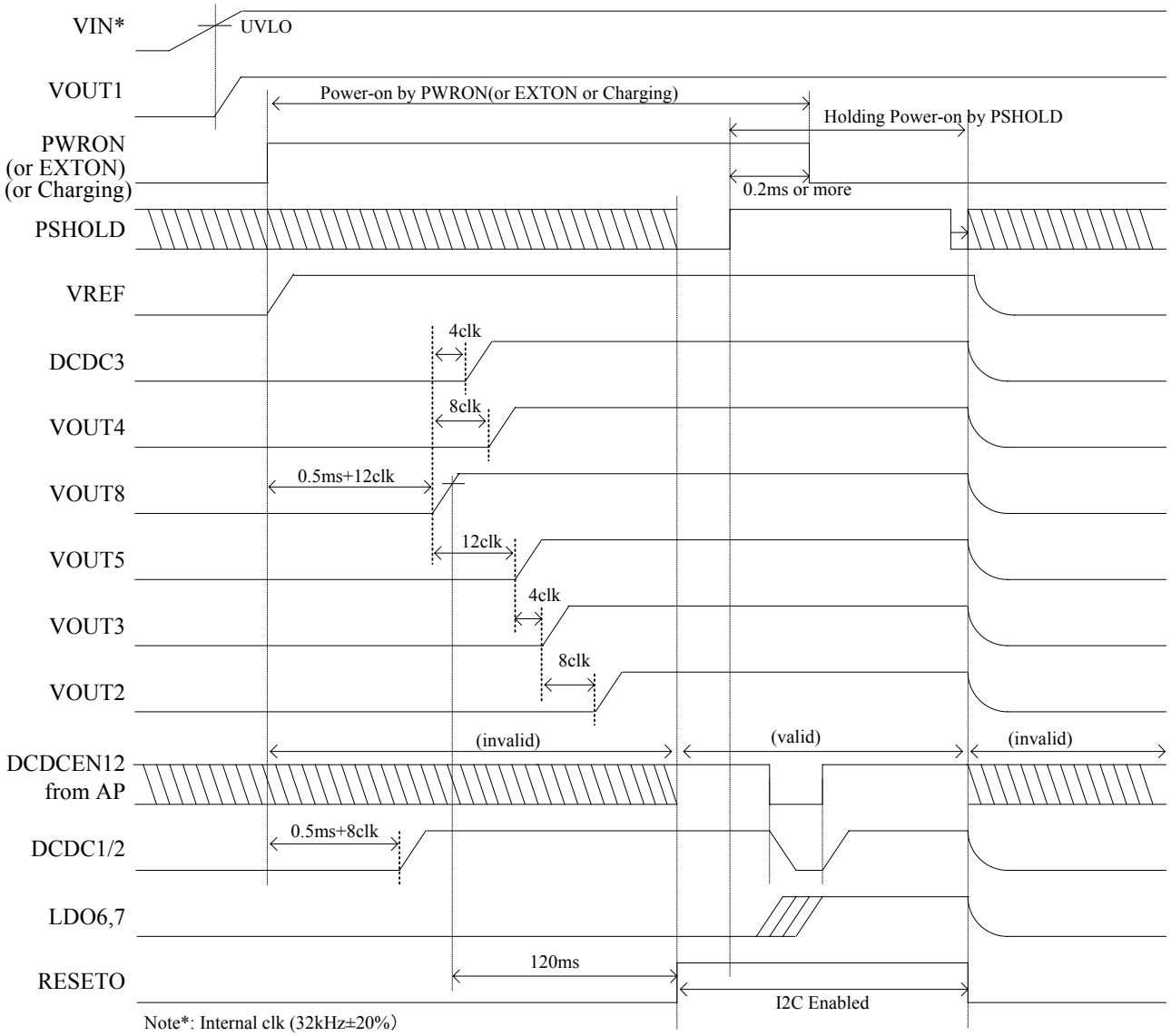
Note*: The trimming setting of this sequence:

- DCDCEN12 pin is valid after RESETO is released. DCDCEN3 pin is invalid.
- LDO2 and VREF turn on following the power-on sequence.
- Default of LDOnON bit is “on”. (n=3, 4, 5)
- Power-on by Charging is valid.

  (Initial value of ILIM[3:0] bits is 720mA.)

  (Initial value of ICHGSET[3:0] bits is 500mA.)

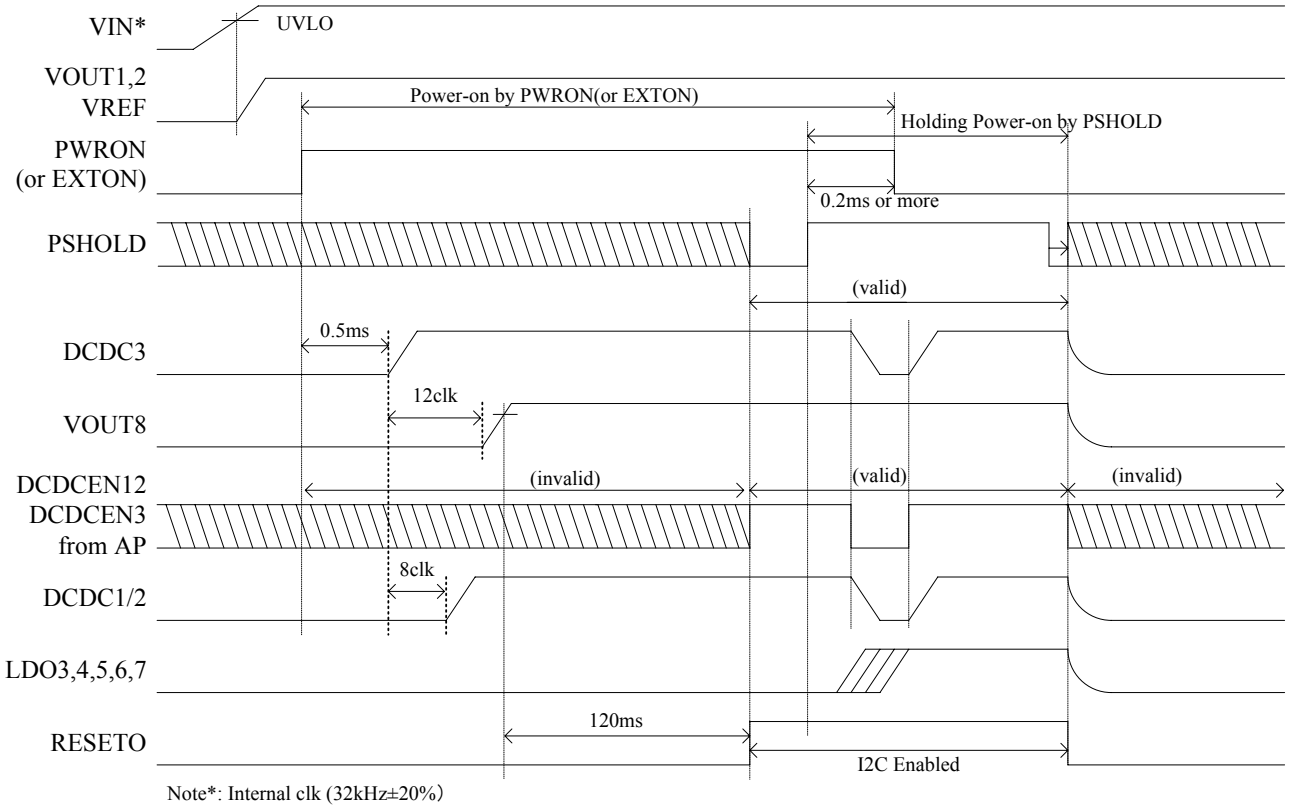
・Sequence3



Note*: The trimming setting of this sequence:

- DCDCEN12 pin is valid after RESETO is released. DCDCEN3 pin is invalid.
- LDO2 and VREF turn on following the power-on sequence.
- Default of LDOnON bit is “on”. (n=3, 4, 5)
- Power-on by Charging is valid.
  (Initial value of ILIM[3:0] bits is 1200mA.)
  (Initial value of ICHGSET[3:0] bits is 900mA.)

・Sequence4



Note*: The trimming setting of this sequence:

- DCDCEN12 pin and DCDCEN3 pin are valid after RESETO is released.
- LDO2 and VREF are always on.
- Default of LDOnON bit is “off”. (n=3, 4, 5)
- Power-on by Charging is invalid.

  (Initial value of ILIM[3:0] bits is 720mA.)

  (Initial value of ICHGSET[3:0] bits is 500mA.)