Power Management System Device

RN5T561-0000

Development Specifications

Rev. 1.3

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RICOH COMPANY, LTD.
Electronic Devices Company

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1. Outline

RN5T561 is the power management IC, which contains the power supply, the power supply control function and etc. in one-chip.

2. Feature

- Power Supply Function
  - ✓ Power supply control function

- One Step-down DC/DC converter
  - ✓ ON/OFF programmable through I2C
  - ✓ PWM control
  - ✓ DCDC output voltage settable by external resistor

- Four LDO Regulators
  - ✓ ON/OFF programmable through I2C (Except LDO2)
  - ✓ ECO-mode for LDO1, 2 and 3: Programmable through I2C
  - ✓ LDO1 output voltage: Selectable by trimming work

- I2C-Bus (Max 400kHz)
  - ✓ Slave address = 32h
  - ✓ LDO, DC/DC converter control

- UVLO
  - ✓ Monitoring VIN2 voltage

- Package
  - ✓ 16pin QFN package (Body size: 3 x 3 x 0.85mm, Pin pitch: 0.4mm)

- Process
  - ✓ CMOS process

3. Pin Configuration

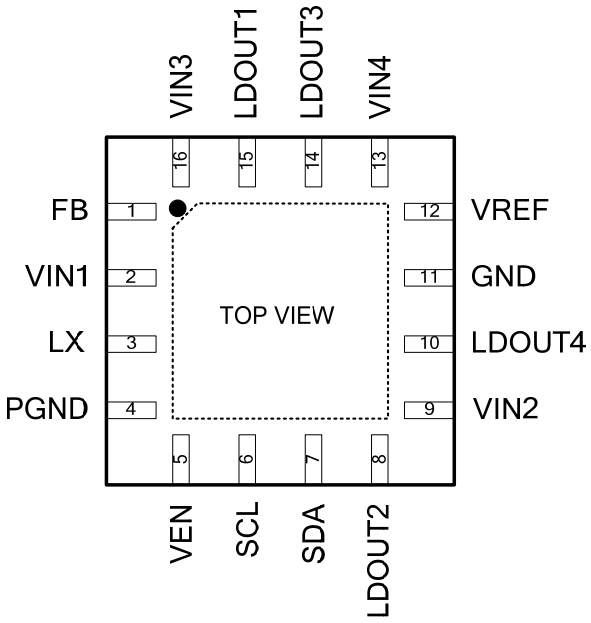

Fig 3-1 Pin Configuration

4. Block Diagram

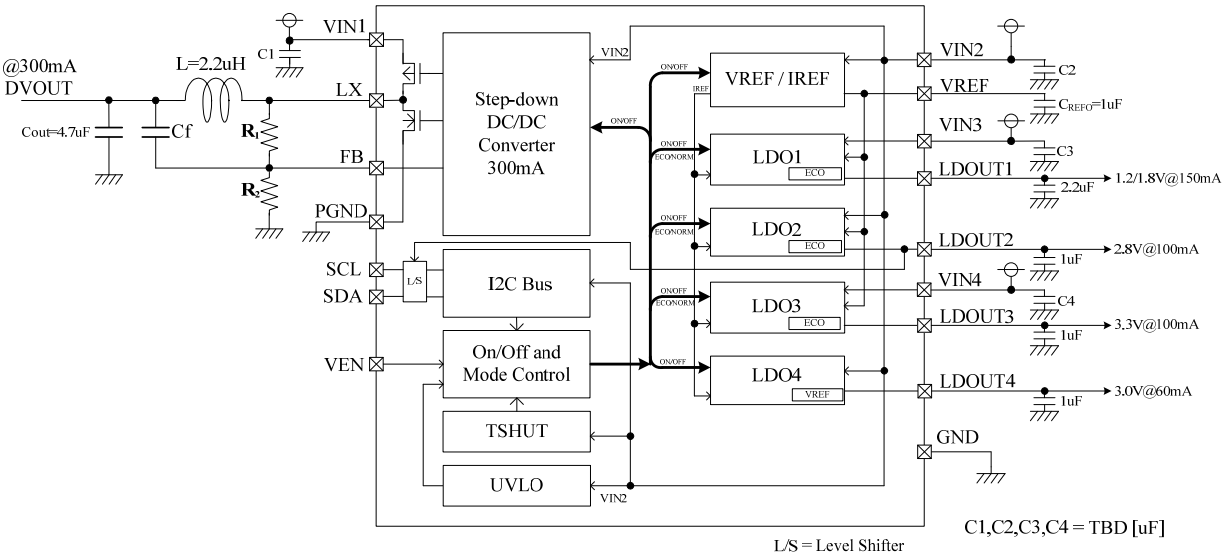

Fig 4-1 Block Diagram

5. Pin Description

NO	NAME	I/O	FUNCTION	NOTES
1	FB	I	Output voltage feedback of DC/DC converter	
2	VIN1	PWR	Power supply for DC/DC converter	
3	LX	O	Switch output of DC/DC converter circuit	
4	PGND	GND	Power GND for DC/DC converter	
5	VEN	I	Power-on signal	Schmitt /pull-down
6	SCL	I	Clock input for I2C-Bus	Schmitt
7	SDA	I/O	Data input/output for I2C-Bus	Schmitt /Nch Open-drain
8	LDOUT2	O	Output of LDO2	
9	VIN2	PWR	Power supply for VREF, LDO2 and 4	
10	LDOUT4	O	Output of LDO4	
11	GND	GND	GND	
12	VREF	O	Capacitor connection for reference	Do not load this pin.
13	VIN4	PWR	Power supply for LDO3	
14	LDOUT3	O	Output of LDO3	
15	LDOUT1	O	Output of LDO1	
16	VIN3	PWR	Power supply for LDO1	

Table 5-1 Pin Description

6. Power On/Off Control

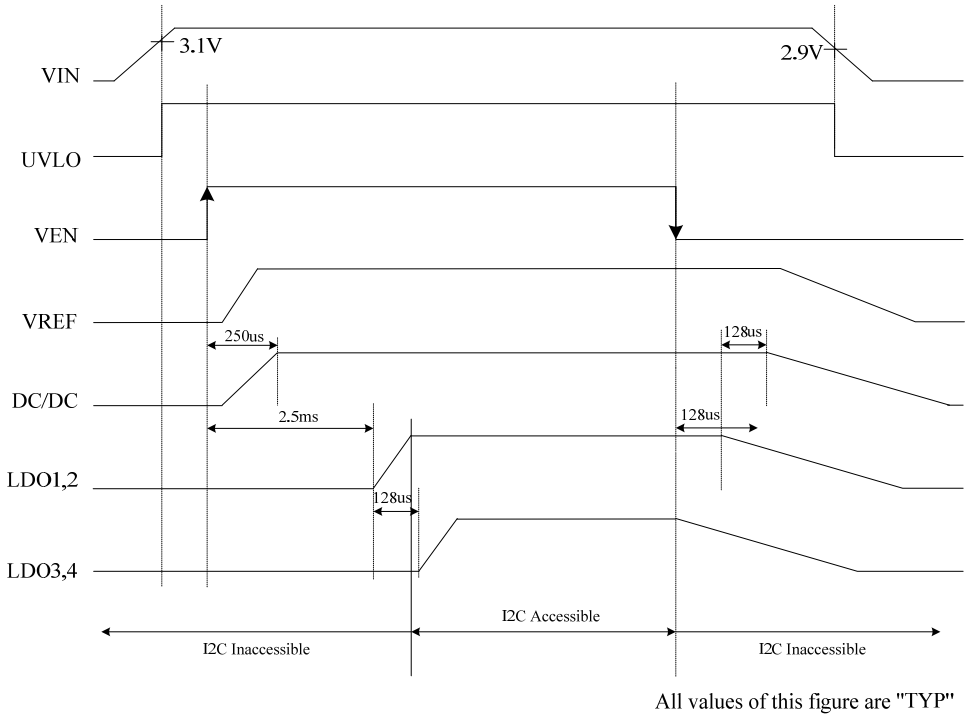

Fig 6-1 Power On/Off Timing

RN5T561 can be asserted power on by pushing VEN pin high but UVLO signal should be high by detecting the battery voltage over 3.1V. Step-down DC/DC converter turns on 250us after VEN pin goes high and then LDO1and 2 turn on. Then LDO3 and 4 are turned on with 120us of time interval.

When VEN goes low, all LDOs, DC/DC converter and logics are powered off and all register will be reset.

Note*: Wait more than 1ms to repower on by VEN= “H”.

6.1 UVLO (Under Voltage Lock Out)

Operating Conditions (unless otherwise specified) Ta = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{Release}$	Under voltage lock out threshold	VCCVIN rising		2.25		V
V_{Detect}	Under voltage lock out threshold	VCCVIN falling	2.05	2.20	2.35	V
V_{HYS}	UVLO Hysteresis	-		50		mV

Table 6-1 UVLO

7. Functional Blocks

7.1 Regulators

RN5T561 has 4 Low Drop Output regulators, LDO1 to LDO4. Power on/off of each regulator and ECO-mode of LDO1, 2 and 3 are programmable by setting data through I2C. LDO1 output voltage is settable by trimming work.

For the type of the bypass capacitor, it must be the ceramic type, not tantalum type, since the optimization design is based on the ceramic type for the phase compensation.

	LDO1	LDO2 (IO/LCD)	LDO3 (USB)	LDO4 (Audio/Analog)
Initial Value	1.2V/1.8V	2.8V	3.3V	3.0V
Programmable Output Voltage	1.2V/1.8V	Fix	Fix	Fix
Initial State *1	ON	ON	ON	ON
ECO-mode	Yes *2	Yes *2	Yes *2	No
On/Off Control	I2C-Bus	-	I2C-Bus	I2C-Bus
Auto-discharge	No	No	No	No

Note*1: Initial State is when VEN pin is high.

Note*2: LDO1, 2 and 3 have ECO-mode. But they can turn on at Normal-mode only not at ECO-mode.

Table 7-1 Regulator Table

7.1.1 Operation Mode Control

RN5T561 provides ECO-mode in LDO1, 2 and 3 for low power consumption. When peripheral Ics are in sleep state or low power consumption state, ECO-mode allows RN5T561 to operate at low power consumption. ECO-mode is programmable by register setting through I2C.

ECO-mode of LDO1, 2 and 3 are individually programmable by setting LDOiECO (I = 1,2,3) bit in MODECTL register. LDO1, 2 and 3 go into ECO-mode when LDOiECO="1" and Normal-mode when LDOiECO="0".

Transition delay time between ECO-mode and Normal-mode is 500us.

It is not recommendable to change LDO operation mode in 500us after transition. (If writing is performed in 500us after transition, noise may appear from the output.)

7.1.2 LDO1 Electrical Characteristics

(1) Normal Mode

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1.0 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT1	Output Voltage	1.6V≦VIN≦2.0V IOUT1=90mA	-3%	1.2	+3%	V
		3.3V≦VIN≦4.5V IOUT1=90mA		1.8		
IOUT1	Output Current	-		90	150	mA
ISHORT1	Short Current	VOUT1=0V		150		mA
VDRP1	Drop-out Voltage	IOUT1=90mA		200		mV
$\frac{\Delta VOUT1}{\Delta VIN}$	Line Regulation	1.6V≦VIN≦2.0V IOUT1=90mA		2.4		mV
		3.3V≦VIN≦4.5V IOUT1=90mA				
$\frac{\Delta VOUT1}{\Delta IOUT1}$	Load Regulation	50 μA＜IOUT1＜150mA		25		mV
$\frac{\Delta VOUT1}{\Delta T_a}$	Output Voltage Temperature Coefficient	-30℃≦T_a≦85℃		±100		ppm/℃
RR1	Ripple Rejection	f=1kHz, IOUT1=90mA		65		dB
EN1	Output Noise (RMS)	BW=100Hz-100kHz, IOUT1=90mA		110		μVrms
BC1	Bypass Capacitor	0 μA＜IOUT1＜150mA		2.2		μF
ISS1	Supply Current	No-load (Normal-mode)		85		μA
		OFF			1	

(2) ECO Mode

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1.0 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT1	Output Voltage	1.6V≦VIN≦2.0V IOUT1=5mA	-3%	1.2	+3%	V
		3.3V≦VIN≦4.5V IOUT1=5mA		1.8		
IOUT1	Output Current	-		5	10	mA
ISS1	Supply Current	ECO-mode		3		μA

Table 7-2 LDO1 Electrical Characteristics

Note*: Bypass capacitor: 2.2 μF in mounted state.

For optimized phase compensation, the bypass capacitor must be the ceramic type.

7.1.3 LDO2 Electrical Characteristics (IO/LCD)

(1) Normal Mode

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT2	Output Voltage	3.3V≦VIN≦4.5V IOUT2=60mA	-3%	2.8	+3%	V
IOUT2	Output Current	-		60	100	mA
ISHORT2	Short Current	VOUT2=0V		100		mA
VDRP2	Drop-out Voltage	IOUT2=60mA		150		mV
$\frac{\Delta VOUT2}{\Delta VIN}$	Line Regulation	3.3V≦VIN≦4.5V IOUT2=60mA		2.4		mV
$\frac{\Delta VOUT2}{\Delta IOUT2}$	Load Regulation	50 μA＜IOUT2＜100mA		25		mV
$\frac{\Delta VOUT2}{\Delta T_a}$	Output Voltage Temperature Coefficient	-30℃≦T_a≦85℃		±100		ppm/℃
RR2	Ripple Rejection	f=1kHz, IOUT2=60mA		60		dB
EN2	Output Noise (RMS)	BW=100Hz-100kHz, IOUT2=60mA		120		μVrms
BC2	Bypass Capacitor	0 μA＜IOUT2＜100mA		1.0		μF
ISS2	Supply Current	No-load		85		μA
		OFF			1	

(2) ECO Mode

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT2	Output Voltage	3.3V≦VIN≦4.5V IOUT2=5mA	-3%	2.8	+3%	V
IOUT2	Output Current	-		5	10	mA
ISS2	Supply Current	ECO-mode		3		μA

Table 7-3 LDO2 Electrical Characteristics

Note*: Bypass capacitor: 1.0 μF in mounted state.

For optimized phase compensation, the bypass capacitor must be the ceramic type.

7.1.4 LDO3 Electrical Characteristics (USB)

(1) Normal Mode

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT3	Output Voltage	3.6V≦VIN≦5.5V IOUT3=60mA	-3%	3.3	+3%	V
IOUT3	Output Current	-		60	100	mA
ISHORT3	Short Current	VOUT3=0V		100		mA
VDRP3	Drop-out Voltage	IOUT3=60mA		100		mV
$\frac{\Delta VOUT3}{\Delta VIN}$	Line Regulation	3.6V≦VIN≦5.5V IOUT3=60mA		2.4		mV
$\frac{\Delta VOUT3}{\Delta IOUT3}$	Load Regulation	50 μA＜IOUT3＜100mA		25		mV
$\frac{\Delta VOUT3}{\Delta T_a}$	Output Voltage Temperature Coefficient	-30℃≦T_a≦85℃		±100		ppm/℃
RR3	Ripple Rejection	f=1kHz, IOUT3=60mA		60		dB
EN3	Output Noise (RMS)	BW=100Hz-100kHz, IOUT3=60mA		140		μVrms
BC3	Bypass Capacitor	0 μA＜IOUT3＜100mA		1.0		μF
ISS3	Supply Current	No-load		85		μA
		OFF			1	

Table 7-4 LDO3 Electrical Characteristics

(2) ECO Mode

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT3	Output Voltage	3.6V≦VIN≦5.5V IOUT3=5mA	-3%	3.3	+3%	V
IOUT3	Output Current	-		5	10	mA
ISS3	Supply Current	ECO-mode		3		μA

Table 7-5 LDO3 Electrical Characteristics

Note*: Bypass capacitor: 1.0 μF in mounted state.

For optimized phase compensation, the bypass capacitor must be the ceramic type.

7.1.5 LDO4 Electrical Characteristics (Analog/Audio)

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUT4	Output Voltage	3.3V≦VIN≦4.5V IOUT4=40mA	-3%	3.0	+3%	V
IOUT4	Output Current	-		40	60	mA
ISHORT4	Short Current	VOUT4=0V		100		mA
VDRP4	Drop-out Voltage	IOUT4=40mA		100		mV
$\frac{\Delta VOUT4}{\Delta VIN}$	Line Regulation	3.3V≦VIN≦4.5V IOUT4=40mA		2.4		mV
$\frac{\Delta VOUT4}{\Delta IOUT4}$	Load Regulation	50μA＜IOUT4＜60mA		25		mV
$\frac{\Delta VOUT4}{\Delta T_a}$	Output Voltage Temperature Coefficient	-30℃≦T_a≦85℃		±100		ppm/℃
RR4	Ripple Rejection	f=1kHz, IOUT4=40mA		70		dB
EN4	Output Noise (RMS)	BW=100Hz-100kHz IOUT4=40mA		130		μVrms
BC4	Bypass Capacitor	0μA＜IOUT4＜60mA		1.0		μF
ISS4	Supply Current	No-load		100		μA
		OFF			1	

Table 7-6 LDO4 Electrical Characteristics

Note*: Bypass capacitor: 1.0 μF in mounted state.

For optimized phase compensation, the bypass capacitor must be the ceramic type.

7.1.6 VREF and IREF Electrical Characteristics

Operating Conditions (unless otherwise specified) VIN= 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{REFO}	Bypass Capacitor	-		1.0		μF
VOUT	Output Voltage	3.3V≦VIN≦4.5V		2.0		V
ISS	Supply Current	No-load		20		μA
		OFF		1		

Table 7-7 VREF and IREF Electrical Characteristics

7.2 Step-down DC/DC Converter

DCDC converter turns on by VEN="H" (DC/DC enable signal). During standby mode, LX pin is high impedance. When DCDC becomes active, the internal Soft-start circuit is enabled and output voltage starts boosting. RN5T561 compares internal reference voltage (typ.0.6V) and FB voltage. If FB voltage is below the reference voltage, it turns on high-side switch by enabling one-shot circuit.

The high-side switch remains on for minimum on time and until FB voltage rises over the reference voltage or inductor current exceeds limit current. Once the high-side switch is disabled, it remains off until FB voltage falls below the reference voltage or inductor current falls below the limit current. During high-side switch is off, low-side switch remains on until inductor current approaches 0. DCDC converter regulates the output voltage by repeating the above operation.

Therefore, oscillator frequency varies by input voltage, output voltage, output current and external circuit (R1, L, Cf).

In addition, the feedback loop from LX pin through R1 and from DVOUT through Cf eliminate phase lag by output capacitor providing the stable loop and fast transient response.

However, the equivalent series resistance causes output voltage to shift by output current. (Theoretically, output voltage falls [IOUT(A)xDCR(Ω)])

7.2.1 Step-down DC/DC Converter Block Diagram

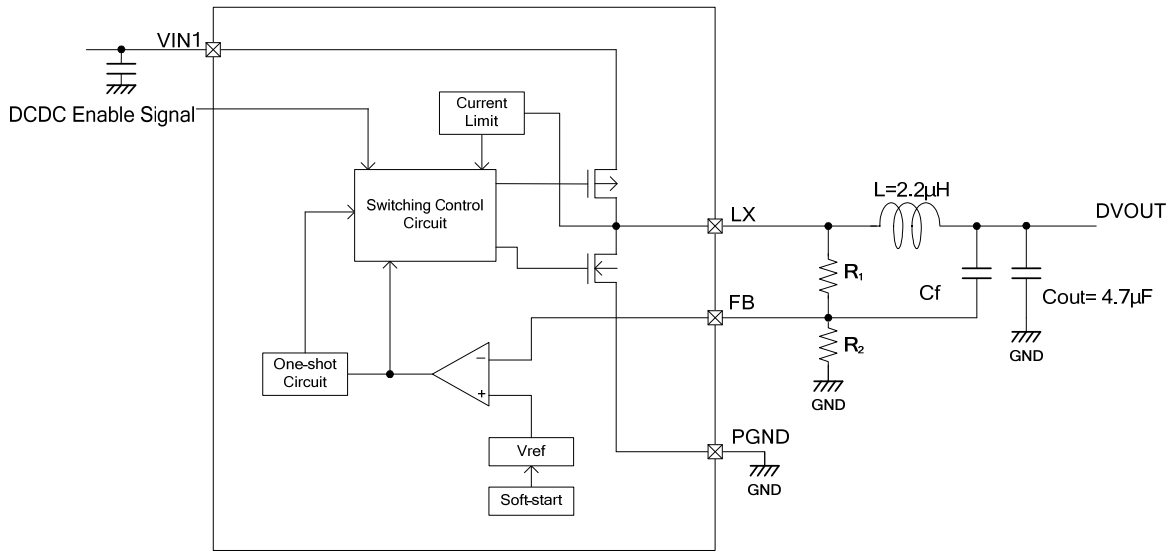

Fig 7-1 Step-down DC/DC Converter Block Diagram

R1=R2*(DVOUT/V_{FB}-1)

DVOUT=Set output voltage

V_{FB} = 0.6V (Internal reference voltage)

$$Cf = \frac{L}{R1} \times 10$$

External components example

- DVOUT=1.2V.
  R_1=220kΩ, R_2=220kΩ, Cf=100pF
- DVOUT=1.8V.
  R_1=220kΩ, R_2=110kΩ, Cf=100pF

7.2.2 Target Electrical Characteristics

Operating Conditions (unless otherwise specified) VIN = 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIN	Input Voltage	-	3.3		4.5	V
DVOUT	Output Voltage Range	DIOUT=200mA	1.0		2.0	V
DIOUT	Maximum continuation output current	VIN=3.3~4.5V			300	mA
DISS	Consumption Current	VIN=3.6V DIOUT=0mA, DVOUT=1.2V		45		μA
DI_{sd}	Standby Current	VIN=4.5V OFF state		0.01		μA
DILx	DC/DC Limit Current	-	600	900	1500	mA
t_{prot}	Protection Delay Time	-		1.6 *1		ms
$\frac{\Delta VFB}{\Delta VIN}$	FB Line Regulation (DC/DC)	VIN=3.3~4.5V DIOUT=200mA		10		mV
t_r	Soft Start Time	-		120		μs
V_{FB}	V_{FB} Voltage	-	-1.5%	0.6	+1.5%	V
$\frac{\Delta V_{FB}}{\Delta T}$	Output Voltage Temperature Coefficient	-30℃≦Ta≦+85℃		±100	±300	ppm/℃
TONmin	Minimum On Time	-		100		ns

Table 7-8 Step-down DCDC Converter Electrical Characteristics

Note*1: If the over-current condition keeps on 1.6ms, a protection circuit starts and RN5T561 clears DCON bit in DCCTL register to “0”. To release DCDC converter block from protection mode, enable DCDC converter by setting DCON bit to “1” through I2C.

7.2.3 Recommended External Component

Vendor	Part number	Inductance [uH]	DCR [Ω]
FDK	MIPW3226D2R2M	2.2	0.1

Table 7-9 Recommended External Component

7.3 Thermal Shutdown Circuit

Overheat state can be detected by comparing the output voltages from two temperature detection circuits, which have different temperature characteristics. If the overheat state is detected, RN5T561 will turn off to protect itself from overheating. When VEN signal is "H" (Enable), the thermal shutdown function is valid.

7.3.1 Thermal Shutdown Electrical Characteristics

Operating Conditions (unless otherwise specified) VIN= 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DET}	Detected Temperature	-		140		℃
T_{RET}	Return Temperature	-		110		℃
I_{SS}	Supply Current	-		5		μA

Table 7-10 Thermal Shutdown Electrical Characteristics

7.4 CPU Interface

RN5T561 uses I2C-Bus system for CPU connection via 2-wires. Connection and transfer system of I2C-Bus are described in the following sections.

Note*: All register of RN5T561 is writing only and it is accessible via I2C-Bus only when LDO2 turns on.

7.4.1 Start and Stop Condition

Within the procedure of I2C-Bus, unique situations arise which are defined as Start and Stop conditions.

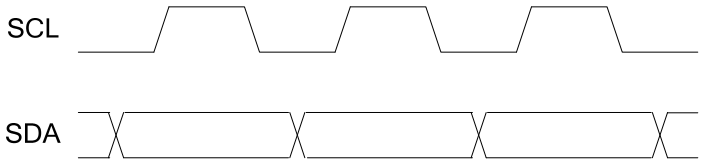

Fig 7-2 I2C-Bus Data Transmission

An “H” to “L” transition on SDA line while SCL is “H” indicates a Start condition. An “L” to “H” transition on SDA line while SCL is “H” defines a Stop condition. Start and Stop conditions are always generated by master (Refer to the figure below). The bus is considered to be busy after the start condition. The bus is considered to be free again a certain time after the stop condition.

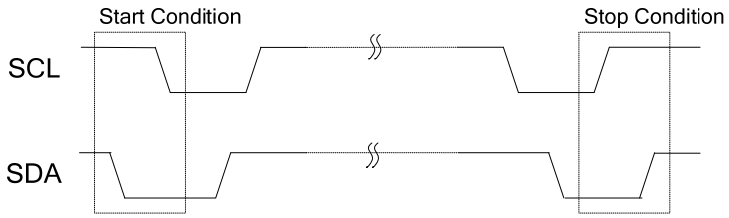

Fig 7-3 I2C-Bus Start and Stop Condition

7.4.2 Data Transmission and its Acknowledge

After start condition, data is transmitted by 1byte (8bits). The number of bytes that can be transmitted per transmission is not limited. Receiver must send an acknowledge signal to the transmitter every time 8bit data is transmitted.

Data transmission must be accompanied by acknowledge signal. The master generates the clock pulse for acknowledge bit. The transmitter releases SDA line during the acknowledge clock pulse.

The receiver must pull down SDA line during the acknowledge clock pulse so that it remains stable "L" during "H" period of this clock pulse.

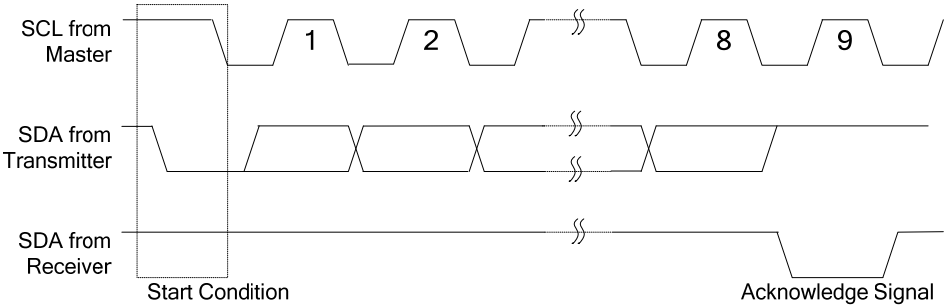

Fig 7-4 I2C-Bus Data Transmission and Acknowledge

7.4.3 I2C-Bus Slave Address

After the start condition, a slave address is sent. This address is 7 bits long followed by. The slave address of RN5T561 is specified at 32h.

	A7	A6	A5	A4	A3	A2	A1
Setting value	0	1	1	0	0	1	0

A7～A1: Slave Address

Table 7-11 Slave Address of RN5T561

7.4.4 Data Transmission Write Format

The transmission format for the slave address allocated to each IC is defined by I2C-Bus standard. However transmission method of address information of each IC is not defined. RN5T561 transmits data to the internal address pointer at 1byte continue to the slave address and write command. For the data transmission, please transmit MSB first from Master and following data in sequence.

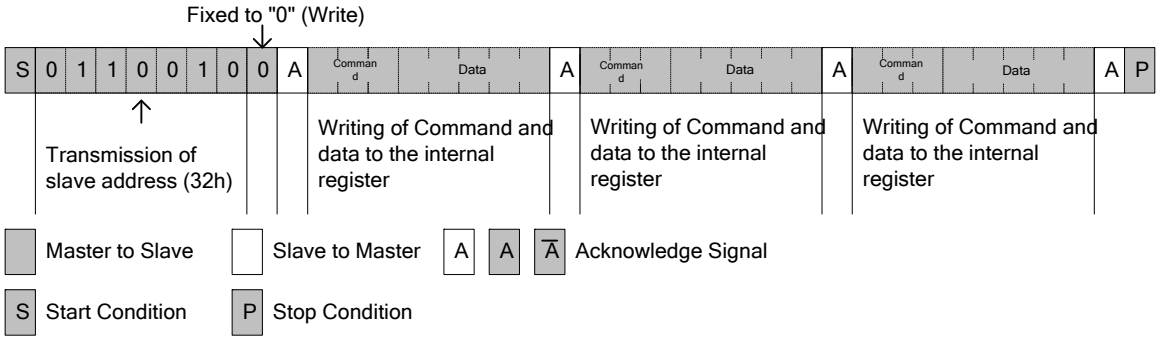

Fig 7-5 Data Transmission Write Format

7.4.5 Internal Register Write-in Timing

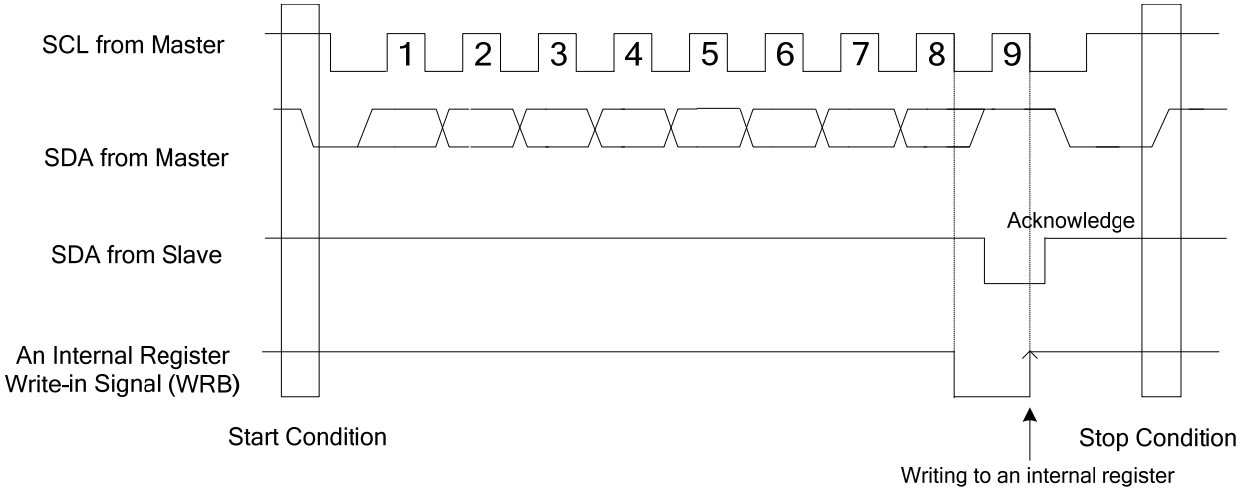

Fig 7-6 Internal Register Write-in Timing

7.4.6 AC Characteristics of I2C-Bus

Operating Conditions (unless otherwise specified) VIN= 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SCL}	SCL Clock Frequency	-			400	kHz
t_{BUF}	Bus Free Time between a STOP and START condition	-	1.3			μs
t_{LOW}	LOW period of SCL clock	-	1.3			μs
t_{HIGH}	HIGH period of SCL clock	-	0.6			μs
$t_{SU;STA}$	Set-up time for a repeated START condition	-	0.6			μs
$t_{HD;STA}$	Hold time (repeated) START condition	-	0.6			μs
$t_{SU;STO}$	Set-up time for STOP Condition	-	0.6			μs
$t_{HD;DAT}$	Data hold time	-	0			μs
$t_{SU;DAT}$	Data Set-up Time	-	100 *2			ns
t_R	Rise Time of both SCL and SDA signals	-			300	ns
t_F	Fall Time of both SCL and SDA signals	-			300	ns
t_{SP}	Spike Width that can be Removed with Input Filter	-			50 *1	ns

Table 7-12 I2C-Bus Electrical Characteristics

Note*: All the above-mentioned values are corresponding to V_{IH} min and V_{IL} max level.

Note*1: Guaranteed by design not production tested.

Note*2: Standard mode is allowed in I^2C-Bus standard. For Standard mode, it needs to satisfy the condition; tSU;DAT>=250ns

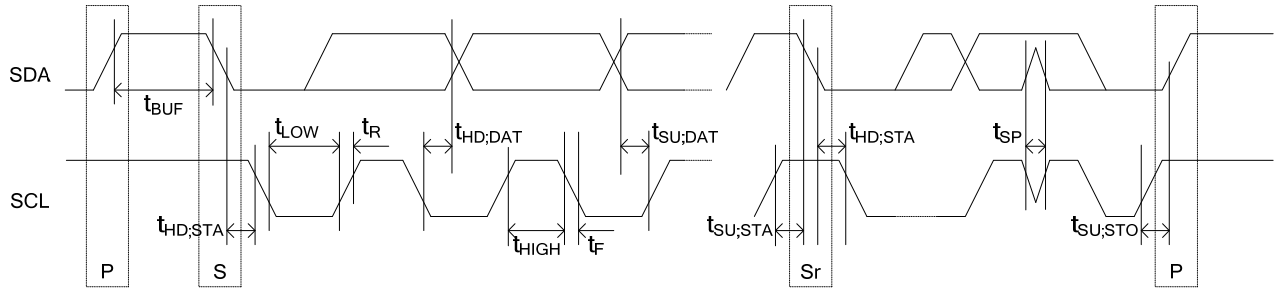

Fig 7-7 AC Characteristics of I2C-Bus

8. Register

8.1 Register Map

Name	Function							
	Command			Data				
	C2	C1	C0	D4	D3	D2	D1	D0
DCCTL	0	0	0	-	-	-	-	DCON
LDOCTL	0	0	1	-	LDO4ON	LDO3ON	-	LDO1ON
MODECTL	0	1	0	-	-	LDO3ECO	LDO2ECO	LDO1ECO
TEST	All other registers except above. *1			Don't touch.				

Note*1: The registers except above top 3 are Test registers. Don't touch Test registers.

Table 8-1 Register Map

8.2 DC/DC Converter Control Register: DCCTL (Command 000b)

bit	Name	R/W	Function	1	0	Initial value
4-1	-	-	Reserved	-	-	-
0	DCON	W	DC/DC converter ON/OFF control bit	ON	OFF	1

8.3 LDO Control Register: LDOCTL (Command 001b)

bit	Name	R/W	Function	1	0	Initial value
4	-	-	Reserved	-	-	-
3	LDO4ON	W	LDO4 ON/OFF control bit	ON	OFF	1
2	LDO3ON	W	LDO3 ON/OFF control bit	ON	OFF	1
1	-	-	Reserved	-	-	-
0	LDO1ON	W	LDO1 ON/OFF control bit	ON	OFF	1

8.4 Mode Control Register: MODECTL (Command 010b)

bit	Name	R/W	Function	1	0	Initial value
4-3	-	-	Reserved	-	-	-
2	LDO3ECO	W	LDO3 ECO-mode control bit	ECO	Normal	0
1	LDO2ECO	W	LDO2 ECO-mode control bit	ECO	Normal	0
0	LDO1ECO	W	LDO1 ECO-mode control bit	ECO	Normal	0

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

The operation exceeding "Absolute Maximum Ratings" below may cause permanent damage to the device. The operation of the device within the stated ratings below is not guaranteed.

Symbol	Parameter	Condition	Rated value	Units
VIN1 VIN2 VIN3 VIN4	Power Supply Voltage	Voltage Input Pins	-0.3～6.0	V
IN1	Input Voltage Range	SCL, SDA	-0.3～VOUT2 +0.3	V
IN2	Input Voltage Range	VEN	-0.3～VIN2 +0.3	V
PD	Package Allowable Dissipation	Mounted on Board, T_a = 70℃	950*	mW
T_{stg}	Storage Temperature	-	-55～+125	℃

Note*: Derate 17.2[mW/℃] above +70℃.

Table 9-1 Absolute Maximum Ratings

9.2 Recommended Operation Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIN1	Power Supply Voltage1	Battery Voltage Input Pin	3.3		4.5	V
VIN2	Power Supply Voltage2	Battery Voltage Input Pin	3.3		4.5	V
VIN3	Power Supply Voltage3	Regulator Voltage Input Pin	1.6		2.0	V
		Battery Voltage Input Pin	3.3		4.5	V
VIN4	Power Supply Voltage4	Battery or USB Voltage Input Pin	3.6		5.5	V
T_a	Temperature of Operation	-	-30		+85	℃

Table 9-2 Recommendation of Operation Conditions

9.3 DC Characteristics

Operating Conditions (unless otherwise specified) VIN= 3.6V, C_{REFO} = 1 μF, T_a = 25℃

Symbol	Parameter	Condition	Min	Typ	Max	Units
VT1+	"H" input rising threshold voltage 1 (Schmitt)	VEN	0.6		1.6	V
VT1-	"L" input falling threshold voltage 1 (Schmitt)	VEN	0.4		1.0	V
V_{HIS1}	Schmitt hysteresis voltage 1	VEN	0.1			V
I_{IL1}	Input Leakage Current 1	VEN, V=0	-3		3	μA
R_{PD}	Pull-down resistance	VEN		3		MΩ
VT2+	"H" input rising threshold voltage 2 (Schmitt)	SCL, SDA	VOUT2 ×0.5		VOUT2 ×0.8	V
VT2-	"L" input falling threshold voltage 2 (Schmitt)	SCL, SDA	VOUT2 ×0.2		VOUT2 ×0.5	V
V_{HIS2}	Schmitt hysteresis voltage 2	SCL, SDA	VOUT2 ×0.10			V
V_{OL}	"L" Output Voltage	SDA, I_{sink}= 3mA			0.4	V
I_{IL2}	Input Leakage Current 1	SCL, SDA V=0～VOUT2	-3		3	μA
I_{OZ}	Off Leakage Current	SDA V=0～VOUT2	-3		3	μA
I_{SHUT}	Shut Down Supply Current (All output off)	VEN=0V VIN1~3=3.6V VIN4=5.0V		1		μA

Table 9-3 DC Characteristics

Terminal equivalent circuit

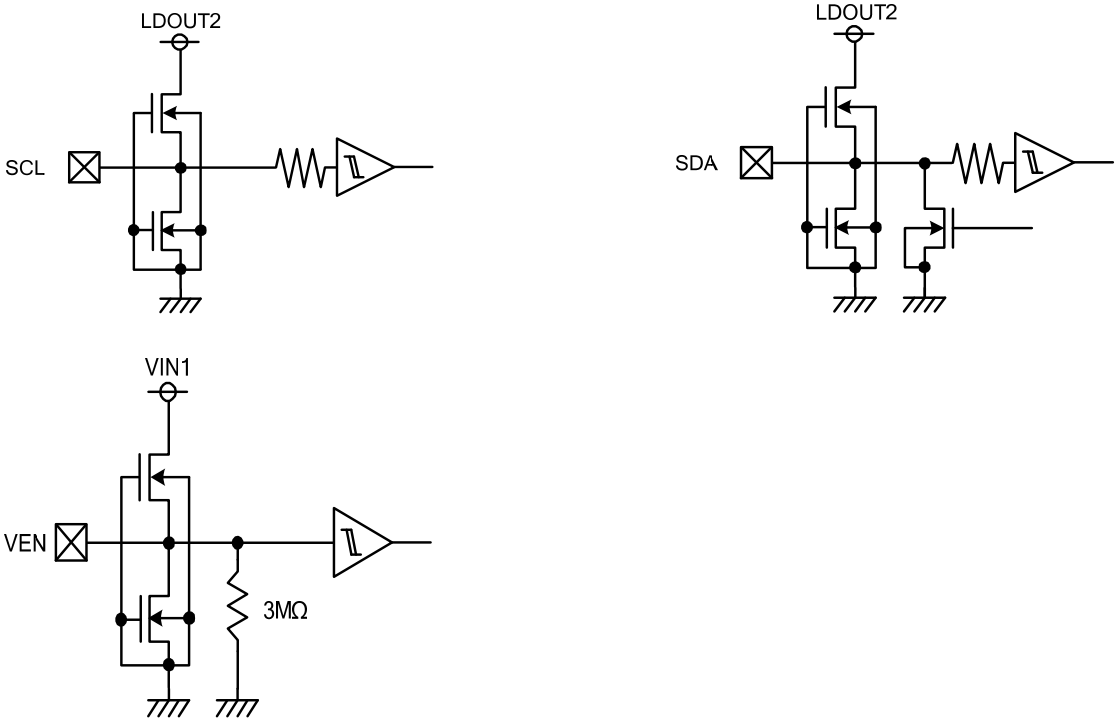

Fig 9-1 Terminal Equivalent Circuit

10. Package Information