
PCMCIA Power Controller

NO.EA-176-100709

OUTLINE

The R5533V Series switch the V_{CC} voltage among 0V, 3.3V or 5.0V. And the V_{PP} voltage is outputted in between either OFF, 0V, 3.3V or 5.0V conditions.

When the V_{CC} or V_{PP} pin are short-circuited to the GND, the minimum current limit protection values are V_{CC} pin=1A and V_{PP} pin=0.2A. R5533V is suitable for standard type of PCMCIA power controllers.

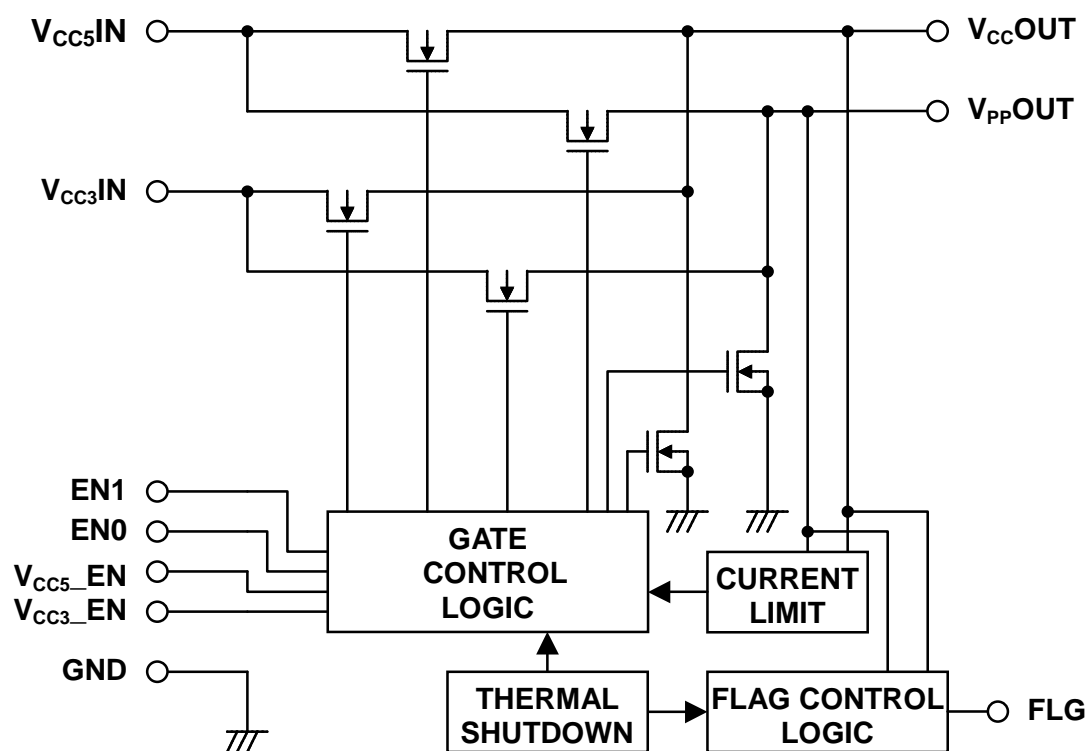
FEATURES

- Low ON resistance Nch MOSFET switch
- Built-in Over Current Limit Protection Function
- Built-in Thermal Shutdown Protection
- Open Drain Flag Pin
- Break-Before-Make Switching
- Package: SSOP-16 pin

APPLICATIONS

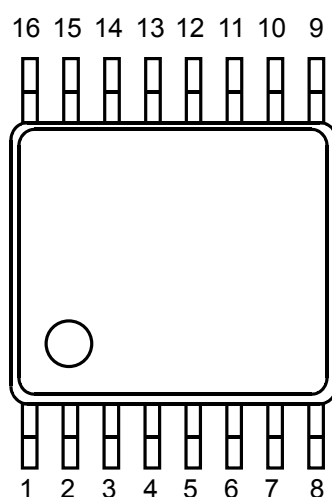
- Power Supply Switch for PC Card
- Power Supply Control for a card-bus slot
- PC Card Reader / Writer

BLOCK DIAGRAMS



PIN CONFIGURATIONS

• SSOP-16



PIN DESCRIPTIONS

| Pin No. | Symbol | Description |
|---------|---------------|---------------------|
| 1 | V_{CC5_EN} | Logic Input Pin |
| 2 | V_{CC3_EN} | Logic Input Pin |
| 3 | EN0 | Logic Input Pin |
| 4 | EN1 | Logic Input Pin |
| 5 | FLG | Flag Output Pin |
| 6 | TST | Test Pin |
| 7 | NC | No Connection |
| 8 | V_{PPOUT} | V_{PP} Output Pin |
| 9 | V_{CCOUT} | V_{CC} Output Pin |
| 10 | NC | No Connection |
| 11 | V_{CC3IN} | 3V Input Pin |
| 12 | V_{CCOUT} | V_{CC} Output Pin |
| 13 | V_{CC5IN} | 5V Input Pin |
| 14 | V_{CCOUT} | V_{CC} Output Pin |
| 15 | V_{CC5IN} | 5V Input Pin |
| 16 | GND | Ground Pin |

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

| Symbol | Item | Rating | Unit |
|-------------|---------------------------|--------------|------|
| V_{CC5IN} | Input Voltage (5V) | - 0.3 to 6.0 | V |
| V_{CC3IN} | Input Voltage (3V) | - 0.3 to 6.0 | V |
| V_{FLG} | Flag Voltage | - 0.3 to 6.0 | V |
| V_{IN} | Logic Input Voltage | - 0.3 to 6.0 | V |
| V_{TST} | Test Pin Voltage | - 0.3 to 6.0 | V |
| P_D | Power Dissipation * | TBD | mW |
| T_a | Ambient Temperature Range | - 40 to 85 | °C |
| T_{stg} | Storage Temperature Range | - 55 to 125 | °C |

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

RECOMMENDATION OF OPERATING CONDITION

(Ta=25°C)

| Item | Symbol | Rating |
|--------------------|---------------|-----------------------|
| Input Voltage (5V) | V_{CC5IN} | 4.5V to 5.5V |
| Input Voltage (3V) | V_{CC3IN} | 3.0V to 3.6V |
| Output Current | $I_O(V_{CC})$ | $I_O(V_{CC}) < 1A$ |
| | $I_O(V_{PP})$ | $I_O(V_{PP}) < 100mA$ |

ELECTRICAL CHARACTERISTICS

$V_{CC5IN} = 5V$, $V_{CC3IN} = 3.3V$, unless otherwise noted.

The specification is guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 85^{\circ}C$. The typical value is at $T_a = 25^{\circ}C$.

$T_a = 25^{\circ}C$

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------------------|---------------------|--|-------|--------------------------|---------|-------------|
| Supply Current | I_{CC5} | $V_{CCOUT} = 5V$ or $3.3V$ | | 180 | 340 | μA |
| Supply Current | I_{SLP5} | $V_{CCOUT} = 0V$ (Sleep Mode) | | 0.2 | 10 | μA |
| Supply Current | I_{CC3} | $V_{CCOUT} = 5V$ or $3.3V$ | | 7 | 20 | μA |
| Supply Current | I_{SLP3} | $V_{CCOUT} = 0V$ (Sleep Mode) | | 0.2 | 10 | μA |
| V_{CCOUT} Switch Resistance | R_{OVCC} | Select $V_{CCOUT} = 5V$ | | 90 | 140 | $m\Omega$ |
| | | Select $V_{CCOUT} = 3.3V$ | | 85 | 140 | $m\Omega$ |
| | | Select $V_{CCOUT} = 0V$ | 300 | 500 | 1100 | Ω |
| V_{PPOUT} Switch Resistance | R_{OVPP} | Select $V_{PPOUT} = 5V$ | | 1 | 1.5 | Ω |
| | | Select $V_{PPOUT} = 3.3V$ | | 1 | 1.5 | Ω |
| | | Select $V_{PPOUT} = 0V$ | 1500 | 2500 | 3900 | Ω |
| V_{PPOUT} Leakage Current | I_{PPL} | Select $V_{PPOUT} = Hi-Z$ | | 1 | 10 | μA |
| Reverse Leakage Current | I_{CC} | $V_{CC5IN} = V_{CC3IN} = 0V$ | | 3 | 50 | μA |
| | I_{PP} | $V_{CC5IN} = V_{CC3IN} = 0V$ | | 3 | 50 | μA |
| Short Current Limit | I_{CCSC} | $V_{CCOUT} = 0V$ | 1 | 1.7 | 2.5 | A |
| | I_{PPSC} | $V_{PPOUT} = 0V$ | 0.2 | 0.4 | 0.7 | A |
| Short Current Limit Response Time *1 | $t_{RES}(I_{CCSC})$ | $V_{CCOUT} = 0V$ | | 50 | | μs |
| | $t_{RES}(I_{PPSC})$ | $V_{PPOUT} = 0V$ | | 20 | | μs |
| Logic Input "H" Voltage | V_{IH} | | 2.0 | | 6.0 | V |
| Logic Input "L" Voltage | V_{IL} | | - 0.3 | | 0.8 | V |
| Logic Input Current | I_{IN} | | | | ± 1 | μA |
| Thermal Shutdown Temperature | T_{SD} | | | 140 | | $^{\circ}C$ |
| Hysteresis *2 | | | | 10 | | $^{\circ}C$ |
| Flag Threshold Voltage | V_{OOK} | FLG is pulled up to V_{CC3IN} with $10k\Omega$ | | V_{CC-1} V_{PP-1} | | V |
| Flag Voltage "L" | V_{FLG} | $I_{OL} = 2mA$ | | 0.3 | | V |
| Flag OFF Leakage Current | I_{FLGOFF} | $V_{IN} = V_{FLG} = 5.5V$ | | | 1 | μA |

*1 The specification is checked and guaranteed by design engineering

*2 The value of Hysteresis is calculated by the thermal Shutdown Temperature. It does not test.

ELECTRICAL CHARACTERISTICS (cont.)

$V_{CC5IN} = 5V$, $V_{CC3IN} = 3.3V$, unless otherwise noted.

The specification is guaranteed by design engineering at $-40^{\circ}C \leq Ta \leq 85^{\circ}C$. The typical value is in $Ta = 25^{\circ}C$.

$Ta=25^{\circ}C$

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|--------|---|------|------|------|---------|
| V_{CC} Turn-ON Delay Time ^{*2} | t1 | $V_{CC}=3.3V$ Time until 10% in 3.3V from EN. | 0.1 | 0.4 | 0.8 | ms |
| | t2 | $V_{CC}=5.0V$ Time until 10% in 5.0V from EN. | 0.15 | 0.45 | 1.0 | ms |
| V_{CC} Rising Time ^{*2} | t3 | $V_{CC}=3.3V$ Time until 90% from 10% in 3.3V. | 0.3 | 0.6 | 1.2 | ms |
| | t4 | $V_{CC}=5.0V$ Time until 90% from 10% in 5.0V. | 0.5 | 1.1 | 1.7 | ms |
| V_{CC} Turn-OFF Delay Time ^{*1,*2,*4} | t7 | $V_{CC}=3.3V$ Time until Hi-Z from EN. | 0.7 | 2 | 8.0 | ms |
| | t8 | $V_{CC}=5.0V$ Time until Hi-Z from EN | 0.9 | 2.1 | 6.0 | ms |
| V_{CC} Falling Time ^{*2} | t5 | $V_{CC}=3.3V$ Time until 10% from 90% in 3.3V. | 0.2 | 0.7 | 1.8 | ms |
| | t6 | $V_{CC}=5.0V$ Time until 10% from 90% in 5.0V. | 0.2 | 0.7 | 2.0 | ms |
| V_{PP} Turn-ON Deay Time ^{*3} | t9 | $V_{PP}=3.3V$ Time until 10% in 3.3V from EN. | 30 | 100 | 210 | μs |
| | t10 | $V_{PP}=5.0V$ Time until 10% in 5.0V from EN. | 40 | 120 | 230 | μs |
| V_{PP} Rising Time ^{*3} | t11 | $V_{PP}=3.3V$ Time until 90% from 10% in 3.3V. | 80 | 180 | 350 | μs |
| | t12 | $V_{PP}=5.0V$ Time until 90% from 10% in 5.0V. | 120 | 280 | 650 | μs |
| V_{PP} Turn-OFF Delay Time ^{*1,*3} | t15 | $V_{PP}=3.3V$ Time until Hi-Z from EN. | 20 | 50 | 160 | ns |
| | t16 | $V_{PP}=5.0V$ Time until Hi-Z from EN | 30 | 50 | 150 | ns |
| V_{PP} Falling Time ^{*3} | t13 | $V_{PP}=3.3V$ Time until 10% from 90% in 3.3V. | 10 | 30 | 80 | ns |
| | t14 | $V_{PP}=5.0V$ Time until 10% from 90% in 5.0V. | 10 | 30 | 80 | ns |

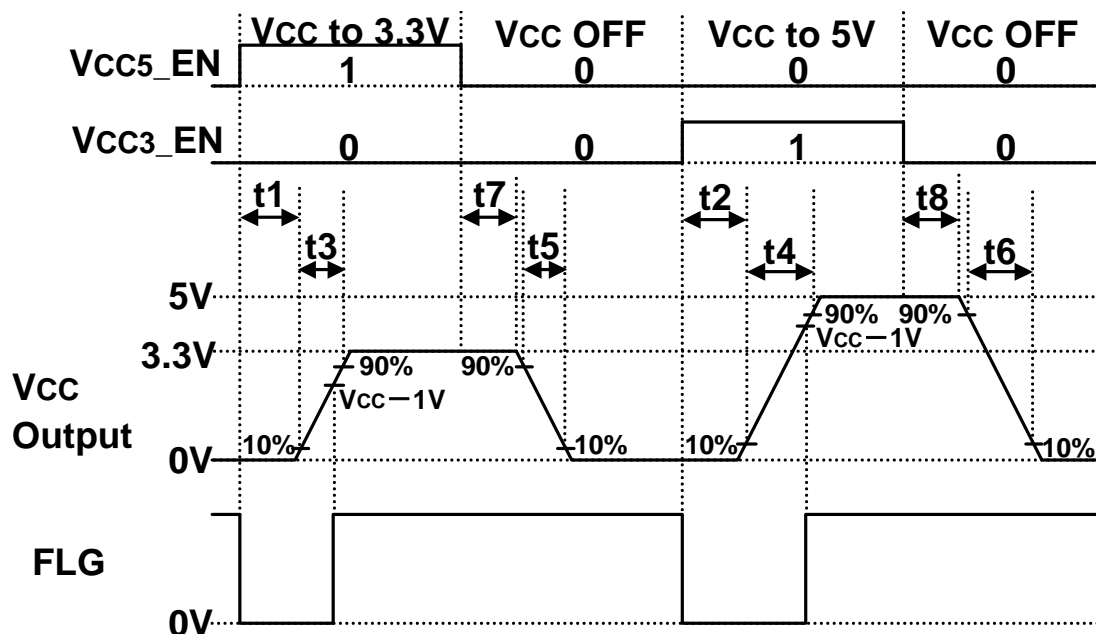
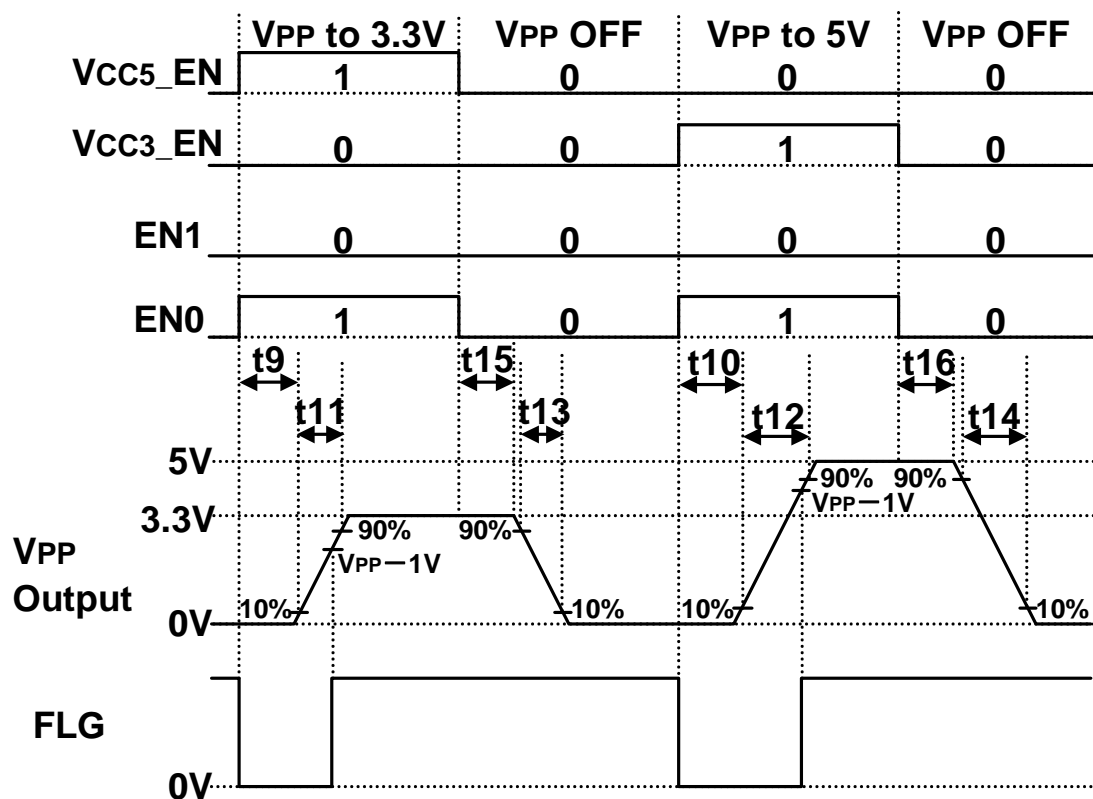
*1 The time between the beginning of falling time of the output from the change of EN.

*2 The measurement condition of t1 ~ t8: $RL = 10\Omega$

*3 The measurement condition of t9 ~ t16: $RL = 100\Omega$

*4 Please avoid the status on current limit or thermal shutdown during t7 and t8.

TIMING CHART

Fig1 Timing Diagram of V_{CC}Fig 2 Timing Diagram of V_{PP}

OPERATION

OPERATING EXPLANATION

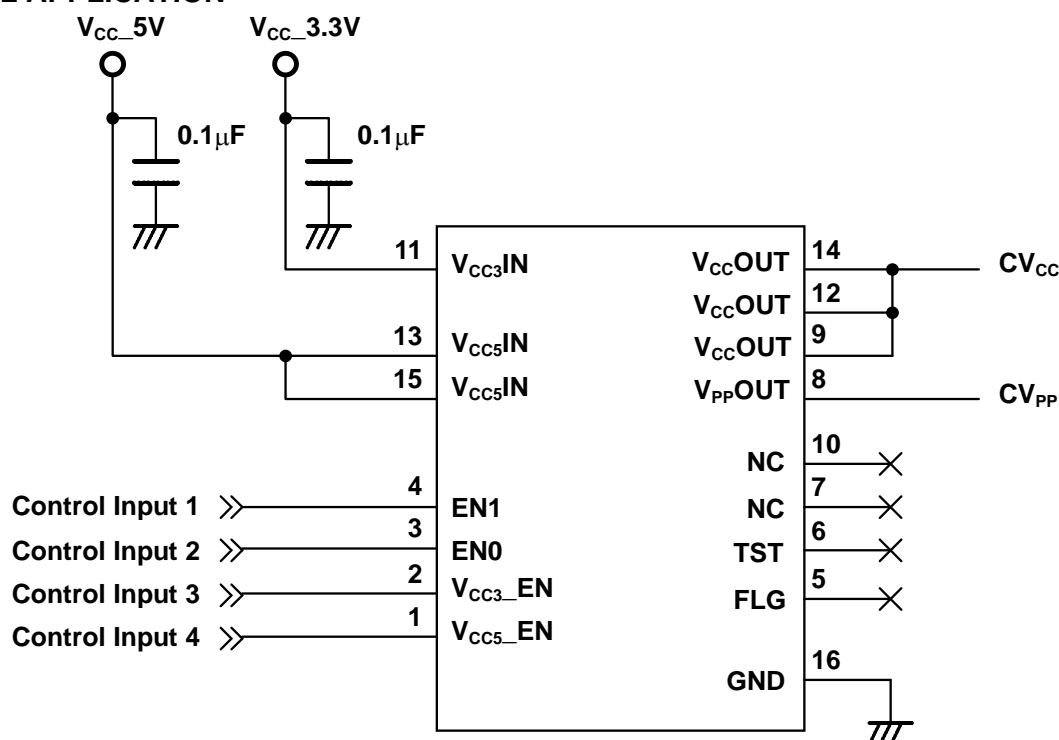
When the $V_{CCOUT}=0V$ is selected, the IC switches into the sleep mode, the supply current decreases to nano-amperes.

If commanded to switch from 5.0V to 3.3V, or vice versa from 3.3V to 5.0V, without selecting $V_{CCOUT}=0V$ between switching. In this case, enhancement of the second switch begins after the first is OFF, that is called as “the break-before-make switching”.

If the condition of the over-current limit caused by the OUT pin clamped to the GND were continue the temperature of the ICs would increase drastically. The switch-transistor is turned OFF if the temperature of the ICs becomes over 140°C (Typ.). And after this, the switch-transistor is turned ON again when the temperature of ICs decreased approximately 10°C. The switch-transistor keeps continual ON and OFF until either the switch is turned OFF or the OUT pin is removed from GND.

The Short Current Limit is fixed internal ICs. The response at the over-current is the following two types. (1) The ICs become constant current state immediately if the ICs are turned ON under the condition that the OUT pin is shorted or the large capacity is loaded. The current value in the state of constant current is the short current limit. (2) The large transient current flows until the current limit circuit responds, if the OUT pin is shorted or the large capacity is loaded under the condition that the switch-transistor is turned ON. The transient current is depending on the impedance from the power supply circuit of V_{CC5IN} / V_{CC3IN} to the output load. It means that the transient current depends upon the transient response characteristics of the power supply circuits of V_{CC5IN} / V_{CC3IN} , PCB layout or the card connector. After the current limit circuit is responded, the short current limit flows as the condition of constant current.

TYPICAL APPLICATION



Note: The signal from Control Input1~4 provided by PCMCIA control.

CONTROL LOGIC TABLE

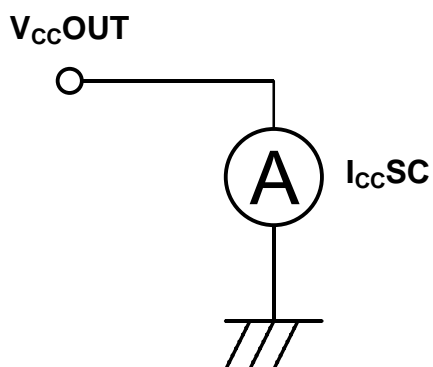
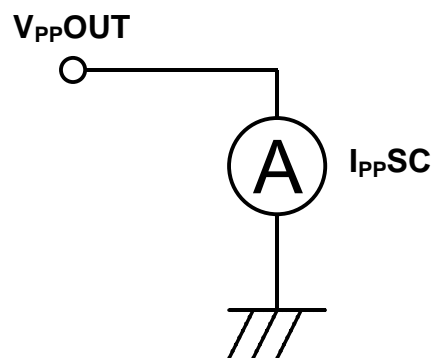
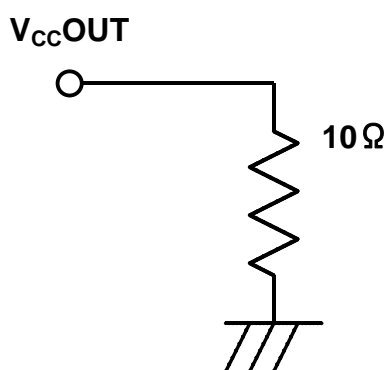
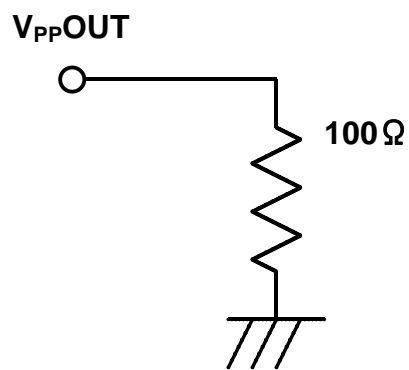
| V_{CC5_EN} | V_{CC3_EN} | EN1 | EN0 | V_{CCOUT} | V_{PPOUT} |
|---------------|---------------|-----|-----|-------------|-------------|
| 0 | 0 | 0 | 0 | 0 V | 0 V |
| 0 | 0 | 0 | 1 | 0 V | Hi-Z |
| 0 | 0 | 1 | 0 | 0 V | Hi-Z |
| 0 | 0 | 1 | 1 | 0 V | Hi-Z |
| 0 | 1 | 0 | 0 | 5 V | 0 V |
| 0 | 1 | 0 | 1 | 5 V | 5 V |
| 0 | 1 | 1 | 0 | 5 V | Hi-Z |
| 0 | 1 | 1 | 1 | 5 V | Hi-Z |
| 1 | 0 | 0 | 0 | 3.3 V | 0 V |
| 1 | 0 | 0 | 1 | 3.3 V | 3.3 V |
| 1 | 0 | 1 | 0 | 3.3 V | Hi-Z |
| 1 | 0 | 1 | 1 | 3.3 V | Hi-Z |
| 1 | 1 | 0 | 0 | 0 V | 0 V |
| 1 | 1 | 0 | 1 | 0 V | Hi-Z |
| 1 | 1 | 1 | 0 | 0 V | Hi-Z |
| 1 | 1 | 1 | 1 | 0 V | Hi-Z |

APPLICATION NOTES

Connect a by-pass capacitor value from 0.1 μ F to 1.0 μ F between V_{CC5IN} and GND pin, V_{CC3IN} and GND pin.
Please connect the same function pins to one another.

TST pin (Pin 6) should be OPEN.

TEST CIRCUITS

Fig.1 I_{CCSC} Fig.2 I_{PPSC} Fig.3 $t_1 \sim t_8$ Fig.3 $t_9 \sim t_{16}$

Note 1: The test circuits of all other pins, except V_{CCOUT} pin and V_{PPOUT} pins refer to the TYPICAL APPLTICATIONS (p.8).

Note 2: Please connect a $10k\Omega$ resistance with between FLG pin and V_{CC3IN} pin when the threshold of FLG pin voltage is testing.

TYPICAL CHARACTERISTICS

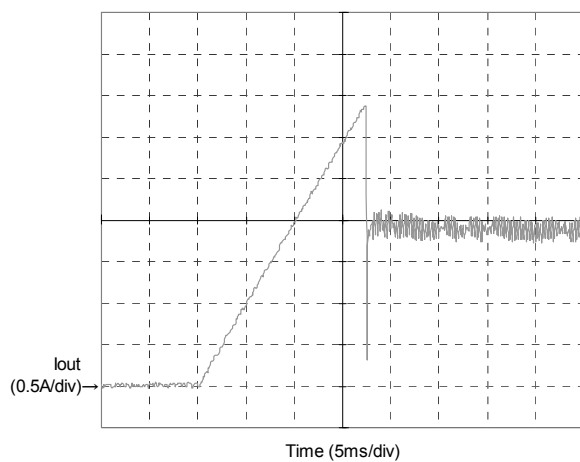


Fig.1 Ramped Load Connected to an Enabled Device

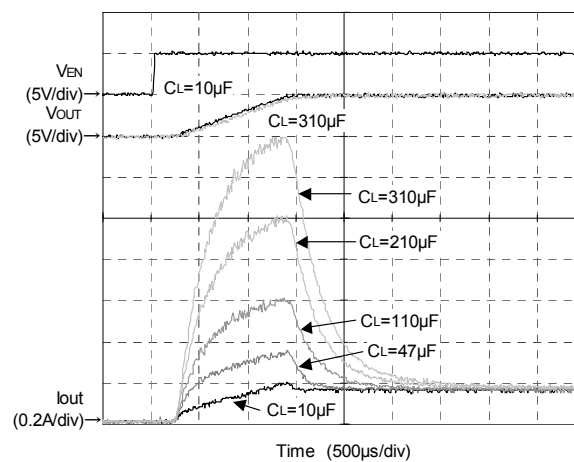


Fig.2 Rush Current



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