

**150mA Dual LDO REGULATOR**

NO.EA-089-120404

**OUTLINE**

The R5323x Series are CMOS-based voltage regulator ICs with high output voltage accuracy, low supply current, low dropout, and high ripple rejection. Each of these voltage regulator ICs consists of a voltage reference unit, an error amplifier, resistors for setting Output Voltage, a current limit circuit, and a chip enable circuit.

These ICs perform with low dropout voltage due to built-in transistor with low ON resistance, and a chip enable function prolongs the battery life of each system. The line transient response and load transient response of the R5323x Series are excellent, thus these ICs are very suitable for the power supply for hand-held communication equipment.

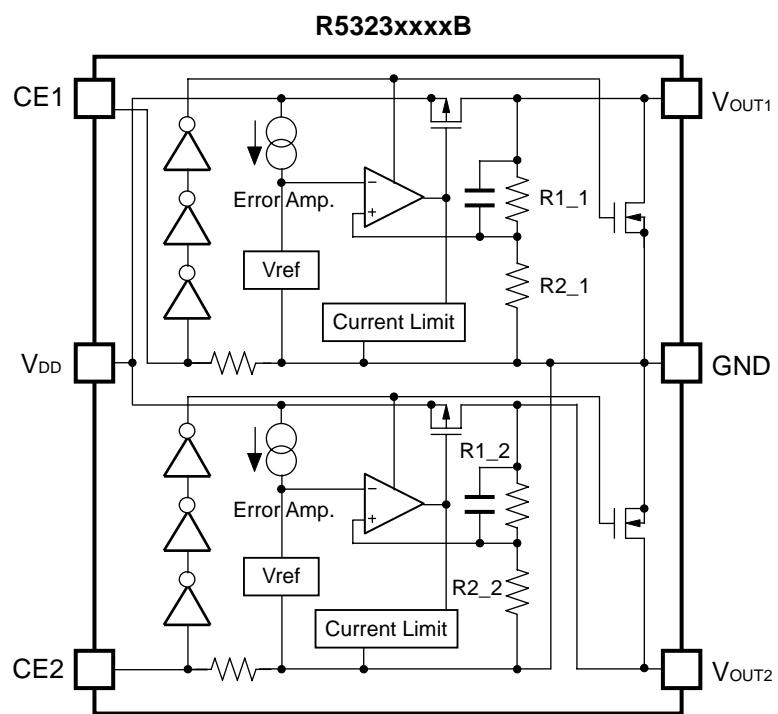
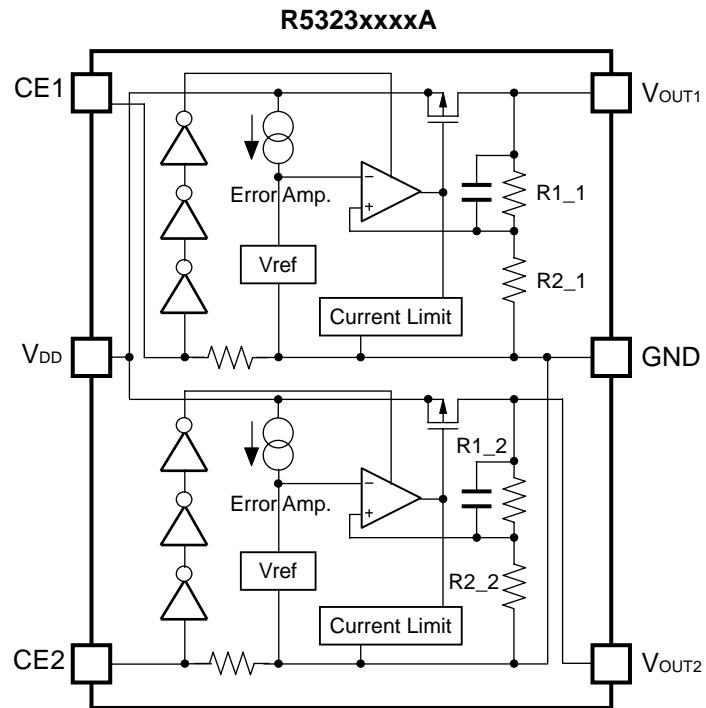
The output voltage of these ICs is internally fixed with high accuracy. Since the packages for these ICs are SOT-23-6 ([Limited](#)), DFN(PLP)1820-6 and WLCSP-6-P1 package, dual LDO regulators are included in each package, high density mounting of the ICs on boards is possible.

**FEATURES**

- Supply Current ..... Typ. 90 $\mu$ A (VR1, VR2)
- Standby Mode ..... Typ. 0.1 $\mu$ A (VR1, VR2)
- Dropout Voltage ..... Typ. 0.22V ( $I_{OUT}$ =150mA ,  $V_{OUT}$ =3.0V)
- Ripple Rejection ..... Typ.75dB( $V_{OUT}$  ≤ 2.4V),Typ.70dB( $V_{OUT}$  ≥ 2.5V), (f=1kHz)  
Typ.65dB( $V_{OUT}$  ≤ 2.4V),Typ.60dB( $V_{OUT}$  ≥ 2.5V), (f=10kHz)
- Input Voltage Range ..... 2.0V to 6.0V
- Output Voltage Range ..... 1.5V to 4.0V (0.1V steps)  
..... (For details, please refer to MARK INFORMATIONS.)
- Output Voltage Accuracy ..... ±2.0%
- Temperature-drift Coefficient of Output Voltage ..... Typ. ±100ppm/ $^{\circ}$ C
- Line Regulation ..... Typ.0.02%/V
- Built-in fold-back protection circuit ..... Typ. 40mA (Current at short mode)
- Packages ..... WLCSP-6-P1, DFN(PLP)1820-6, SOT-23-6 ([Limited](#))
- Ceramic Capacitor is recommended ..... 1.0 $\mu$ F or more
- Built-in chip enable circuit (A/B: active high)

**APPLICATIONS**

- Power source for handheld communication equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for battery-powered equipment.

**BLOCK DIAGRAMS**

## SELECTION GUIDE

The output voltage, auto discharge function, package, etc. for the ICs can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5323Zxxx*-TR-F	WLCSP-6-P1	3,000 pcs	Yes	Yes
R5323Kxxx*-TR	DFN(PLP)1820-6	3,000 pcs	Yes	Yes
R5323Nxxx*-TR-FE	SOT-23-6 ( <b>Limited</b> )	3,000 pcs	Yes	Yes

xxx : The combination of output voltage for each channel can be designated by serial numbers. (from 001)  
The output voltage for each channel can be set in the range from 1.5V to 4.0V in 0.1V steps.  
(For details, please refer to MARK INFORMATIONS.)

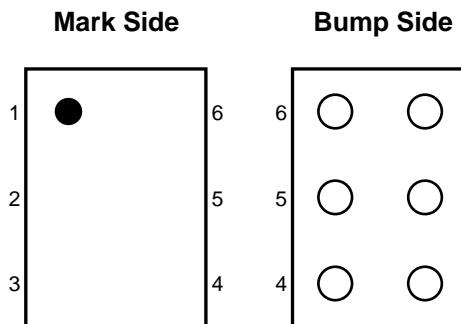
\* : The auto discharge function at off state are options as follows.  
(A) without auto discharge function at off state  
(B) with auto discharge function at off state

### The products scheduled to be discontinued (be sold to limited customer) : "Limited"

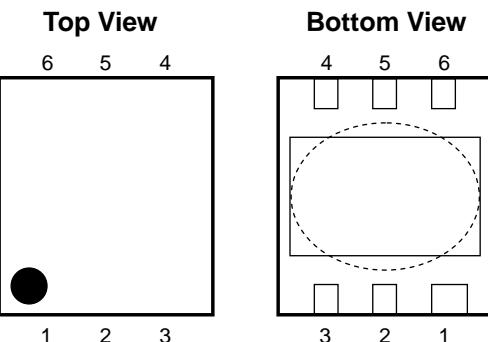
These products will be discontinued in the future. You can not select these products newly.  
We will provide these products to the customer who has been using or has ordered them before.  
But we recommend changing to other products as soon as possible.

## PIN CONFIGURATION

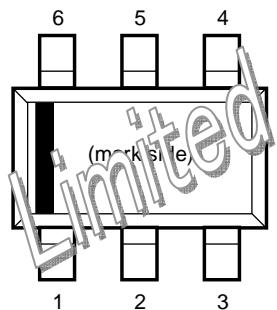
### • WLCSP-6-P1



### • DFN(PLP)1820-6



### • SOT-23-6



## PIN DESCRIPTIONS

### • WLCSP-6-P1

Pin No	Symbol	Pin Description
1	$V_{OUT1}$	Output Pin 1
2	$V_{DD}$	Input Pin
3	$V_{OUT2}$	Output Pin 2
4	CE2	Chip Enable Pin 2 ("H" Active)
5	GND	Ground Pin
6	CE1	Chip Enable Pin 1 ("H" Active)

### • DFN(PLP)1820-6

Pin No	Symbol	Pin Description
1	$V_{OUT2}$	Output Pin 2
2	$V_{DD}$	Input Pin
3	$V_{OUT1}$	Output Pin 1
4	GND	Ground Pin
5	CE1	Chip Enable Pin 1 ("H" Active)
6	CE2	Chip Enable Pin 2 ("H" Active)

\*) パッケージ裏面のタブの電位は基板電位(GND)です。  
GND端子と接続する(推奨)か、オーブンとしてください。

- SOT-23-6 (**Limited**)

Pin No	Symbol	Pin Description
1	V <sub>OUT1</sub>	Output Pin 1
2	V <sub>DD</sub>	Input Pin
3	V <sub>OUT2</sub>	Output Pin 2
4	CE2	Chip Enable Pin 2 ("H" Active)
5	GND	Ground Pin
6	CE1	Chip Enable Pin 1 ("H" Active)

## ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V <sub>IN</sub>	Input Voltage	6.5	V
V <sub>CE</sub>	Input Voltage (CE Pin)	-0.3 to 6.5	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>IN</sub> + 0.3	V
I <sub>OUT1</sub>	Output Current 1	200	mA
I <sub>OUT2</sub>	Output Current 2	200	mA
P <sub>D</sub>	Power Dissipation (WLCSP-6-P1)	633	mW
	Power Dissipation (DFN(PLP)1820-6) *	880	
	Power Dissipation (SOT-23-6) ( <b>Limited</b> )*	420	
T <sub>opt</sub>	Operating Temperature Range	-40 to 85	°C
T <sub>stg</sub>	Storage Temperature Range	-55 to 125	°C

\*) For Power Dissipation, please refer to PACKAGE INFORMATION.

### ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.

The functional operation at or over these absolute maximum ratings is not assured.

### RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

## ELECTRICAL CHARACTERISTICS

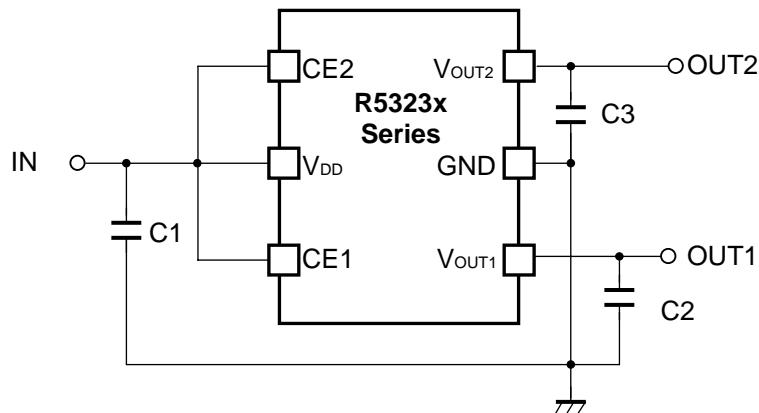
- R5323xxxxA/B

Topt=25°C

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V <sub>OUT</sub>	Output voltage	V <sub>IN</sub> -V <sub>OUT</sub> =1.0V 1mA ≤ I <sub>OUT</sub> ≤ 30mA		×0.98		×1.02	V
I <sub>OUT</sub>	Output Current	V <sub>IN</sub> -V <sub>OUT</sub> =1.0V		150			mA
ΔV <sub>OUT</sub> / ΔI <sub>OUT</sub>	Load regulation	V <sub>IN</sub> =Set V <sub>OUT</sub> +1V 1mA ≤ I <sub>OUT</sub> ≤ 150mA			15	40	mV
V <sub>DIF</sub>	Dropout Voltage	I <sub>OUT</sub> =150mA	V <sub>OUT</sub> =1.5		0.38	0.70	V
			V <sub>OUT</sub> =1.6		0.35	0.65	
			V <sub>OUT</sub> =1.7		0.33	0.60	
			1.8V ≤ V <sub>OUT</sub> ≤ 2.0V		0.32	0.55	
			2.1V ≤ V <sub>OUT</sub> ≤ 2.7V		0.28	0.50	
			2.8V ≤ V <sub>OUT</sub> ≤ 4.0V		0.22	0.35	
I <sub>SS</sub>	Supply Current	V <sub>IN</sub> -V <sub>OUT</sub> =1.0V			90	120	μA
I <sub>standby</sub>	Standby Current	V <sub>IN</sub> -V <sub>OUT</sub> =1.0V V <sub>CE</sub> =GND			0.1	1.0	μA
ΔV <sub>OUT</sub> / ΔV <sub>IN</sub>	Line regulation	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 6.0V I <sub>OUT</sub> =30mA			0.02	0.10	%/V
RR	Ripple Rejection	Ripple 0.5Vp-p V <sub>IN</sub> -V <sub>OUT</sub> =1.0V, I <sub>OUT</sub> =30mA (In case that V <sub>OUT</sub> ≤ 1.7V, V <sub>IN</sub> -V <sub>OUT</sub> =1.2V, I <sub>OUT</sub> =30mA)	f=1kHz		75 *Note1		dB
			f=10kHz		65 *Note2		
V <sub>IN</sub>	Input Voltage			2.0		6.0	V
ΔV <sub>out</sub> / ΔT <sub>opt</sub>	Output Voltage Temperature Coefficient	I <sub>OUT</sub> =30mA -40°C ≤ T <sub>opt</sub> ≤ 85°C			±100		ppm /°C
I <sub>sc</sub>	Short Current Limit	V <sub>OUT</sub> =0V			40		mA
R <sub>PD</sub>	Pull-down resistance for CE pin			0.7	2.0	8.0	MΩ
V <sub>CEH</sub>	CE Input Voltage "H"			1.5		6.0	V
V <sub>CEL</sub>	CE Input Voltage "L"			0		0.3	V
en	Output Noise	BW=10Hz to 100kHz			30		μVrms
R <sub>LOW</sub>	Low Output Nch Tr. ON Resistance (of B version)	V <sub>CE</sub> =0V			60		Ω

\*Note1: f=1kHz, 70dB as to V<sub>OUT</sub> ≥ 2.5V Output type.\*Note2: f=10kHz, 60dB as to V<sub>OUT</sub> ≥ 2.5V Output type.

## TYPICAL APPLICATION



C1=C2=C3=Ceramic 1.0 $\mu$ F

## TECHNICAL NOTES

When using these ICs, consider the following points:

### Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor C2 and C3 with good frequency characteristics and ESR (Equivalent Series Resistance).

(Note: If additional ceramic capacitors are connected with parallel to the output pin with an output capacitor for phase compensation, the operation might be unstable. Because of this, test these ICs with as same external components as ones to be used on the PCB.)

### PCB Layout

Make V<sub>DD</sub> and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor C1 with a capacitance value as much as 1.0 $\mu$ F or more between V<sub>DD</sub> and GND pin, and as close as possible to the pins.

Set external components, especially the output capacitor C2 and C3, as close as possible to the ICs, and make wiring as short as possible.

## TEST CIRCUIT

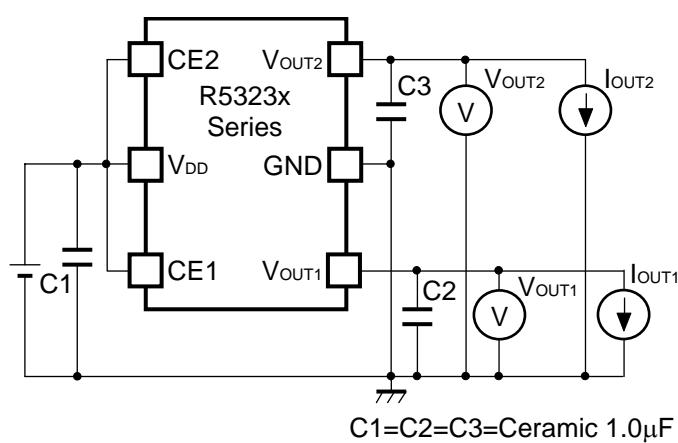


Fig.1 Standard test Circuit

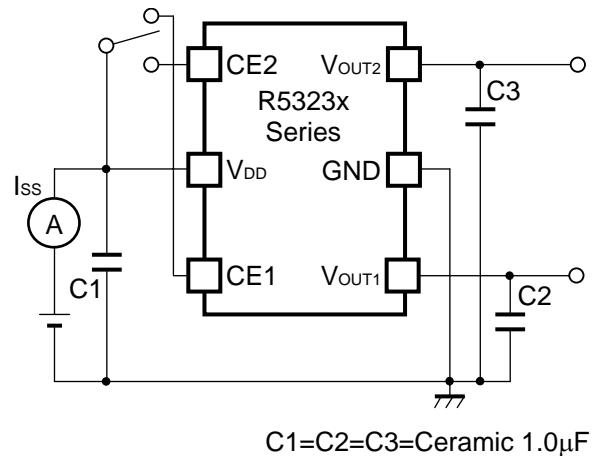


Fig.2 Supply Current Test Circuit

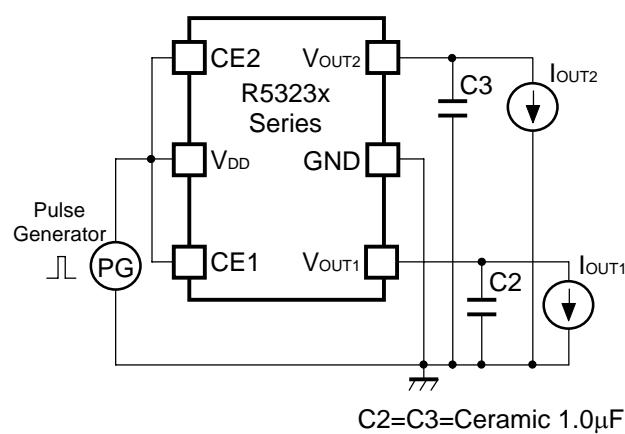


Fig.3 Ripple Rejection, Line Transient Response Test Circuit

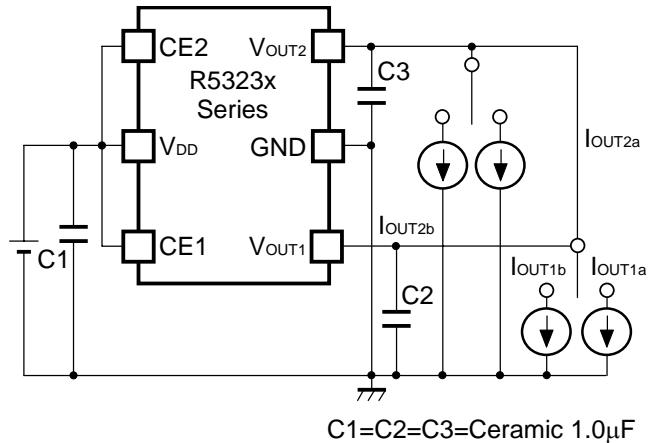
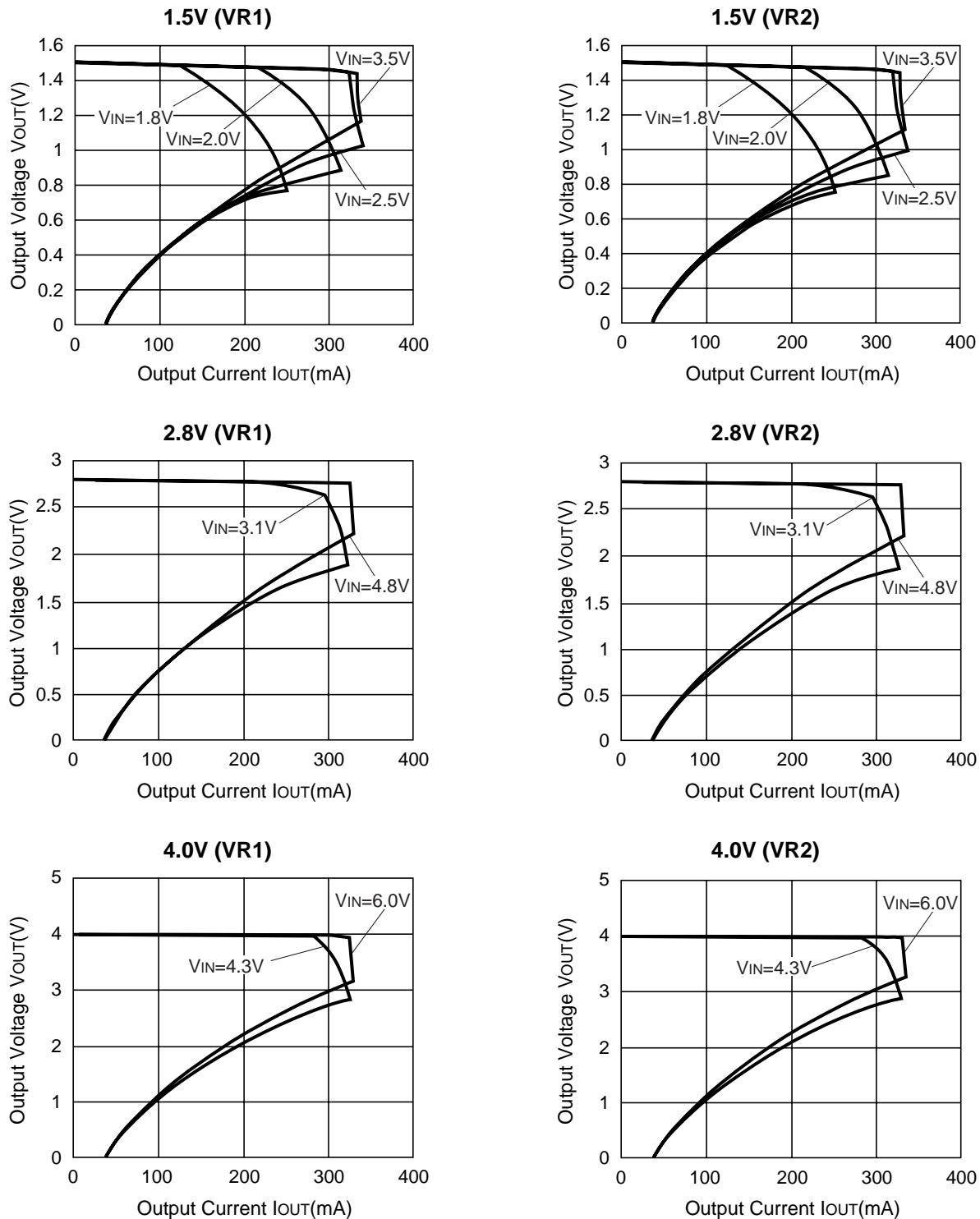


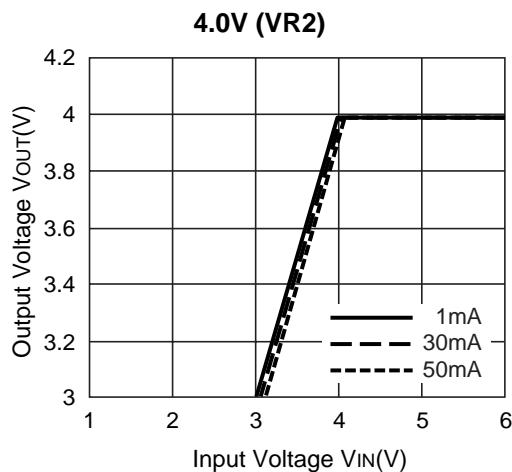
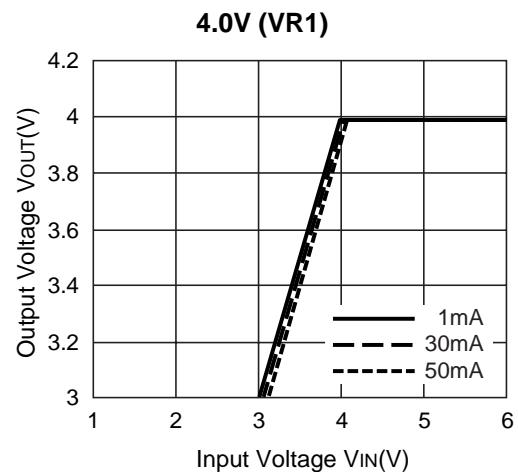
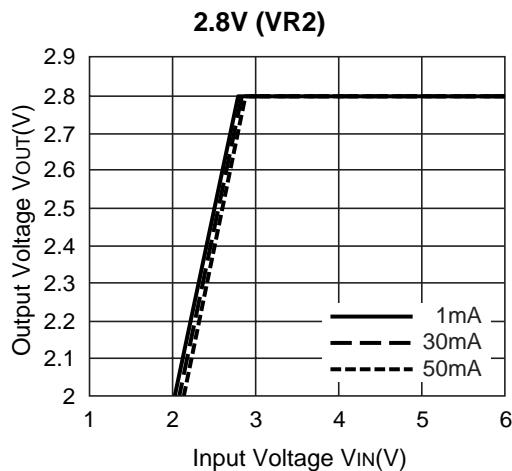
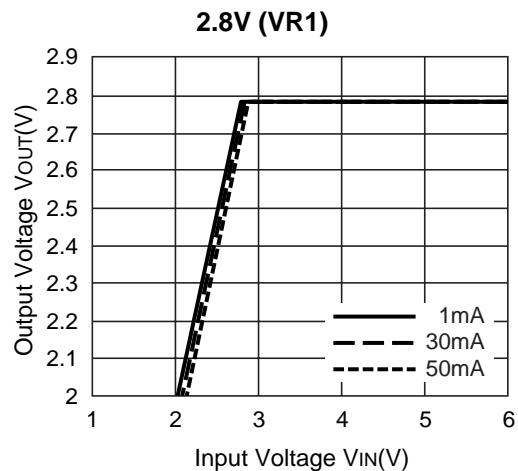
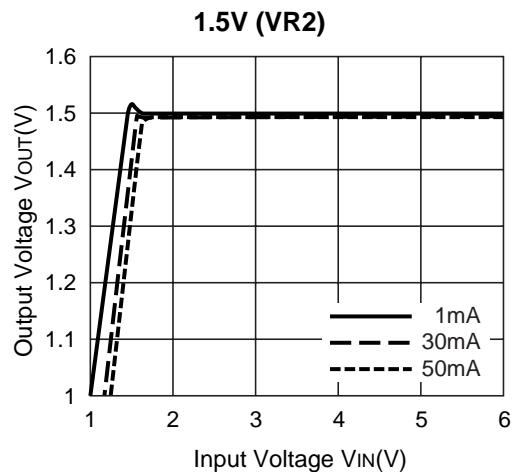
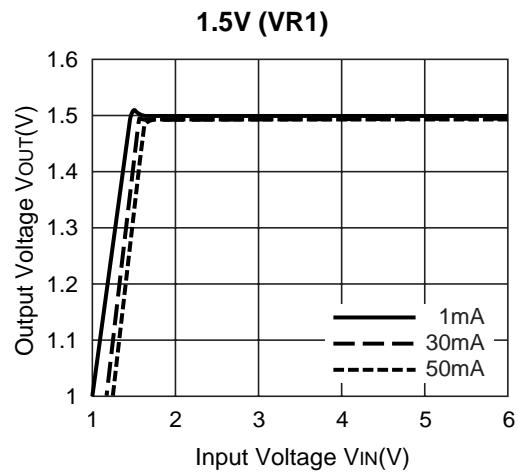
Fig.4 Load Transient Response Test Circuit

## TYPICAL CHARACTERISTICS

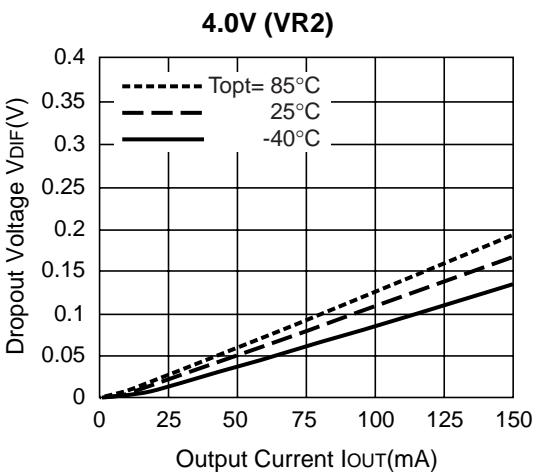
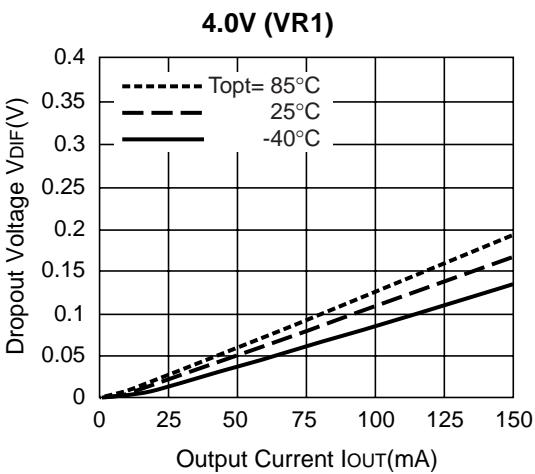
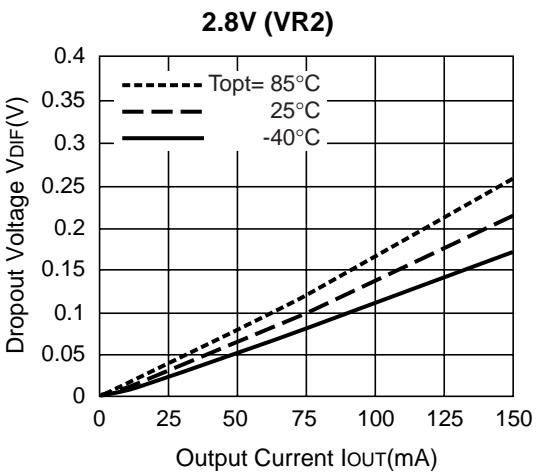
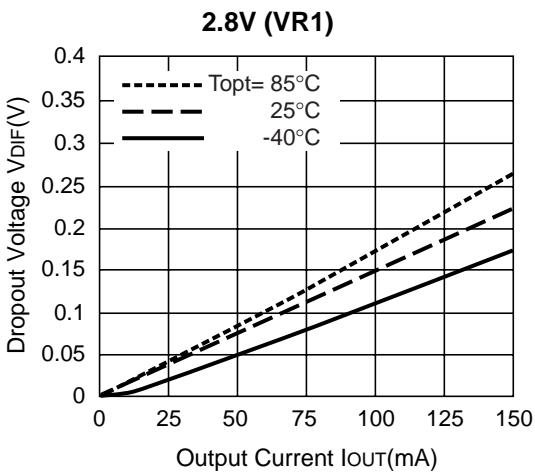
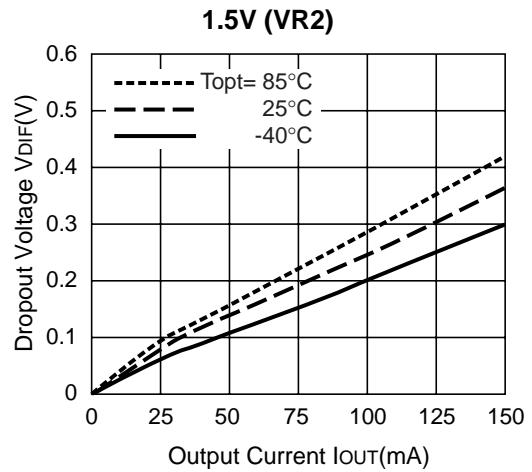
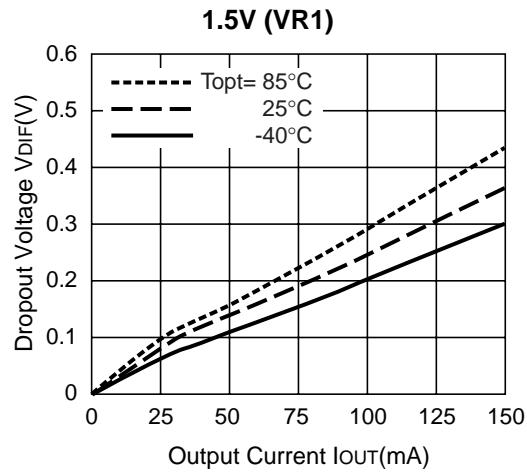
### 1) Output Voltage vs. Output Current ( $T_{opt}=25^{\circ}\text{C}$ )



**2) Output Voltage vs. Input Voltage ( $T_{opt}=25^{\circ}\text{C}$ )**

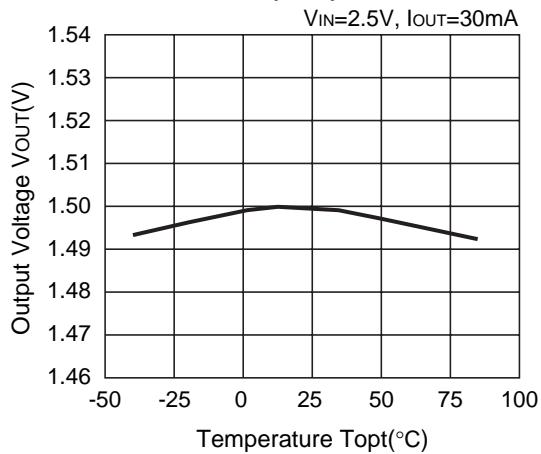


### 3) Dropout Voltage vs. Output Current

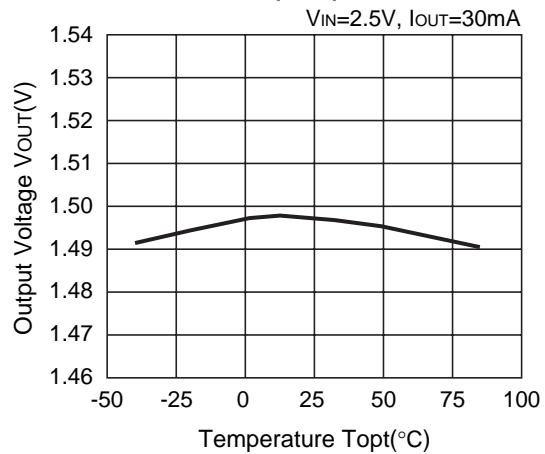


#### 4) Output Voltage vs. Temperature

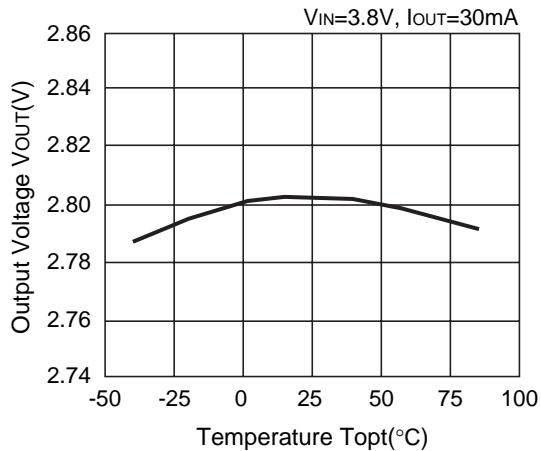
**1.5V (VR1)**



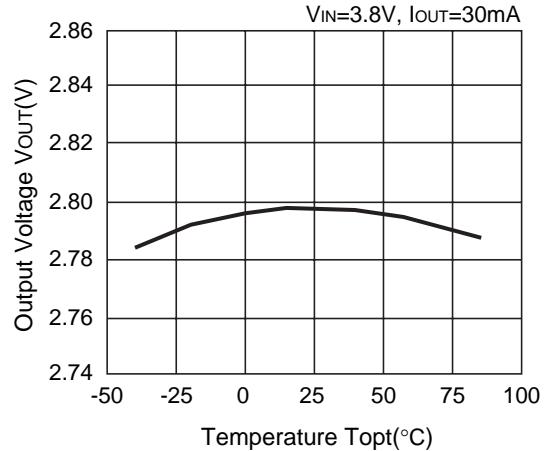
**1.5V (VR2)**



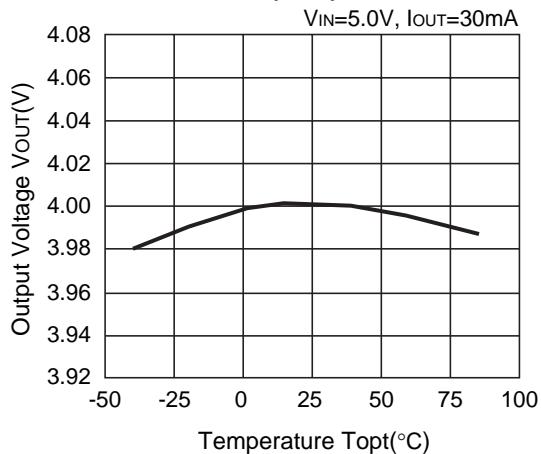
**2.8V (VR1)**



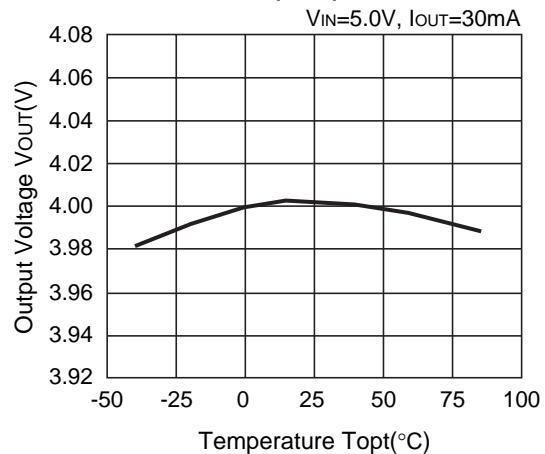
**2.8V (VR2)**



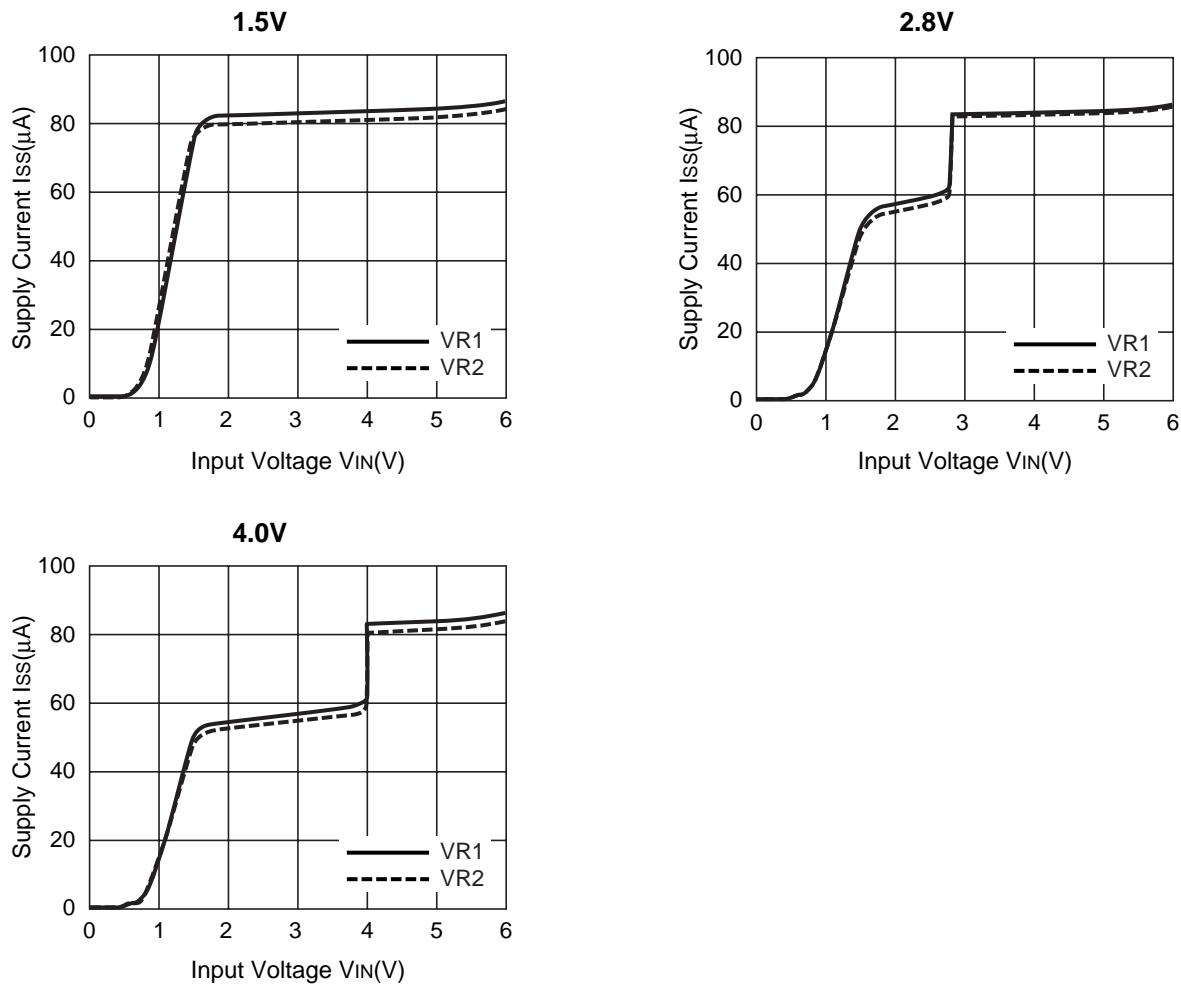
**4.0V (VR1)**



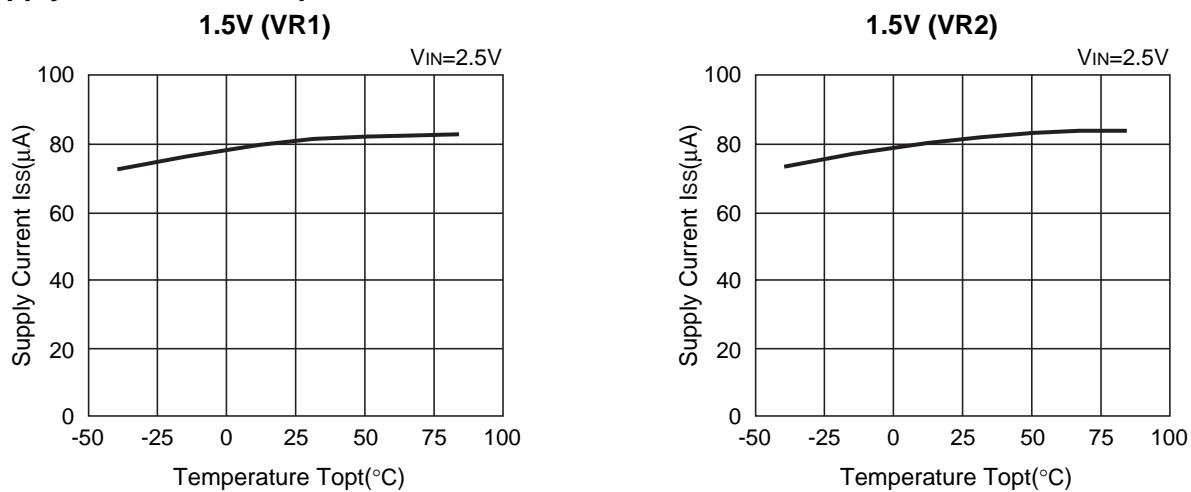
**4.0V (VR2)**

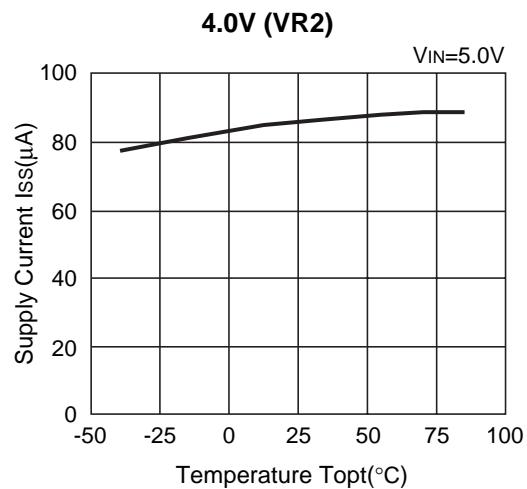
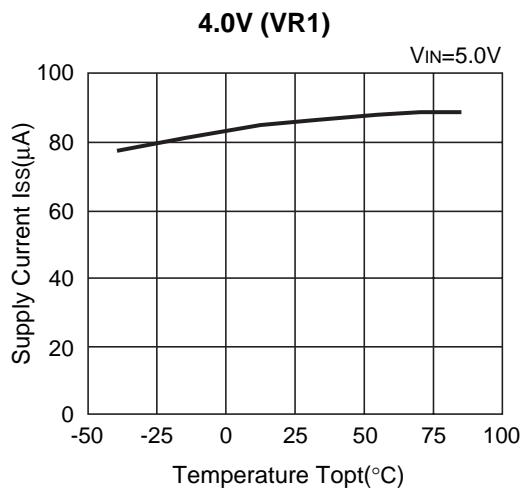
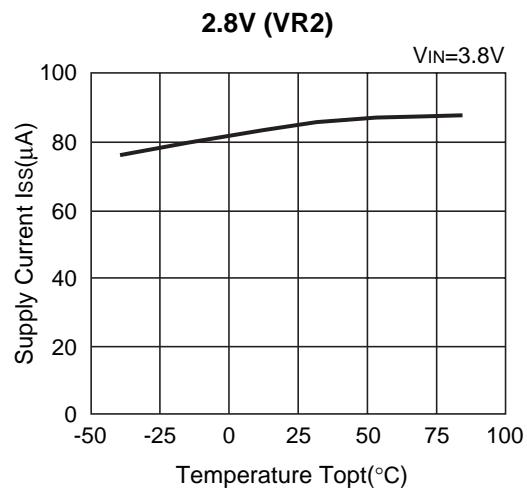
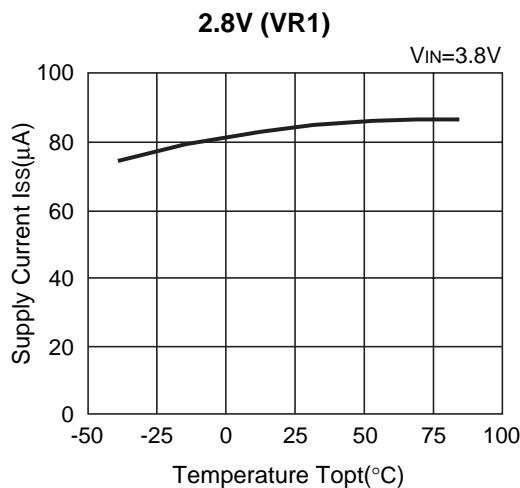


### 5) Supply Current vs. Input Voltage ( $T_{opt}=25^{\circ}\text{C}$ )

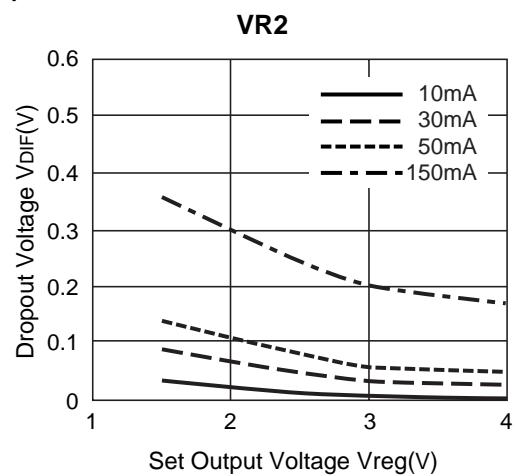
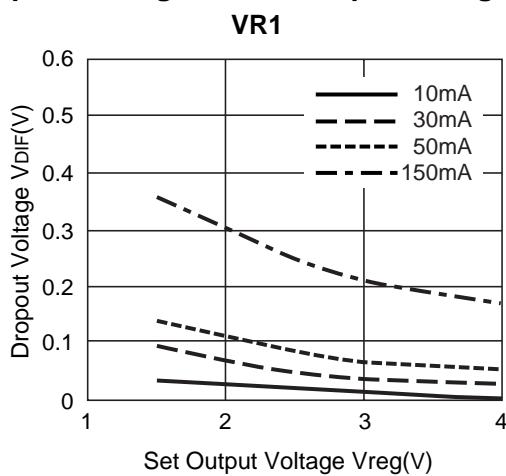


### 6) Supply Current vs. Temperature

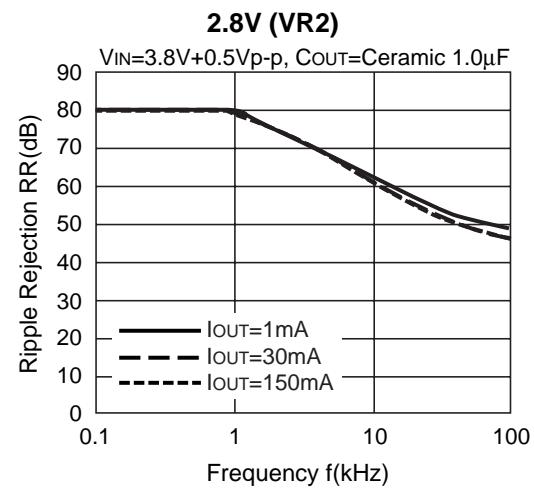
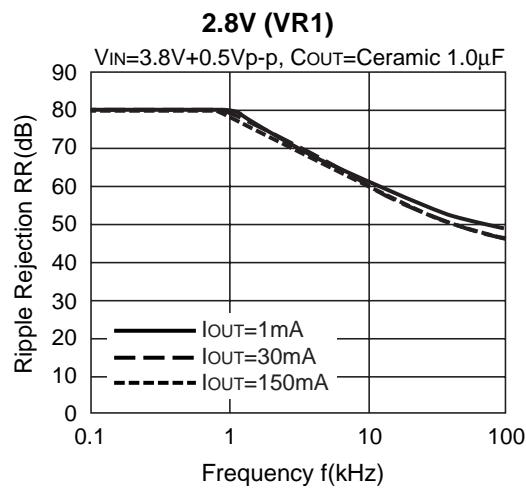
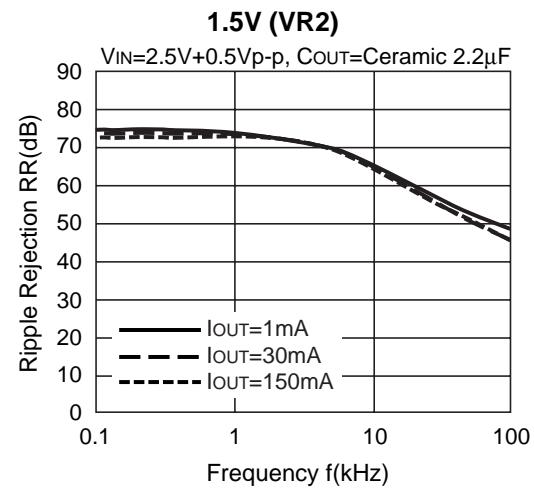
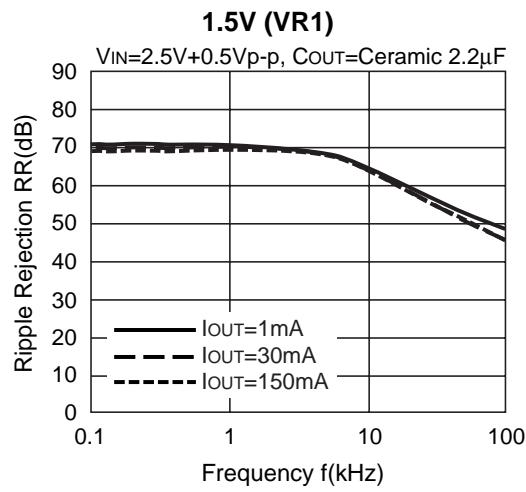
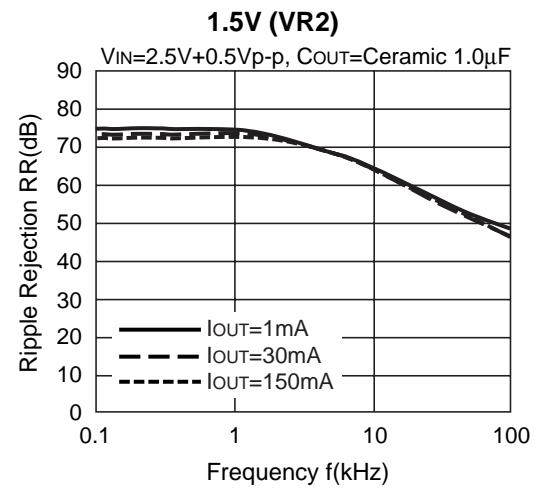
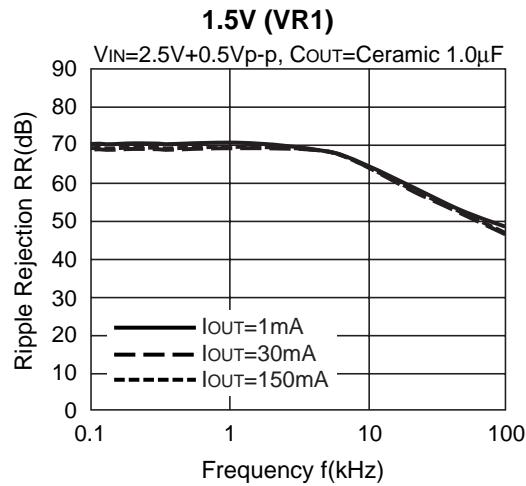


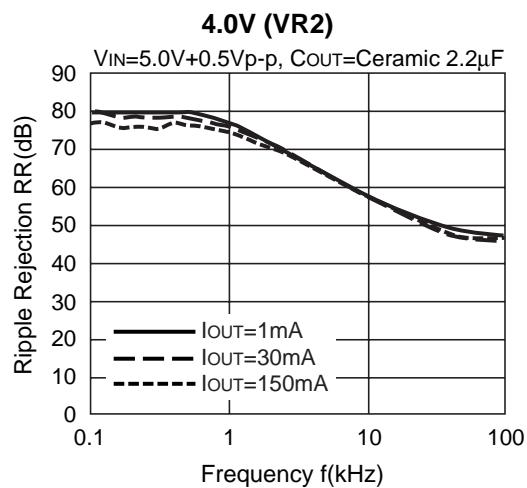
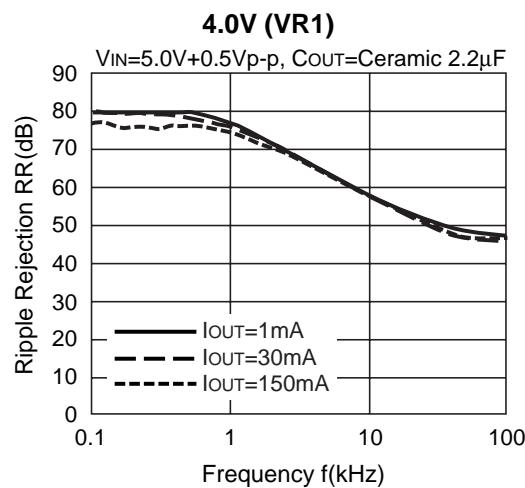
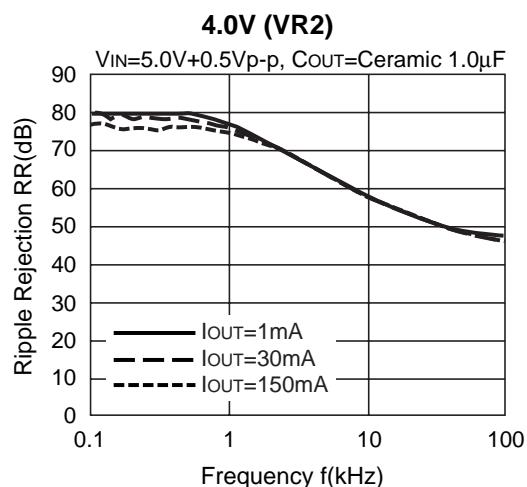
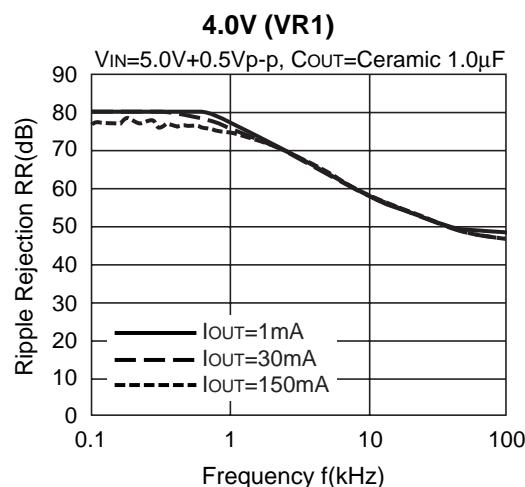
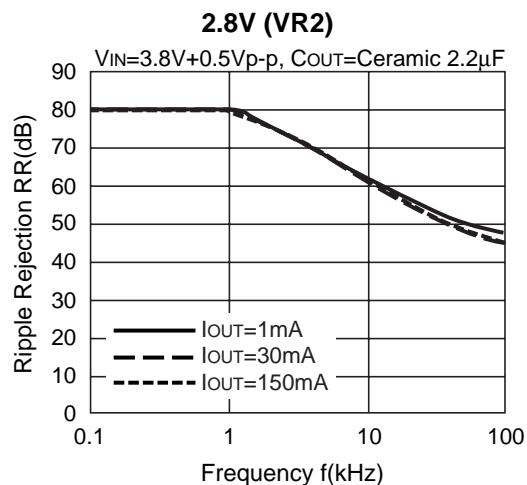
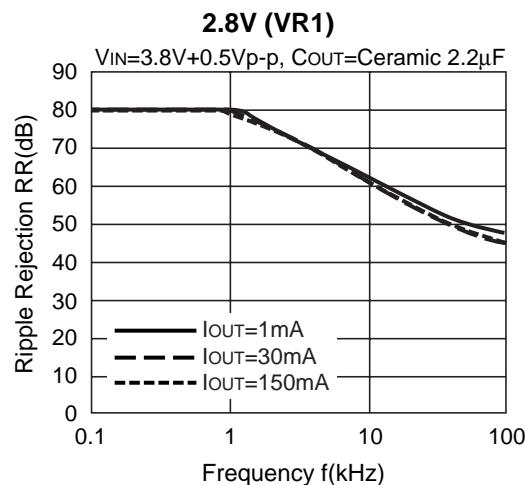


### 7) Dropout Voltage vs. Set Output Voltage ( $T_{opt}=25^{\circ}C$ )

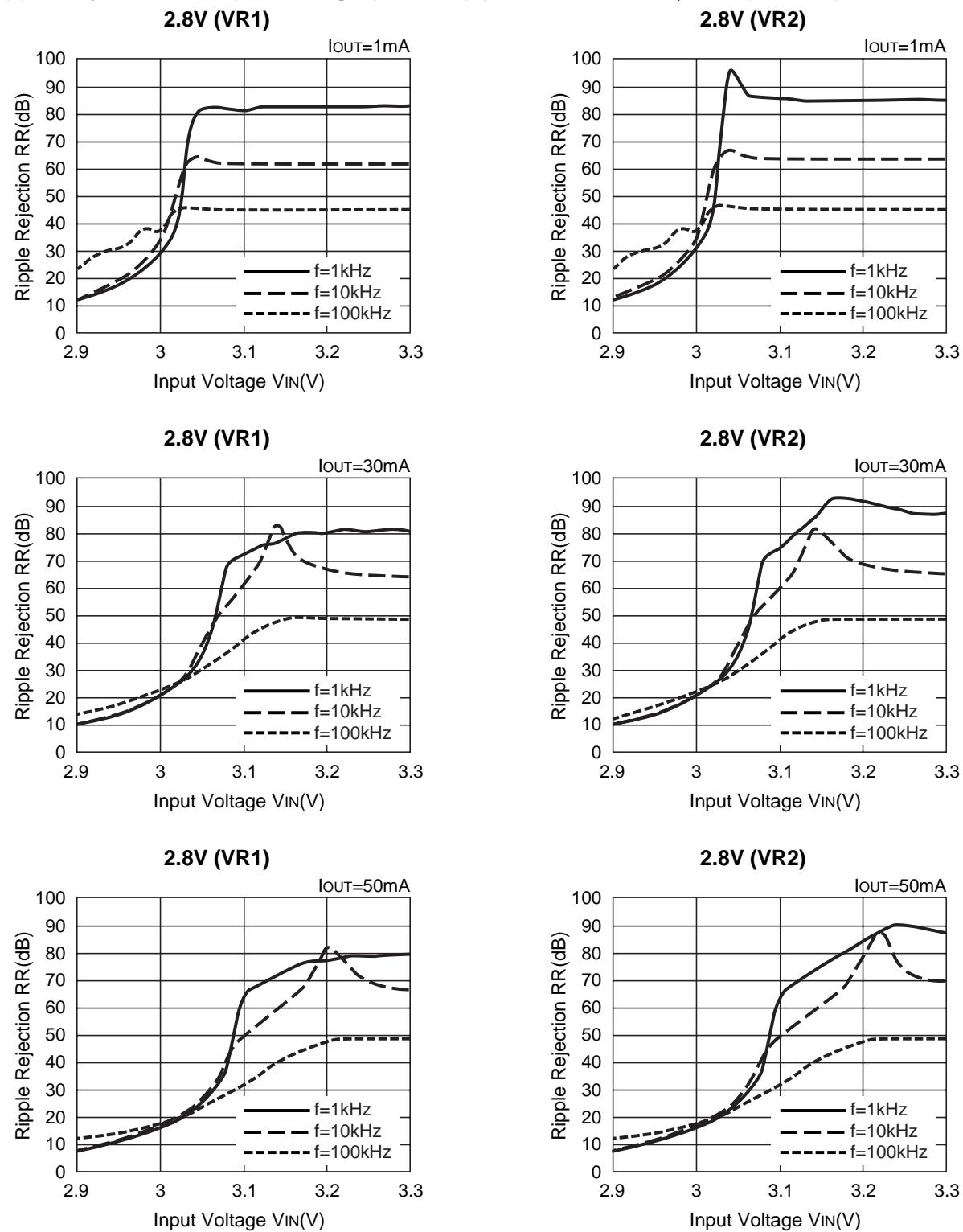


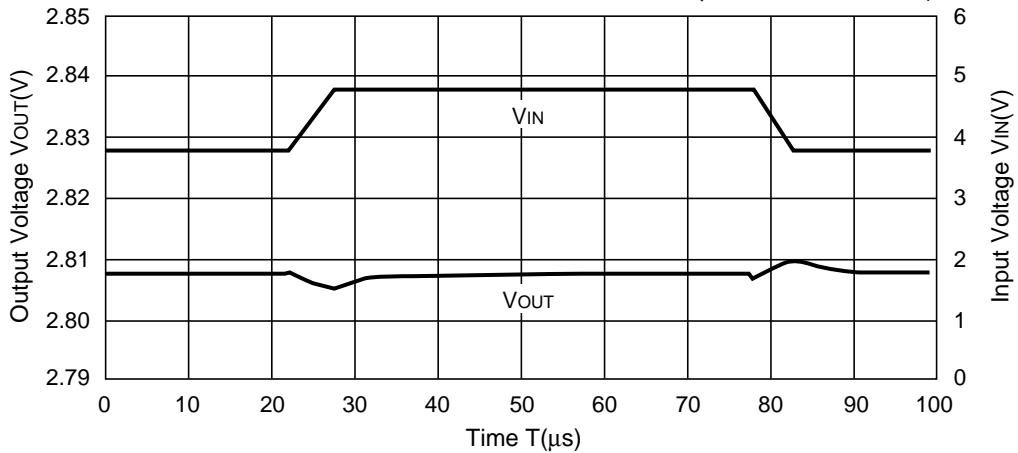
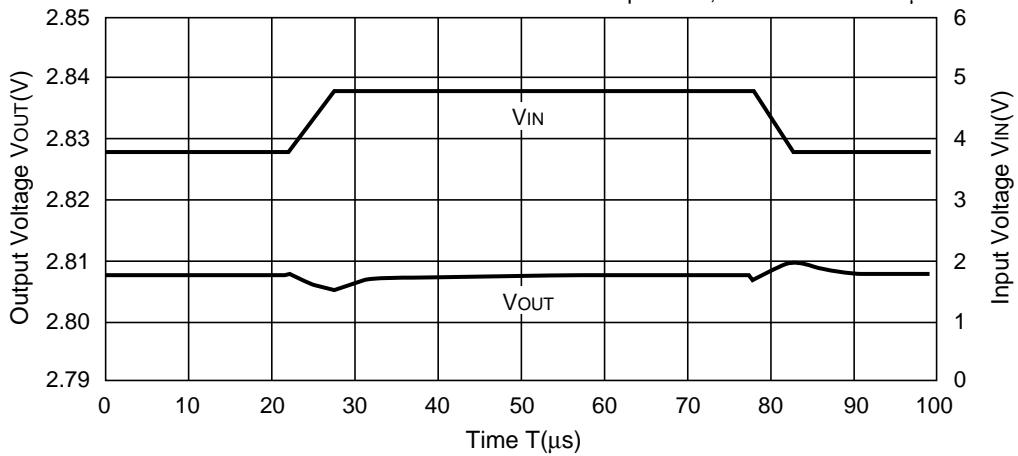
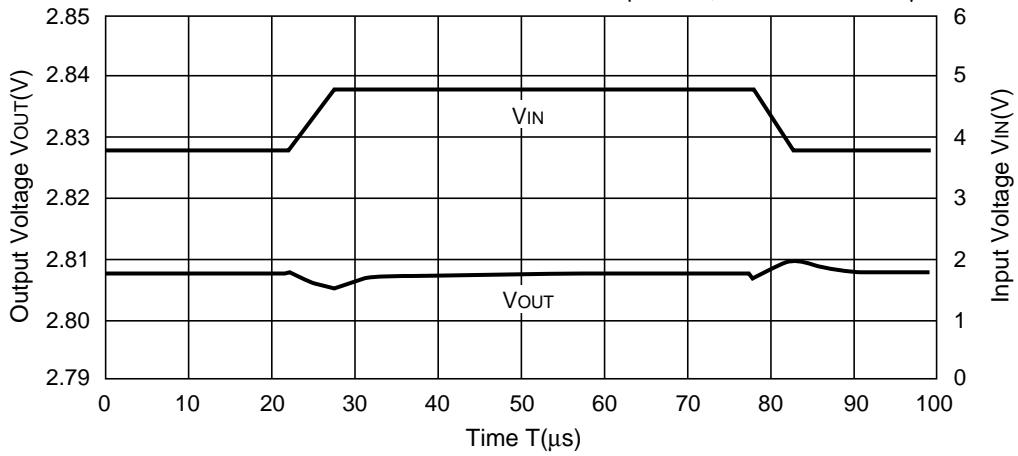
### 8) Ripple Rejection vs. Frequency ( $T_{opt}=25^{\circ}\text{C}$ )

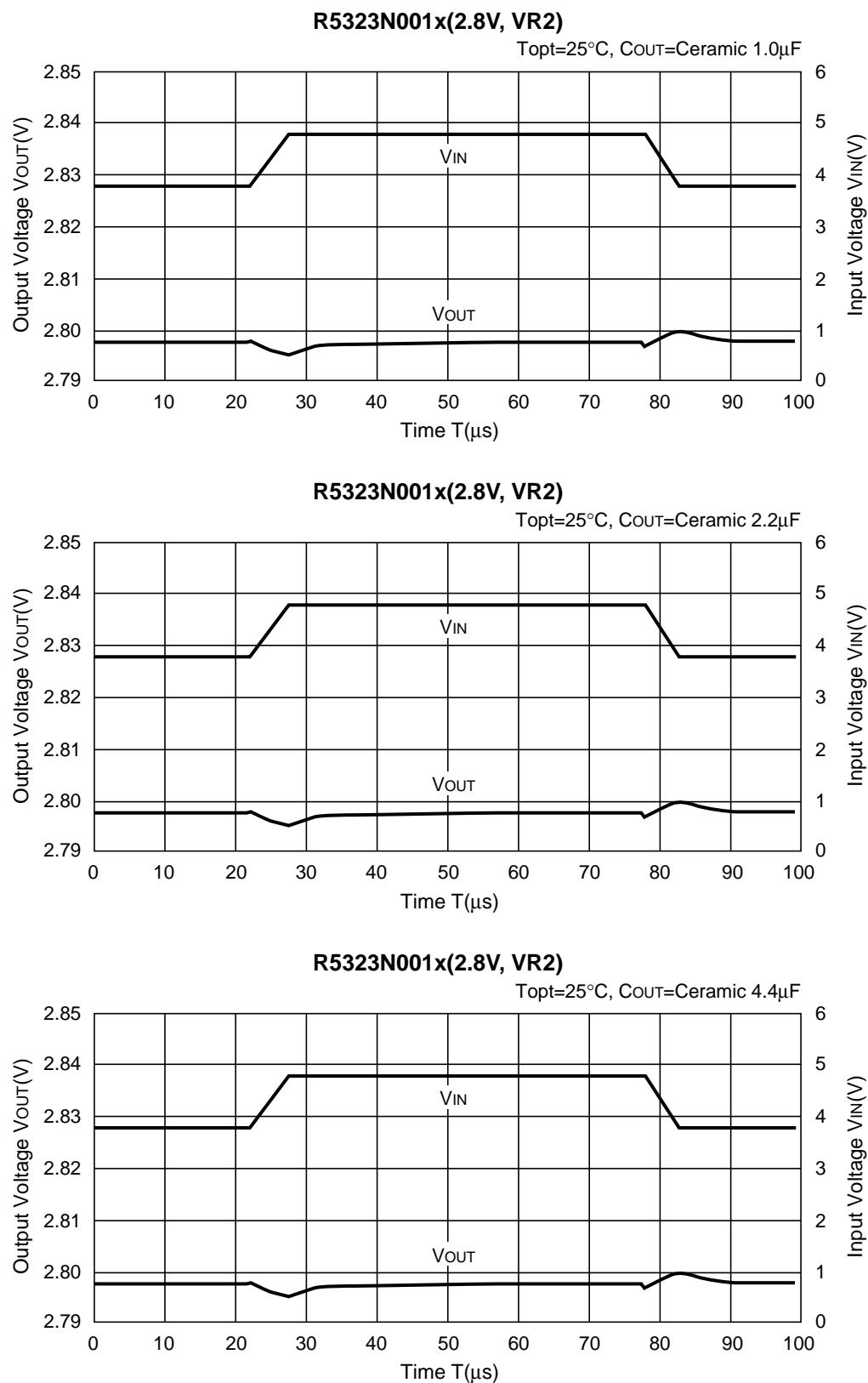




**9) Ripple Rejection vs. Input Voltage (DC bias) ( $C_{OUT}$ =Ceramic  $1.0\mu F$ ,  $T_{opt}=25^{\circ}C$ )**

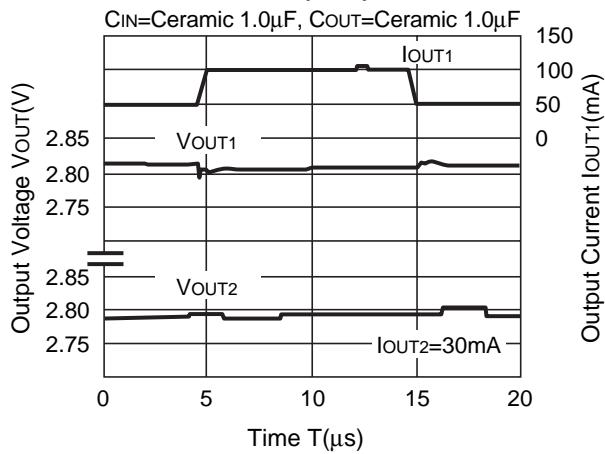


**10) Input Transient Response ( $I_{OUT}=30mA$ ,  $tr=tf=5\mu s$ )****R5323N001x(2.8V, VR1)** $I_{OUT}=30mA$ ,  $tr=tf=5\mu s$ ,  $C_{OUT}=\text{Ceramic } 1.0\mu F$ **R5323N001x(2.8V, VR1)** $T_{opt}=25^{\circ}\text{C}$ ,  $C_{OUT}=\text{Ceramic } 2.2\mu F$ **R5323N001x(2.8V, VR1)** $T_{opt}=25^{\circ}\text{C}$ ,  $C_{OUT}=\text{Ceramic } 4.4\mu F$ 

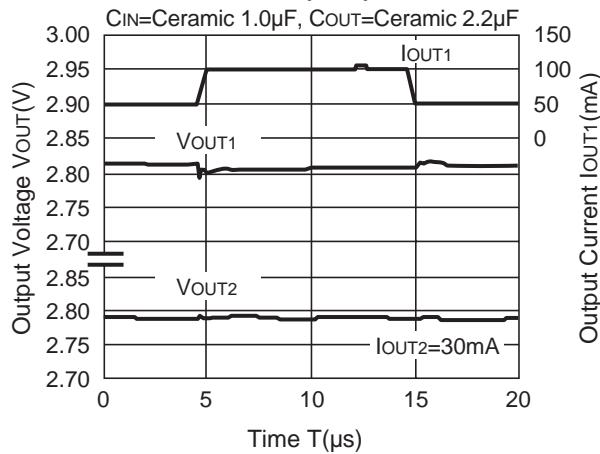


### 11) Load Transient Response

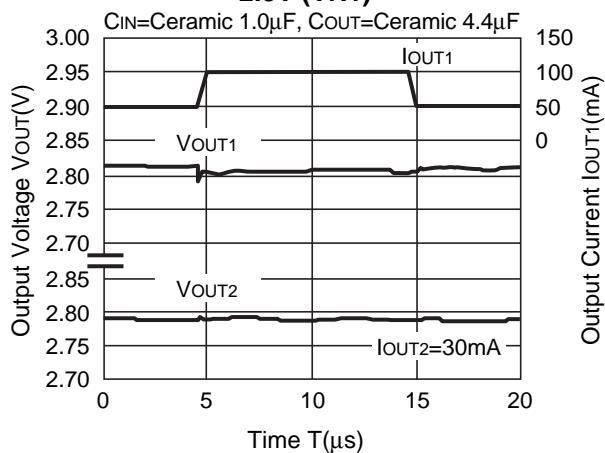
**2.8V (VR1)**



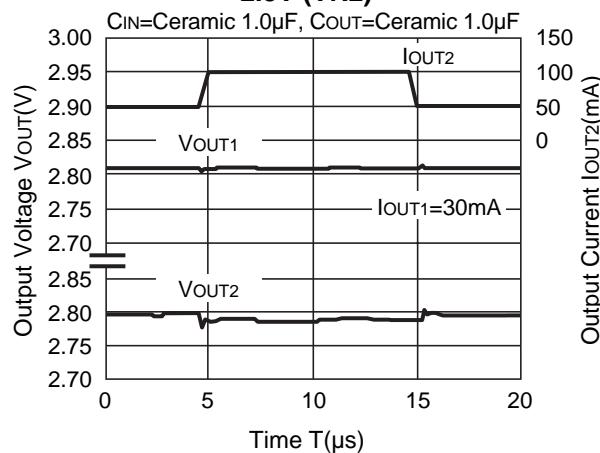
**2.8V (VR1)**



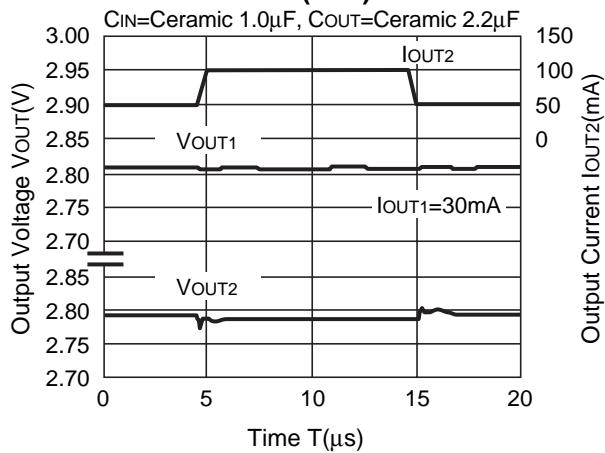
**2.8V (VR1)**



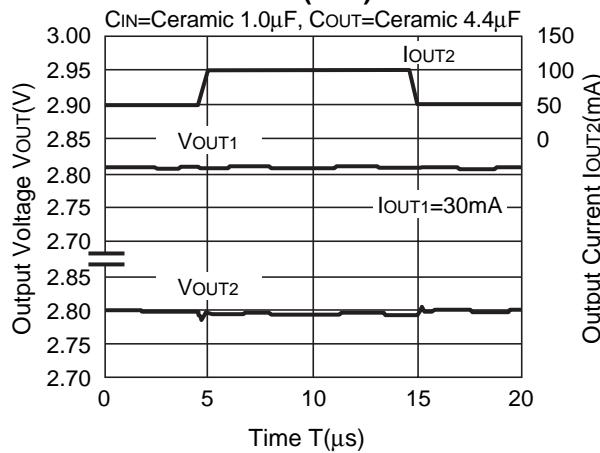
**2.8V (VR2)**



**2.8V (VR2)**

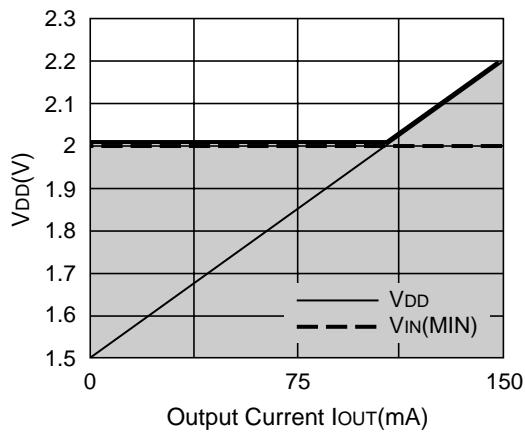


**2.8V (VR2)**



## 12) Minimum Operating Voltage

### 1.5V Minimum Operating Voltage Range



## ESR vs. Output Current

When using these ICs, consider the following points:

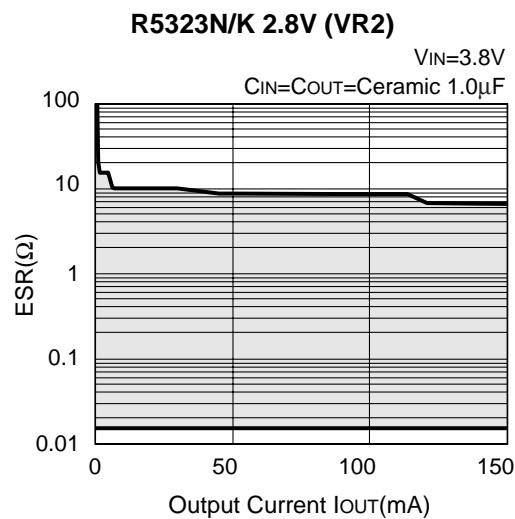
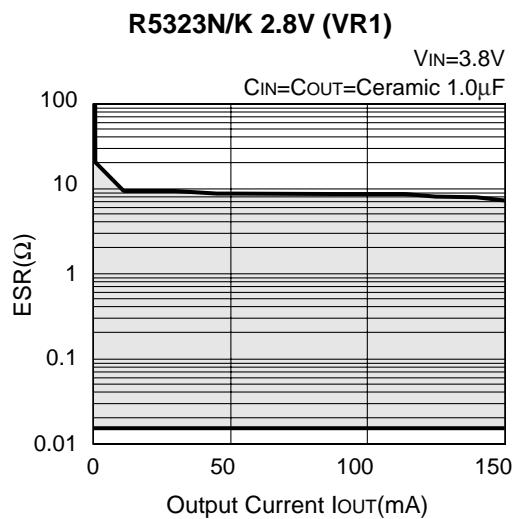
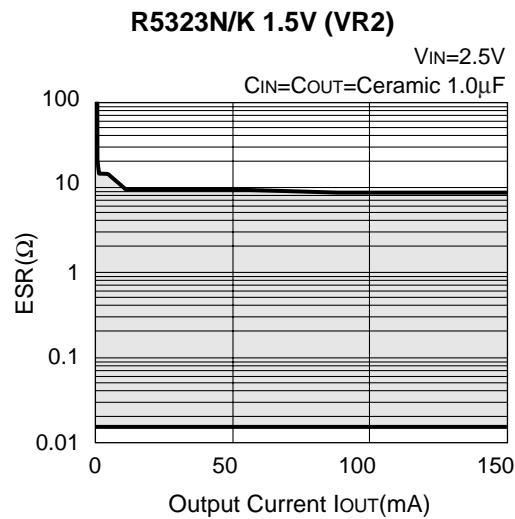
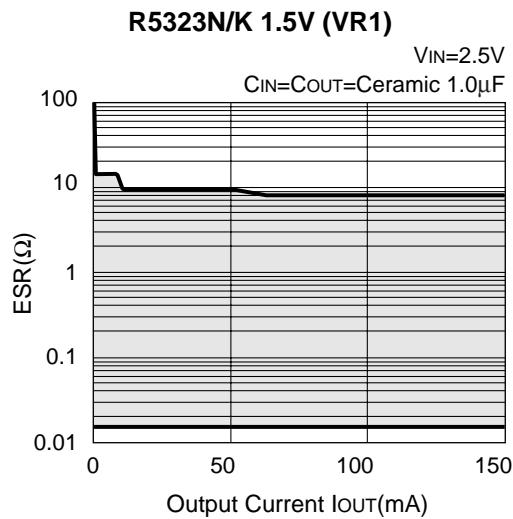
The relations between  $I_{OUT}$  (Output Current) and ESR of an output capacitor are shown below.

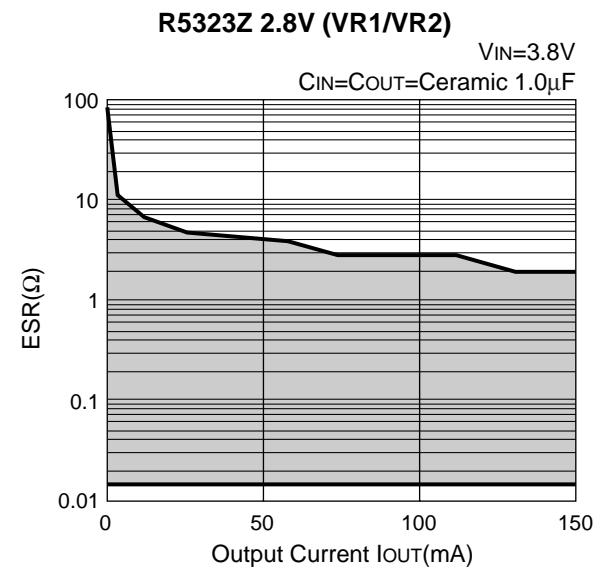
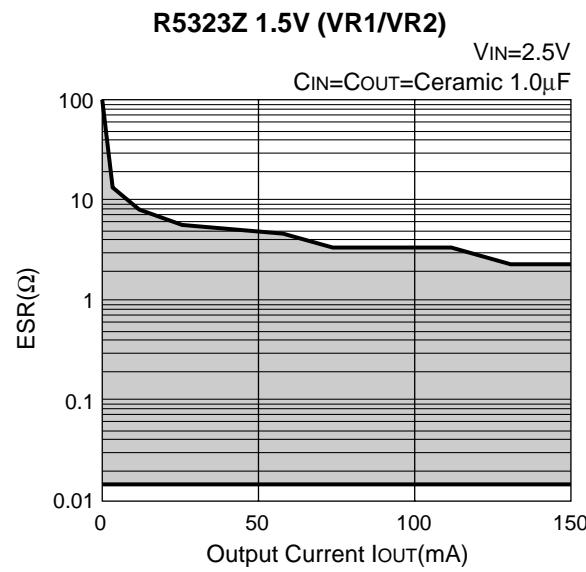
The conditions when the white noise level is under  $40\mu V$  (Avg.) are marked as the hatched area in the graph.

### Measurement conditions

Frequency Band : 10Hz to 2MHz (BW=30Hz)

Temperature :  $25^{\circ}C$







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