RICOH

R5109G SERIES

Microprocessor Supervisory Circuit with 2 clock input pin

NO.EA-172-111103

OUTLINE

The R5109G Series are CMOS-based microprocessor supervisory circuit, or high accuracy and ultra low supply current voltage detector with built-in delay circuit and watchdog timer. When the supply voltage is down across the threshold, or the watchdog timer does not detect the system clock from the microprocessor, the reset output is generated.

The voltage detector circuit is used for the system reset, etc. The detector threshold is fixed internally, and the accuracy is ±1.0%. The released delay time (Power-on Reset Delay) circuit is built-in, and output delay time is adjustable with an external capacitor, and the accuracy is ±16%*. When the supply voltage becomes the released voltage, the reset state will be maintained during the delay time. The output type of the reset is selectable, Nch open-drain, or CMOS.

The time out period of the watchdog timer can be also set with an external capacitor, and the accuracy is ±33%*.

The function to stop supervising clock by the watchdog timer (INH function) and the function to supervise two different clocks are built in this IC.

There are another 4 products by the difference of packages and the function of voltage detector and watchdog timer. The package of R5109G is SSOP-8G.

FEATURES

- Supply Current ..... Typ. 11.5μA
- Operating Voltage Range ..... 0.9V to 6.0V

< Voltage Detector Part >

- Detector Threshold Range ..... 1.5V to 5.5V (0.1V steps)
- Detector Threshold Accuracy ..... ±1.0%
- Power-on Reset Delay Time accuracy ..... ±16%* (–40°C ≤ Topt ≤ 105°C)
- Power-on reset delay time of the voltage detector ..... Typ. 370ms with an external capacitor : 0.1μF

< Watchdog Timer Part >

- Built-in a watchdog timer's time out period accuracy ..... ±33%* (–40°C ≤ Topt ≤ 105°C)
- Timeout period for watchdog timer ..... Typ. 310ms with an external capacitor : 0.1μF
- Reset timer for watchdog timer ..... Typ. 34ms with an external capacitor : 0.1μF
- With Inhibit pin (INH) ..... Able to stop watchdog timer
- Dual clock input ..... Able to supervise two microprocessors
- Package SSOP-8G

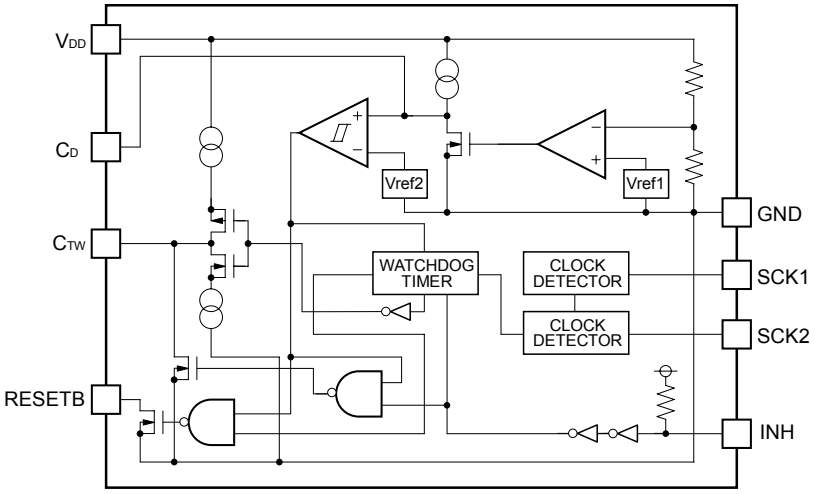
*) Accuracy to center value of (Min.+Max.)/2

APPLICATIONS

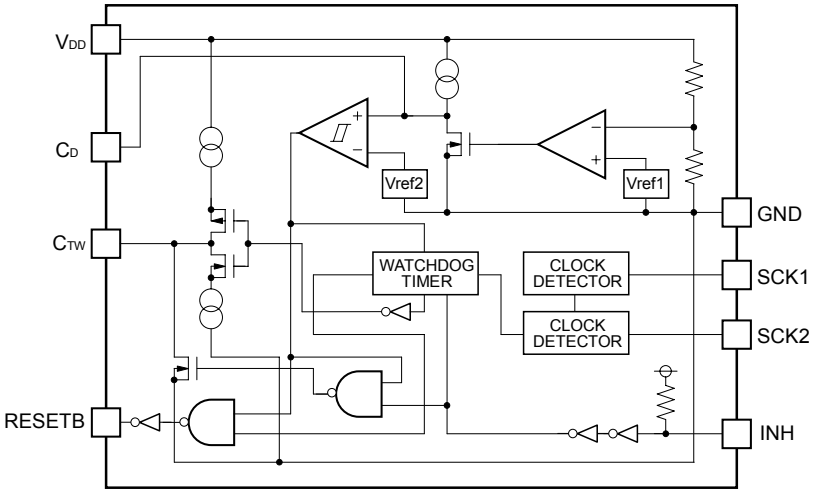
- Supervisory circuit for equipment with using microprocessors.

BLOCK DIAGRAMS

Nch Open Drain Output (R5109Gxx1A)



CMOS Output (R5109Gxx1C)



SELECTION GUIDE

The detector threshold, the output type and the taping type for the ICs can be selected at the users' request. The selection can be made with designating the part number as shown below;

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5109Gxx1∗-TR-FE	SSOP-8G	3,000 pcs	Yes	Yes

xx: The detector threshold can be designated in the range from 1.5V(15) to 5.5V(55) in 0.1V steps.

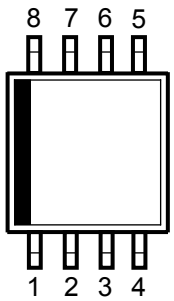
∗ : Designation of Output Type
(A) Nch Open Drain
(C) CMOS

SERIES SELECTION

	R5105N	R5106N	R5107G	R5108G	R5109G
Package	SOT-23-6		SSOP-8G		
With INH pin (Inhibit)	No	Yes			
2 clock input	No				Yes
With MR pin (Manual Reset)	No		Yes	No	
With SENSE pin	No			Yes	No
Remarks		C_D pin and C_{TW} pin are combined uses.		Operating Voltage Range 1.5V to 6.0V	Supply Current 11.5μA

PIN CONFIGURATION

● **SSOP-8G**



PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	RESETB	Output Pin for Reset signal of Watchdog timer and Voltage Detector. (Output "L" at detecting Detector Threshold and Watchdog Timer Reset.)
2	INH	Inhibit Pin ("L": Inhibit the watchdog timer)
3	C_D	External Capacitor Pin for Setting Delay Time of Voltage Detector
4	GND	Ground Pin
5	SCK1	Clock Input Pin 1 from Microprocessor
6	SCK2	Clock Input Pin 2 from Microprocessor
7	C_{TW}	External Capacitor Pin for Setting Reset and Watchdog Timeout Periods
8	V_{DD}	Power supply Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item		Rating	Unit
V_{DD}	Supply Voltage		−0.3 to 7.0	V
V_{CD}	Output Voltage	Voltage of C_D Pin	−0.3 to V_{DD} + 0.3	V
V_{CTW}		Voltage of C_{TW} Pin	−0.3 to V_{DD} + 0.3	V
V_{RESETB}		Voltage of RESETB Pin	−0.3 to 7.0	V
V_{SCK}	Input Voltage	Voltage of SCK1, SCK2 Pin	−0.3 to 7.0	V
V_{INH}		Voltage of INH Pin	−0.3 to 7.0	V
I_{RESETB}	Output Current	Current of RESETB Pin	20	mA
P_D	Power Dissipation (SSOP-8G)*		380	mW
Topt	Operating Temperature Range		−40 to 105	°C
Tstg	Storage Temperature Range		−55 to 125	°C

∗) For Power Dissipation, please refer to PACKAGE INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

V_{DD}=6.0V, C_{TW}=0.1μF, C_D=0.1μF, In case of Nch Open Drain Output type, the output pin is pulled up with a resistance of 100kΩ (R5109Gxx1A), unless otherwise noted.

The specification in ☐ is checked and guaranteed by design engineering at −40°C ≤ Topt ≤ 105°C.

• R5109Gxx1A/C

Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage		0.9		6.0	V
I_{SS}	Supply Current	V_{DD}= -V_{DET}+0.5V, Clock pulse input		11.5	15.5	μA

• VD Part

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
-V_{DET}	Detector Threshold	Topt=25°C		×0.990		×1.010	V
		−40°C ≤ Topt ≤ 105°C		×0.972		×1.015	
V_{HYS}	Detector Threshold Hysteresis			-V_{DET} ×0.03	-V_{DET} ×0.05	-V_{DET} ×0.07	V
Δ-V_{DET}/ ΔTopt	Detector Threshold Temperature Coefficient	−40°C ≤ Topt ≤ 105°C			±100		ppm/°C
t_{PLH}	Output Delay Time	C_D=0.1μF *1		340	370	467	ms
I_{RESETB}	Output Current (RESETB Output pin)	Nch	V_{DD}=1.2V V_{DS}=0.1V	0.38	0.8		mA
		Pch *2	V_{DD}=6.0V V_{DS}=0.5V	0.65	0.9		mA

• WDT Part

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
t_{WD}	Watchdog Timeout period	C_{TW}=0.1μF *1	230	310	450	ms
t_{WR}	Reset Hold Time of WDT	C_{TW}=0.1μF *1	29	34	48	ms
V_{SCKH}	SCK Input "H"	SCK1, SCK2	V_{DD}×0.8		6.0	V
V_{SCKL}	SCK Input "L"	SCK1, SCK2	0		V_{DD}×0.2	V
V_{INHH}	INH Input "H"		1.0		6.0	V
V_{INHL}	INH Input "L"		0		0.35	V
R_{INH}	INH pull-up Resistance		60	110	164	kΩ
t_{SCKW}	SCK Input Pulse Width	V_{SCKL}=V_{DD}×0.2 V_{SCKH}=V_{DD}×0.8	500			ns

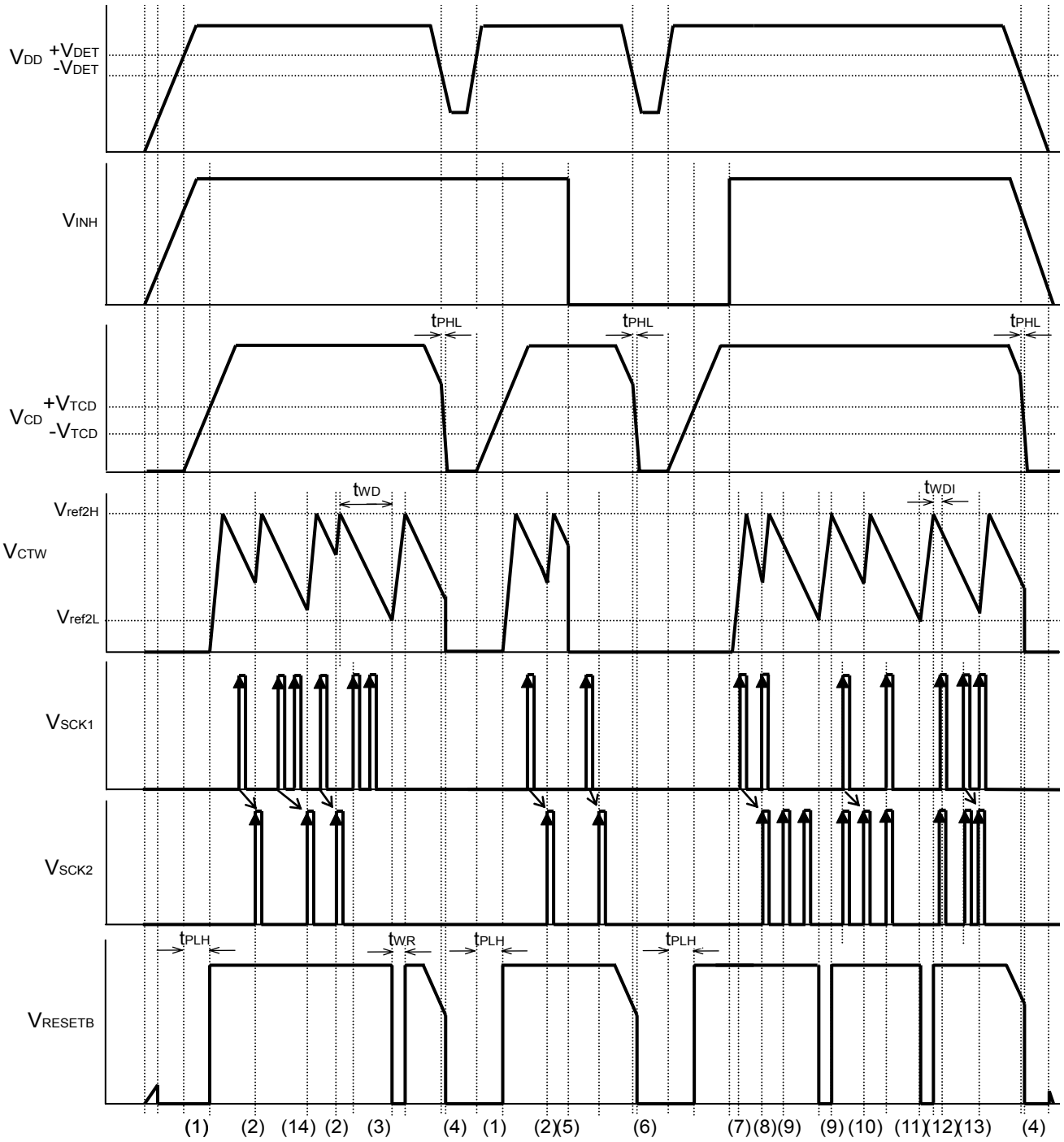
All of unit are tested and specified under load conditions such that Topt=25°C except for Detector Threshold Temperature Coefficient.

∗1) The specification does not contain the temperature characteristics of the external capacitor.
∗2) In case of CMOS type (R5109Gxx1C)

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge.
And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

TIMING CHART



∗) V_{TCD} : Threshold voltage of C_D pin when a power-on reset pulse inverting.

∗) V_{ref2H} : C_{TW} pin voltage at the end of WDT timeout period.

∗) V_{ref2L} : C_{TW} pin voltage at the begin of WDT timeout period.

OPERATION

(1) When the power supply, V_{DD} pin voltage becomes more than the released voltage ($+V_{DET}$), after the released delay time (or the power on reset time t_{PLH}), the output of RESETB becomes "H" level.

(2) After the SCK1 pulse is input, when the SCK2 pulse is input, the watchdog timer is cleared, and C_{TW} pin mode changes from the discharge mode to the charge mode. When the C_{TW} pin voltage becomes higher than V_{ref2H}, the mode will change into the discharge mode, and next watchdog time count starts.

(3) After the SCK1 pulse is input, unless the SCK2 pulse is input, WDT will not be cleared, and during the charging period of C_{TW} pin, RESETB="L".

(4) When the V_{DD} pin becomes lower than the detector threshold voltage ($-V_{DET}$), RESETB outputs "L" after the t_{PHL}.

(5) If "L" signal is input to the INH pin, the RESETB outputs "H", regardless the SCK clock state.

(6) During the "L" period of INH pin, the voltage detector monitors the supply voltage.

(7) When the signal to the INH pin is set from "L" to "H", the watchdog starts supervising the system clock, or charge cycle to the C_{TW} pin starts, the capacitor connected to the C_{TW} pin is charged with the current of setting Reset time of WDT.

(8) After the SCK1 pulse is input, when the SCK2 is input, the WDT will be cleared.

(9) Without the input of SCK1 pulse input, even if the SCK2 pulse is input, the WDT will not be cleared.

(10) After the SCK1 pulse is input, when the SCK2 is input, the WDT will be cleared.

(11) If SCK1 pulse and SCK2 pulse are input at the same time, the WDT will not be cleared.

(12) After from the discharge of the external capacitor even if the clock pulse is input during the time period "t_{WDI}", the clock pulse is ignored.

(13) After the SCK1 pulse is input, when the SCK2 is input, the WDT will be cleared.

(14) The WDT supervises SCK1 pulse and SCK2 pulse by turns, therefore, for example, if only SCK1 pulse is input twice or more without SCK2 pulse, the second or later consecutive SCK1 pulse will be ignored. After the SCK1 pulse is input, and when the SCK2 pulse is input, the WDT will be cleared. In the same way, if only SCK2 pulse is input twice or more without SCK1 pulse, the second or later consecutive SCK2 pulse will be ignored.

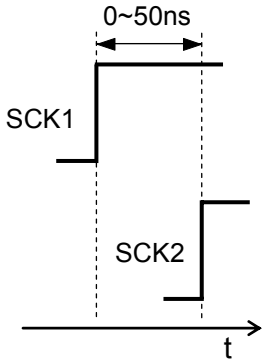
Too close timing of SCK1 pulse input and SCK2 pulse input means the rising edge interval time range from 0ns to 50ns. (Guaranteed by design, not mass production tested.)

Even if the SCK1 and SCK2 are input at almost the same time as above, the WDT will still try to supervise these two clock by turns.

Therefore, after the SCK1 pulse is input, if SCK1 pulse and SCK2 pulse are input at almost the same time, the WDT will be cleared. (as the status (8))

Likewise, after the SCK1 pulse and SCK2 pulse are input at almost the same time, when the SCK2 pulse is input, the WDT will be cleared. (as the status (10))

If the almost same timing input of SCK1 and SCK2 continues twice, the WDT will be cleared. (as the status (13))



Example timing of too close input pulses

(This pattern will be recognized the clock timing is same by the WDT)

- **Watchdog Timeout period/Reset hold time**

The watchdog timeout period and reset hold time can be set with an external capacitor to C_{TW} pin.

The next equations describe the relation between the watchdog timeout period and the external capacitor value, or the reset hold time and the external capacitor value.

t_{WD} (s) = 3.1 × 10^6 × C (F)

t_{WR} (s) = t_{WD}/9

The watchdog timer (WDT) timeout period is determined with the discharge time of the external capacitor. During the watchdog timeout period, if the clock pulse from the system is detected, WDT is cleared and the capacitor is charged. When the charge of the capacitor completes, another watchdog timeout period starts again. During the watchdog timeout period, if the clock pulse from the system is not detected, during the next reset hold time RESETB pin outputs "L".

During the reset time, (while charging the external capacitor) and after starting the watchdog timeout period, (just after from the discharge of the external capacitor) even if the clock pulse is input during the time period "t_{WDI}", the clock pulse is ignored.

t_{WDI} (s) = t_{WD}/10

- **Released Delay Time (Power-on Reset delay time)**

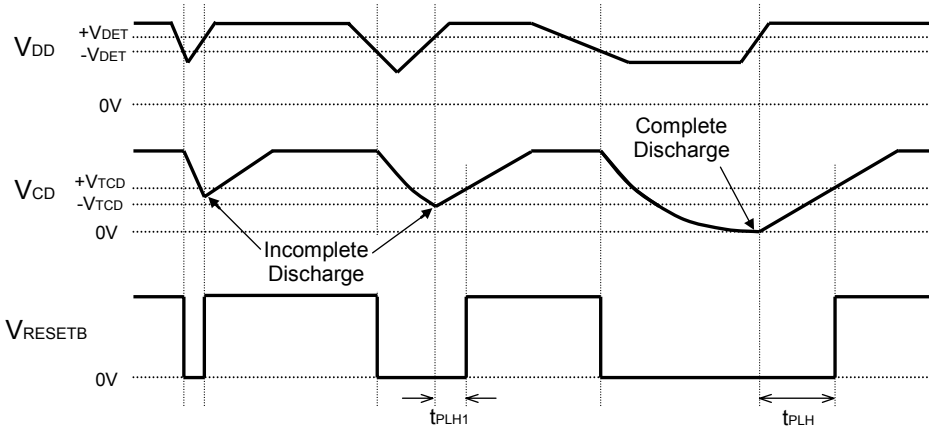
The released delay time can be set with an external capacitor connected to the C_D pin. The next equation describes the relation between the capacitance value and the released delay time (t_{PLH}).

t_{PLH} (s) =3.7 × 10^6 × C (F)

The capacitor connected to C_D pin determines t_{WD}, t_{WR}, and t_{PLH}.

When the V_{DD} voltage becomes equal or less than ($-V_{DET}$), discharge of the capacitor connected to the C_D pin starts. Therefore, if the discharge is not enough and V_{DD} voltage returns to ($+V_{DET}$) or more, thereafter the delay time will be shorter than t_{PLH} which is expected.

Power on Reset Operation against the input glitch (t_{PLH1} < t_{PLH})



- **Minimum Operating Voltage**

We specified the minimum operating voltage as the minimum input voltage in which the condition of RESETB pin being 0.1V or lower than 0.1V. (Herein, pull-up resistance is set as 100kΩ in the case of the Nch open-drain output type.)

- **Inhibit (INH) Function**

If INH pin is set at "L", the watchdog timer stops monitoring the clock, and the RESETB output will be dominant by the voltage detector's operation. Therefore, if the supply voltage is set at more than the detector threshold level, RESETB outputs "H" regardless the clock pulse. INH pin is pulled up with a resistor (Typ.110kΩ) internally.

- **RESETB Output**

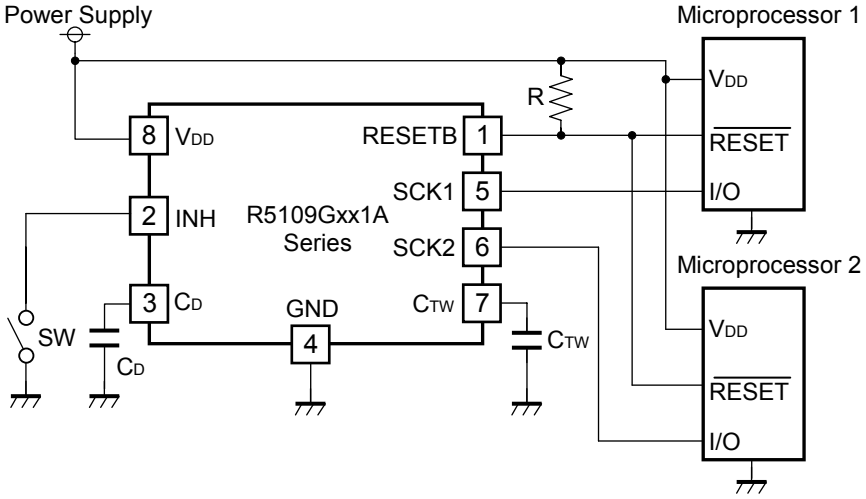
RESETB pin's output type is selectable either the Nch open-drain output or CMOS output. If the Nch open-drain type output is selected, the RESETB pin is pulled up with an external resistor to an appropriate voltage source.

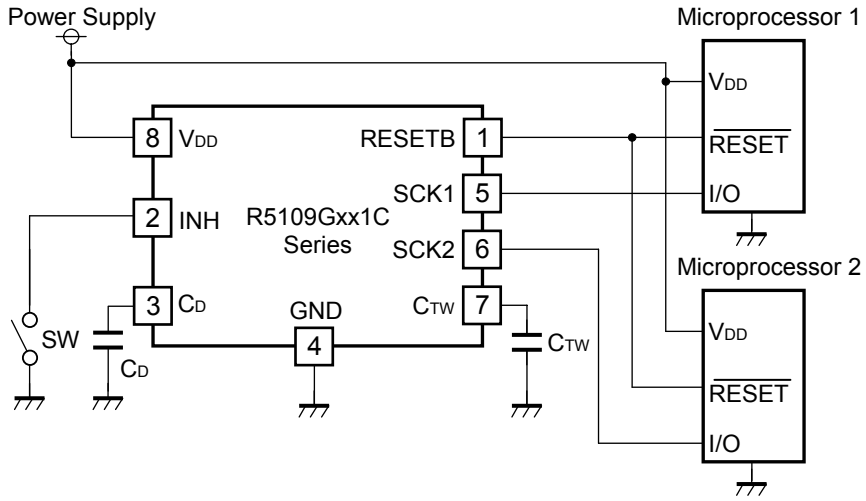
- **Clock Pulse Input**

Built-in watchdog timer is cleared with the SCK clock pulse within the watchdog timeout period.

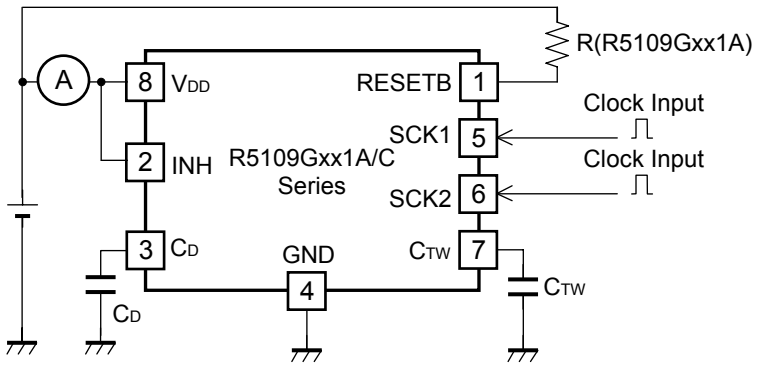
After the SCK1 clock pulse is input, when the SCK2 pulse is input, the watchdog timer will be cleared. If the system requires only one clock supervise, SCK1 pin and SCK2 pin must connect each other. In this case, the watchdog timer is cleared with every other clock pulse. Depending on the timing of these two clock pulses, SCK1 pulse and SCK2 pulse are recognized at almost the same time by the watchdog timer, during the watchdog timeout period, after the SCK1 clock pulse, two or more SCK2 clock pulses are desirable to put into.

TYPICAL APPLICATIONS





TEST CIRCUIT

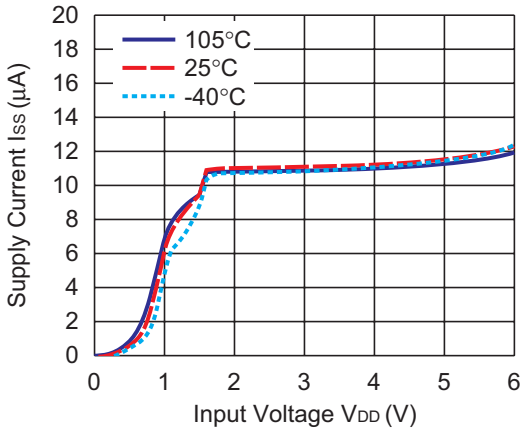


Supply Current Test Circuit

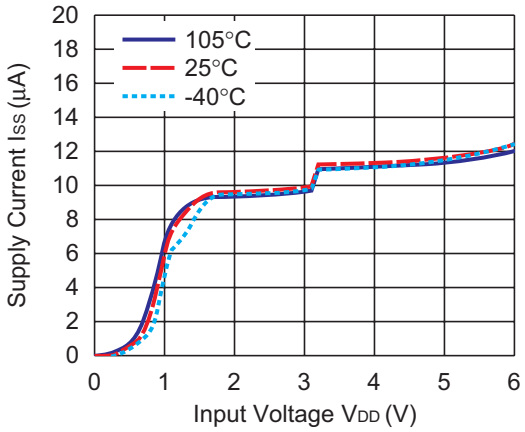
TYPICAL CHARACTERISTICS

1) Supply Current vs. Input Voltage

R510xx151x

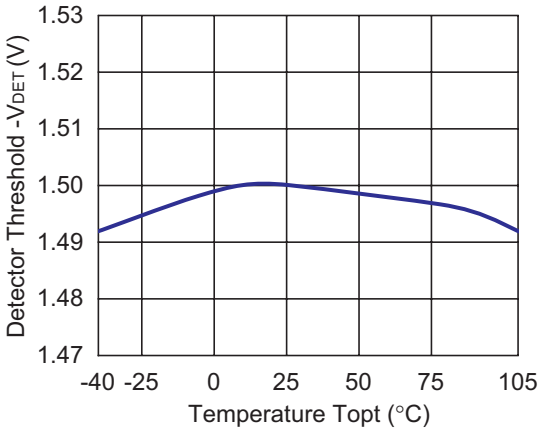


R510xx301x

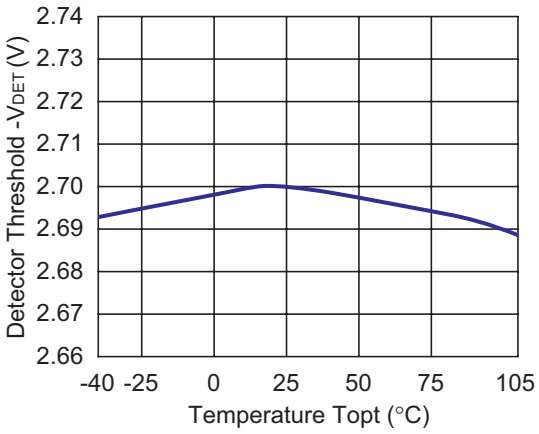


2) Detector Threshold vs. Temperature

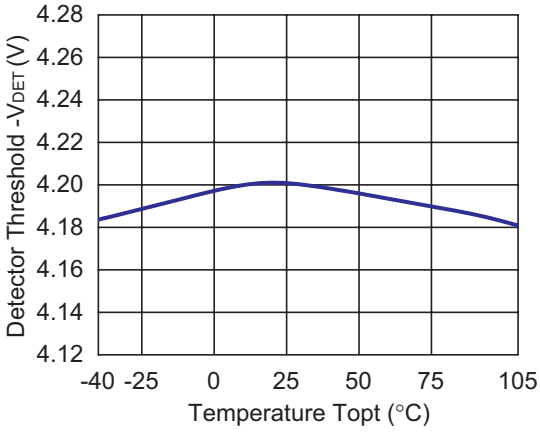
R510xx151x



R510xx271x

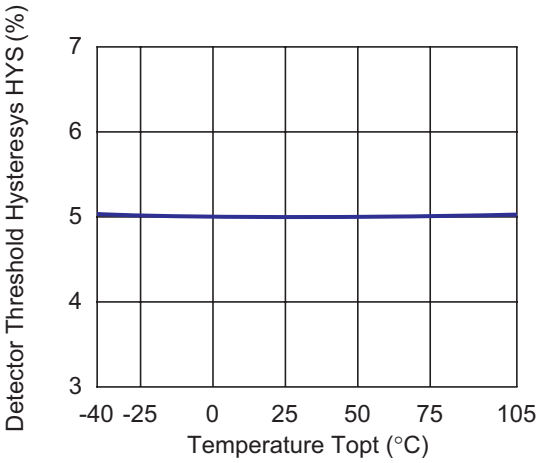


R510xx421x



3) Detector Threshold Hysteresis vs. Temperature

R510xx151x



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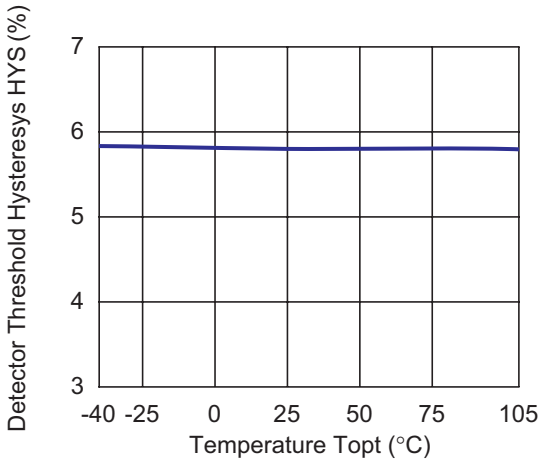

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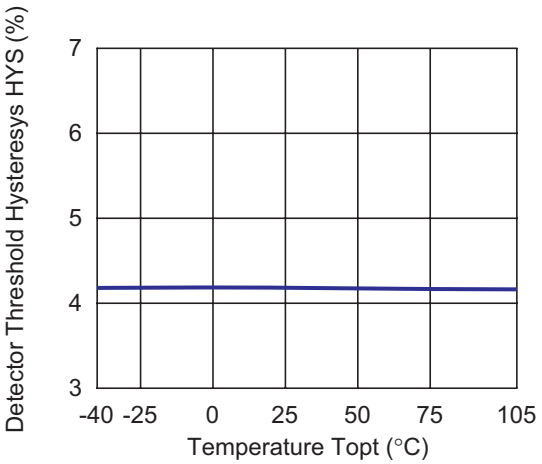
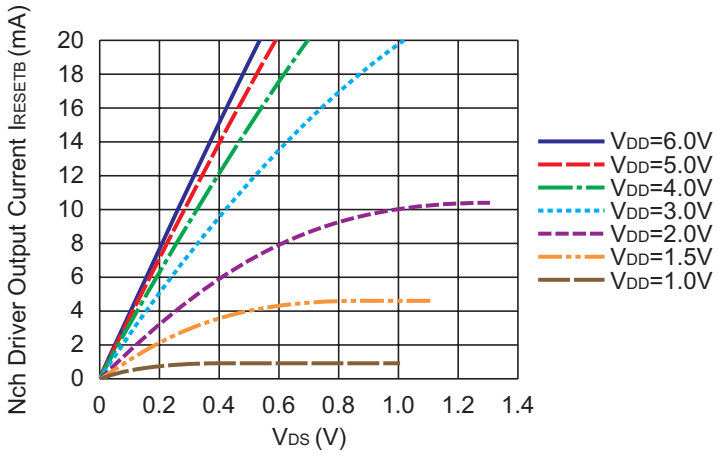


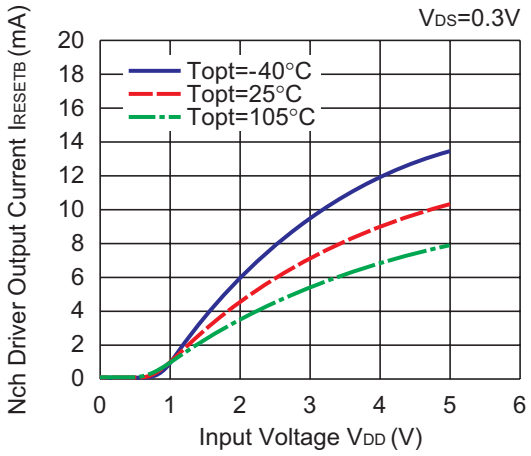
4) Nch Driver Output Current vs. V_{DS}

R510xx



5) Nch Driver Output Current vs. Input Voltage

R510xx



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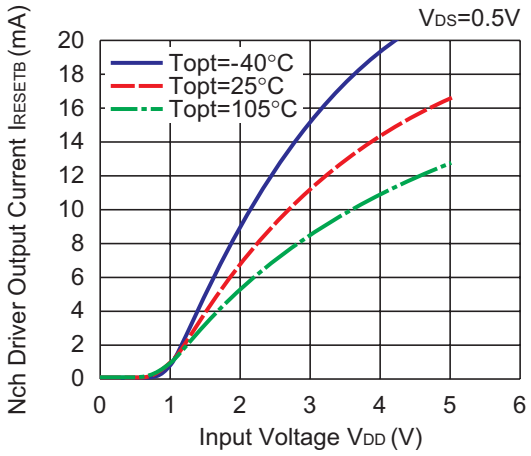
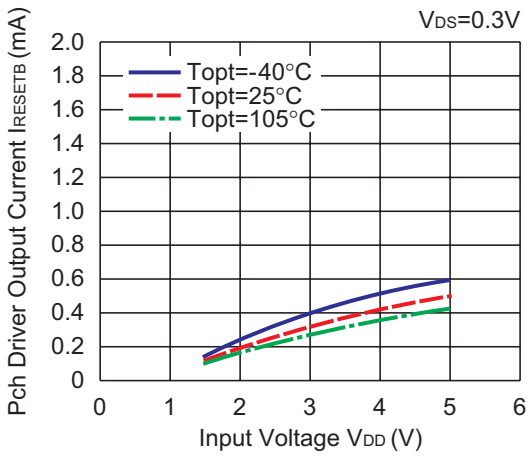


6) Pch Driver Output Current vs. Input Voltage

R510xx



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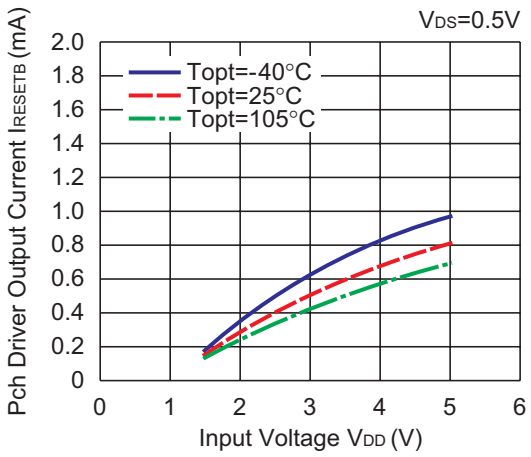

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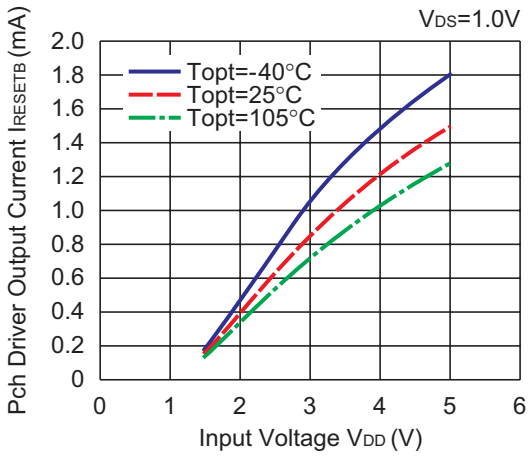

7) Released Delay Time vs. Input Voltage

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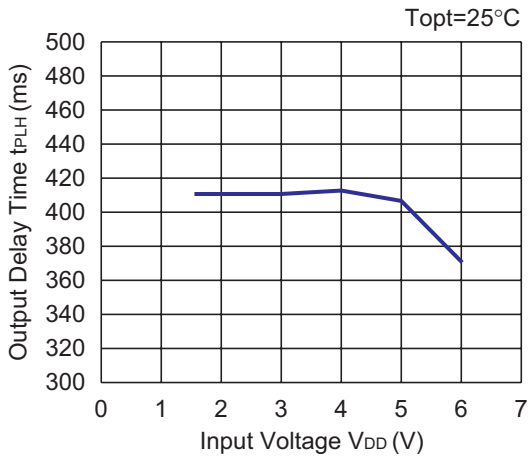
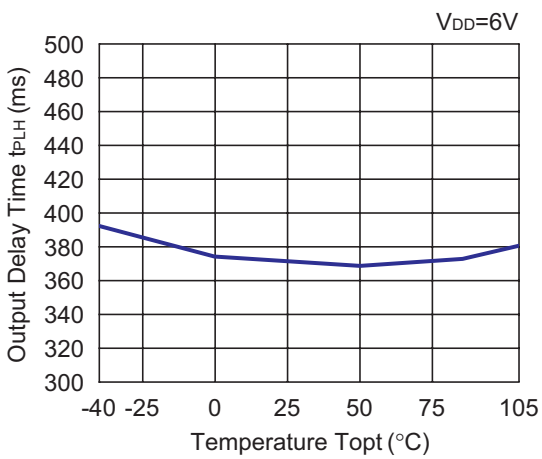


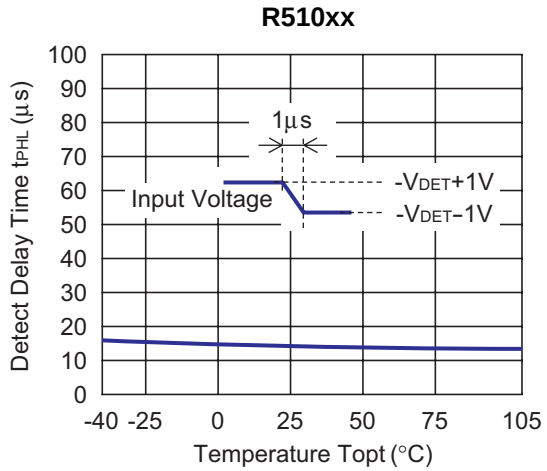
8) Released Delay Time vs. Temperature

R510xx



9) Detector Output Delay Time vs. Temperature

R510xx



10) WDT Reset Timer vs. Temperature

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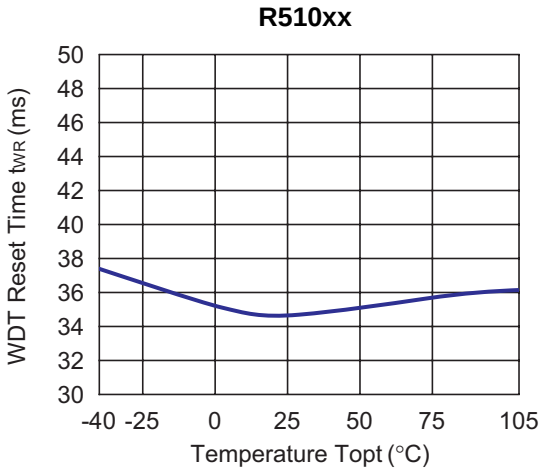
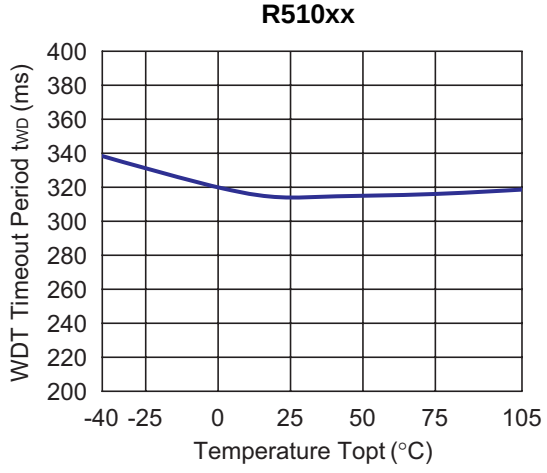


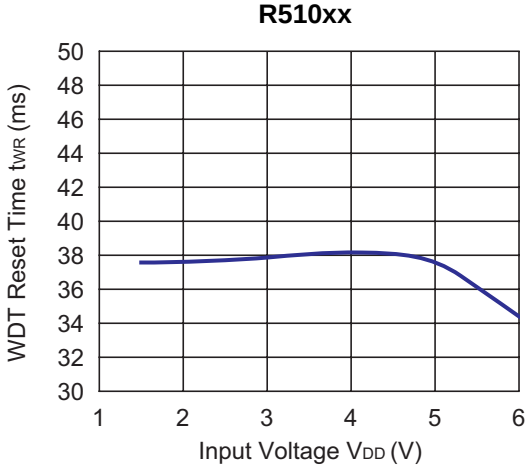
11) WDT Timeout Period vs. Temperature

R510xx

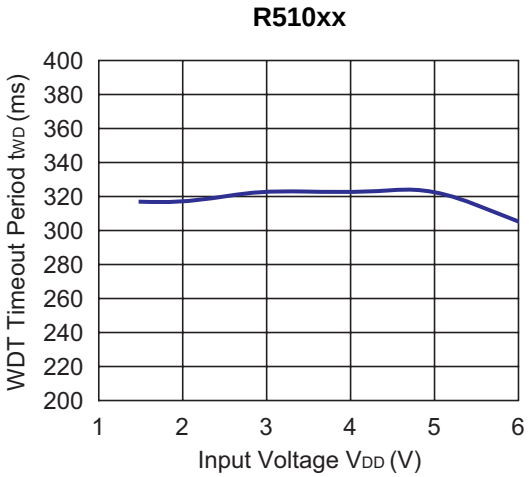


12) WDT Reset Timer vs. Input Voltage

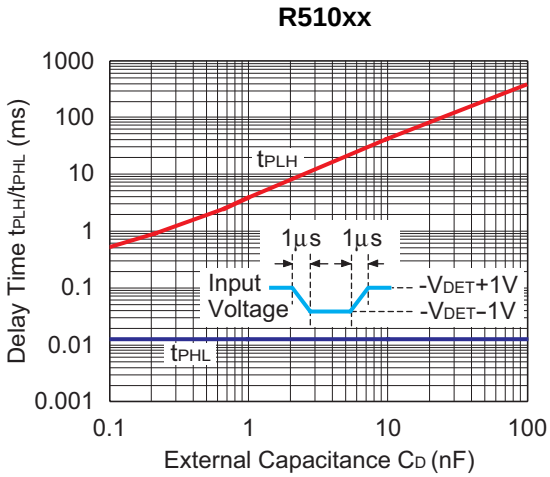
R510xx



13) WDT Timeout Period vs. Input Voltage



14) Output Delay Time vs. External Capacitance



TECHNICAL NOTES

When R510xxxx1A (Nch Open Drain Output Type) is used in Figure A or Figure B, if impedance of Voltage Supply pin, V_{DD} and V_{DD} of this IC is large, detector threshold level would shift by voltage dropdown caused by the consumption current of the IC itself. Released voltage may also shift and delay time for start-up might be generated by this usage.

When R510xxxx1C (CMOS Output Type) is used in Figure A or Figure B, Output level could be unstable by cross conduction current which is generated at detector threshold level or at released voltage level, therefore, do not use this IC with the connection in Figure A or Figure B.

The connection in Figure C may cause the oscillation in both R510xxxx1A (Nch Open Drain Output) and R510xxxx1C (CMOS Output), therefore do not use R510xx Series with the connection in Figure C.

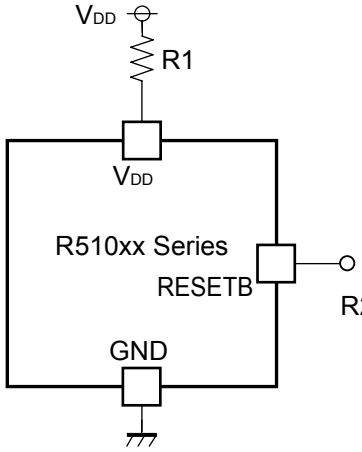


Figure A

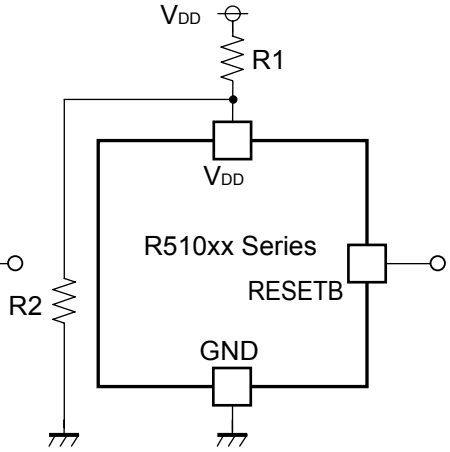


Figure B

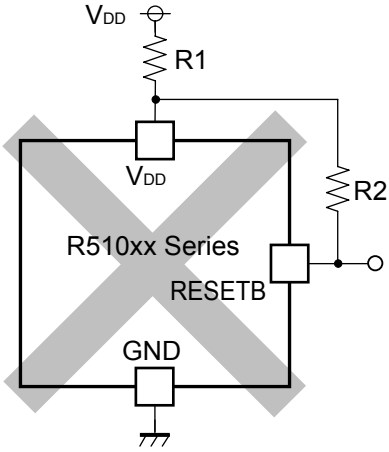


Figure C

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