REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-09-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 4K X 8-BIT UVEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90658
A	67268	

SHEET 1 OF 12

1

DESC FORM 193
JUL 91

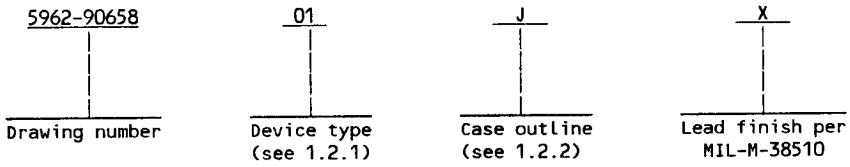
5962-E591-92

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	57C43C-70	4K x 8-bit UVEPROM	70 ns
02	57C43C-55	4K x 8-bit UVEPROM	55 ns
03	57C43C-45	4K x 8-bit UVEPROM	45 ns
04	57C43C-35	4K x 8-bit UVEPROM	35 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line 1/
K	GDFP2-F24 or CDFP3-F24	24	Flat pack 1/
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line 1/
3	CQCC1-N28	28	Square leadless chip carrier 1/

1.3 Absolute maximum ratings.

Voltage range on any pin with respect to ground . . . . . -0.6 V dc to +7.0 V dc
V_{pp} range with respect to ground . . . . . -0.6 V dc to +14.0 V dc
Storage temperature range . . . . . -65°C to +150°C
Maximum power dissipation (P_D) . . . . . 1 W
Lead temperature (soldering, 10 seconds) . . . . . +300°C
Thermal resistance, junction-to-case (θ_{JC}) . . . . . See MIL-STD-1835
Junction temperature (T_J) 2/ . . . . . +150°C
Temperature (under bias) range . . . . . -55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) . . . . . +4.5 V dc to +5.5 V dc
Ground voltage (GND) . . . . . 0 V dc
Input high voltage (V_{IH}) . . . . . 2.0 V dc minimum
Input low voltage (V_{IL}) . . . . . 0.8 V dc maximum
Case operating temperature range (T_C) . . . . . -55°C to +125°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified		Group A subgroups	Device types	Limits		Units
						Min	Max	
Input load current	I_{LI}	V_{IN} = 5.5 V and GND		1,2,3	All	-10	10	µA
Input leakage current	I_{IX}	V_{IN} = V_{CC} and GND		1,2,3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{OUT} = 5.5 V and GND		1,2,3	All	-10	10	µA
V_{CC} active current (CMOS)	I_{CC1}	CMOS inputs: 0 ± 0.3 V or V_{cc} ±0.3 V 1/		1,2,3	All		35	mA
V_{CC} active current (TTL)	I_{CC2}	TTL inputs: $V_{IL} \le 0.8$ V, $V_{IH} \ge 2.0$ V 1/		1,2,3	All		50	mA
Input high level voltage	V_{IH}			1,2,3	All	2.0	V_{CC} +0.3	V
Input low level voltage	V_{IL}			1,2,3	All	-0.1	0.8	V
Ouput high voltage	V_{OH}	I_{OH} = -4 mA		1,2,3	All	2.4		V
Output low voltage	V_{OL}	I_{OL} = 16 mA		1,2,3	All		0.4	V
Functional tests		See 4.3.1d		7,8A,8B	All			
Input capacitance	C_{IN}	V_{IN} = 0 V 2/	T_A = +25°C f = 1 MHz	4	All		6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V 2/	T_A = +25°C f = 1 MHz	4	All		12	pF
Address to output delay	t_{ACC}	See figures 3 and 4		9,10,11	01		70	ns
					02		55	
					03		45	
					04		35	
$\overline{CS1}/V_{PP}$ to output delay	t_{CS}			9,10,11	01-03		25	ns
					04		20	
Output disable to output float	t_{DF}	3/ See figures 3 and 4		9,10,11	All		25	ns
Address to output hold	t_{OH}	See figures 3 and 4		9,10,11	All	0		ns

1/ Add 3 mA/MHz for ac power component.
2/ Tested initially and after any design or process changes that affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
3/ May not be tested, but shall be guaranteed to the limits specified in table I.

Device types	All	
Case outlines	J, K, and L	3
Terminal number	Terminal symbol	
1	A_7	NC
2	A_6	A_7
3	A_5	A_6
4	A_4	A_5
5	A_3	A_4
6	A_2	A_3
7	A_1	A_2
8	A_0	A_1
9	O_0	A_0
10	O_1	NC
11	O_2	O_0
12	GND	O_1
13	O_3	O_2
14	O_4	GND
15	O_5	NC
16	O_6	O_3
17	O_7	O_4
18	CS2	O_5
19	A_{11}	O_6
20	$\overline{CS1}/V_{PP}$	O_7
21	A_{10}	NC
22	A_9	CS2
23	A_8	A_{11}
24	V_{CC}	$\overline{CS1}/V_{PP}$
25	---	A_{10}
26	---	A_9
27	---	A_8
28	---	V_{CC}

FIGURE 1. Terminal connections.

Mode	V_{CC}	$\overline{CS1}/V_{PP}$	CS2	O_0-O_7
Read	5.0 V ±10%	V_{IL}	V_{IH}	D_{OUT}
Output disable	5.0 V ±10%	V_{IH}	X 1/	High Z
Output disable	5.0 V ±10%	X 1/	V_{IL}	High Z
Program	V_{CC}	V_{PP}	X 1/	D_{IN}
Program verify	V_{CC}	V_{IL}	V_{IH}	D_{OUT}

1/ X can be V_{IL} or V_{IH}.

FIGURE 2. Truth table.

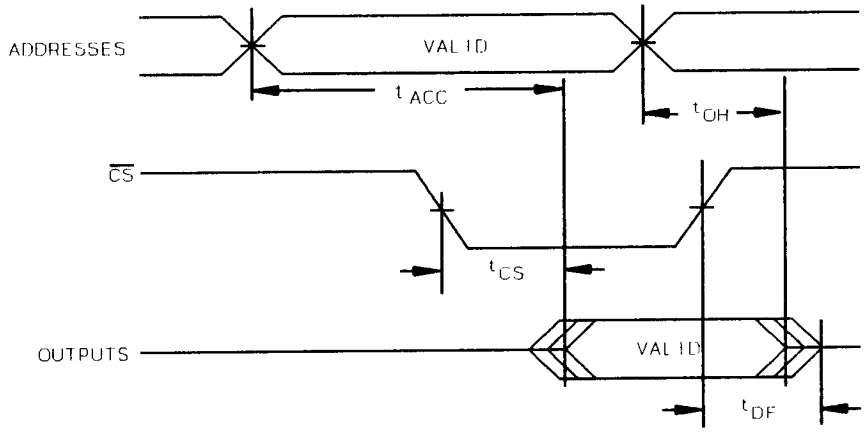
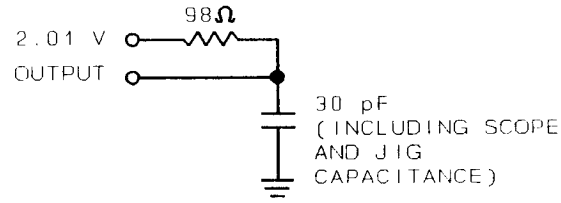


FIGURE 3. AC read timing diagram.



Test conditions (ac):

Input pulse levels: GND to 3.0 V
Input rise and fall times: ≤ 5 ns
Input timing reference levels: 1.5 V
Output reference levels: 1.5 V

FIGURE 4. Test load circuit.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.6.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed to specified program or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC of change of product (see 6.3 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

a. All devices selected for testing shall be programmed in accordance with 3.2.3.2 herein.

b. Verify pattern (see 3.6.3).

c. Erase (see 3.6.1).

d. Verify pattern erasure (see 3.6.3).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters for for unprogrammed devices (method 5004)	1*,2,3,7*,8A,8B, 9,10,11
Final electrical test parameters for programmed devices (method 5004)	1,2,3,7*,8A,8B, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7***, 8***,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1e.
*** See 4.3.1d.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method. 4/

(1) At +25°C, program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worst case speed pattern.
(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C.
(3) At +25°C, perform a margin test using V_m = +5.8 V to loose timing (i.e., t_{ACC} = 1 µs).
(4) Perform dynamic burn-in accordance with 4.2a.
(5) At +25°C, perform a margin test using V_m = +5.8 V.
(6) Perform electrical test in accordance with 4.2b.
(7) Erase in accordance with 3.6.1. Devices may be submitted to quality conformance inspection.
(8) Verify erasure in accordance with 3.6.3.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4/ Steps 1 through 3 may be performed at the wafer level.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.

d. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6021.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-ECS.