PMC-Sierra,Inc.

PM4344 TQUAD

Quad T1 Framer

FEATURES

- Monolithic single-chip device that integrates four full-featured T1 framers and transmitters for terminating duplex DS1 signals.
- Supports SF, ESF, T1DM (DDS), and SLC®96 format DS1 signals.
- Supports unframed mode. Supports B8ZS or AMI line codes.
- Supports transfer of PCM and signalling data to/from 1.544 Mbit/s, 2.048 Mbit/s, 12.352 Mbit/s, or 16.384 Mbit/s backplane buses.
- Supports *n* x DS0 backplane interface for fractional T1.
- Provides robbed-bit signalling extraction/insertion, programmable idle and digital milliwatt code substitution, and two superframes of signalling debounce on a per-channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signalling conditioning on all/selected channels.
- Provides ESF bit-oriented code detection/generation, and an HDLC interface for terminating/generating the ESF data link.
- Software and functionally compatible with the PM4341A T1XC Single T1 Transceiver. Pin-compatible with the PM6344 EQUAD Quad E1 Framer.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 5 V CMOS technology.
- Available in a rectangular 128-pin PQFP (14 by 20 mm) package.

RECEIVE SECTION

- Recovers clock and data using a digital PLL for high jitter tolerance.
- Accepts/provides dual- or single-rail digital PCM inputs/outputs. Accepts gapped data streams to support higher rate demultiplexing.
- Provides Loss Of Signal (LOS) detection, and red, yellow, and Alarm Indication Signal (AIS) alarm detection.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window.
- Provides programmable in-band loopback code detection.
- Supports line and path performance monitoring according to AT&T and ANSI specifications. Accumulators are provided for counting, ESF CRC-6 errors, Framing bit errors, Line Code Violations (LCVs), and Loss Of Frame (LOF) or change of frame alignment events.
- Extracts the data link in ESF, T1DM (DDS), or SLC®96 modes. Extracts selected channels.
- Provides a 2-frame elastic store buffer for jitter and wander attenuation.

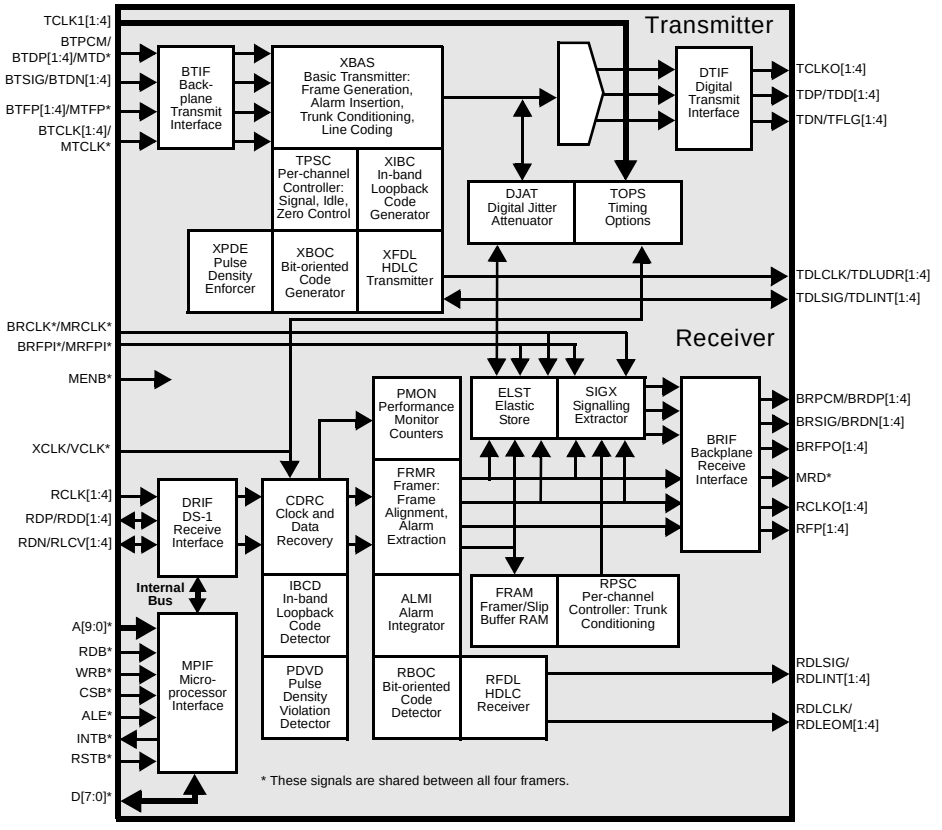
TRANSMIT SECTION

- Optionally accepts/provides dual-rail digital PCM inputs/outputs.
- Provides per-channel minimum ones density through Bell (bit 7), GTE, DDS, or “jammed bit 8" (56 Kbit/s) zero code suppression.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window.
- Allows insertion of framed or un-framed in-band loopback code sequences.
- Allows insertion of a data link in ESF, T1DM (DDS) or SLC®96 modes.
- Allows insertion of selected channels through a serial port.
- Supports transmission of the AIS or the yellow alarm signal in all formats.
- Provides a digital PLL for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and transmit rate conversion. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.

APPLICATIONS

- T1/T3 Multiplexers and Digital Private Branch Exchanges (PBXs)
- T1 Frame Relay Interfaces
- T1 ATM Interfaces
- Fractional T1 Interfaces
- Digital Access and Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSXs)
- Digital Loop Carriers (DLCs)
- T1 Channel Service Units (CSUs) and Data Service Units (DSUs)
- ISDN Primary Rate Interfaces (PRIs)
- SONET Add/Drop Multiplexers (ADMs)

BLOCK DIAGRAM



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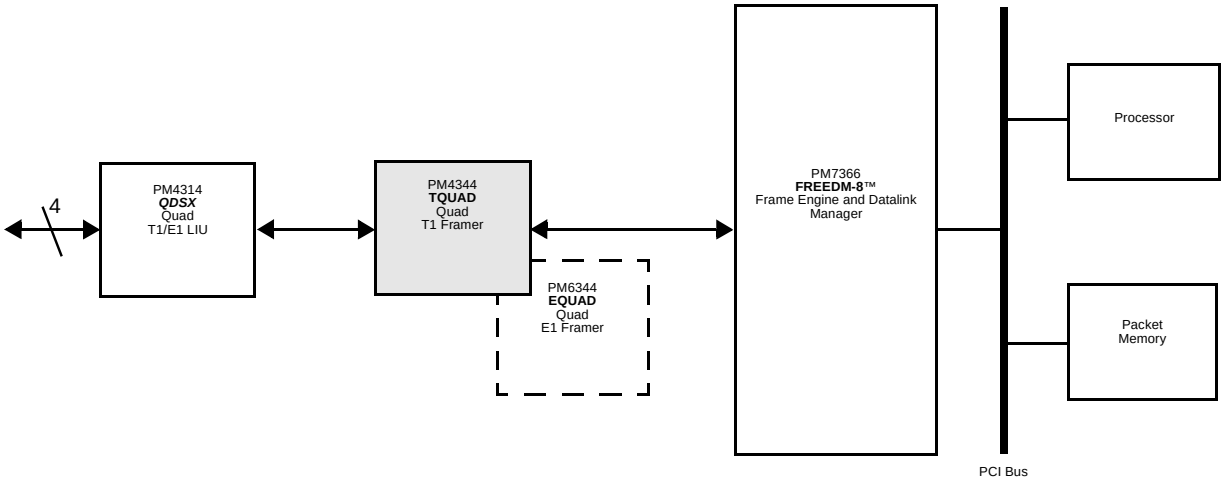
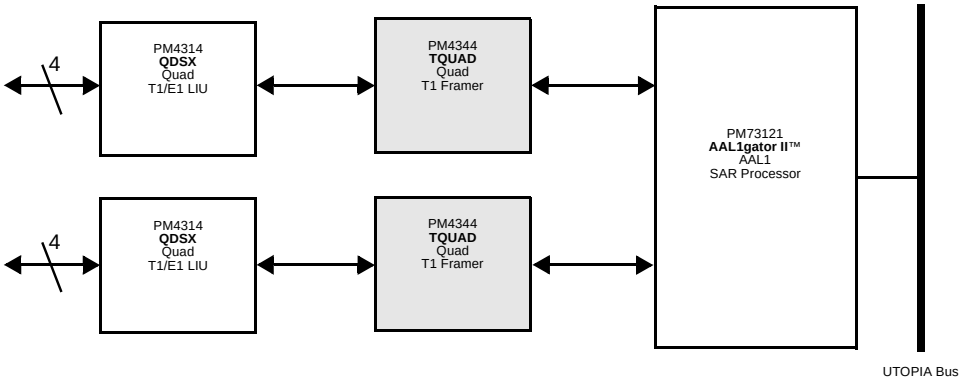
TYPICAL APPLICATIONS

FULLY CHANNELIZED HDLC APPLICATION



STRUCTURED/UNSTRUCTURED T1 AAL1 OCTAL PORT CARD



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