Quadruple filter DAC TDA1314T

FEATURES

- High dynamic range to enable digital DSP (Digital Signal Processor) volume control
- 18 bits data input format for each of the four channels
- Four times bit-serial oversampling filter
- 1st-order $4f_{as}$ (audio sampling frequency) noise shaper
- Four very low noise DACs
- Only 1st-order analog post filtering required
- Smooth power-on of the DAC output currents
- Because of the automatic digital PLL divider range setting the master clock is selectable in a wide $4f_{as}$ integer range
- Insensitive to jitter on the I^2S-bus signals with respect to the DAC total harmonic distortion deterioration.

APPLICATIONS

- Stand-alone quadruple low noise DAC
- Car radio DAC in conjunction with DSP.

GENERAL DESCRIPTION

The TDA1314T is a quadruple very low noise high dynamic range DAC which is intended for use in motor cars and is controlled by the car radio DSP. Each channel incorporates an 8th-order IIR up-sampling filter from 1ASF to 4ASF followed by a 1st-order noise shaper and DAC. The DAC currents are converted to audio voltage signals using operational amplifiers (one per channel).

QUICK REFERENCE DATA

V_{ref} = 2.5 and 5 V; T_{amb} = 25 °C; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
$I_{O(DAC)}$	DAC output current (FS)	R_{ref} = 20.5 kΩ	±0.4	±0.5	±0.6	mA
$V_{O(DAC)}$	DAC output voltage, nominal DAC operational amplifier output voltage	$R_L \geq 5$ kΩ; R_{fb} = 3 kΩ	1.0	–	4.0	V
RES	DAC resolution	length of data input word	–	–	18	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; 0 dB signal level	–	–66	–56	dB
DR	dynamic range of DAC	f_i = 1 kHz; –60 dB signal level	92	96	–	dB
DS	digital silence	no signal; A-weighted	–	–110	–100	dB
P_{tot}	total power dissipation		–	85	–	mW
T_{amb}	operating ambient temperature		–40	+25	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1314T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

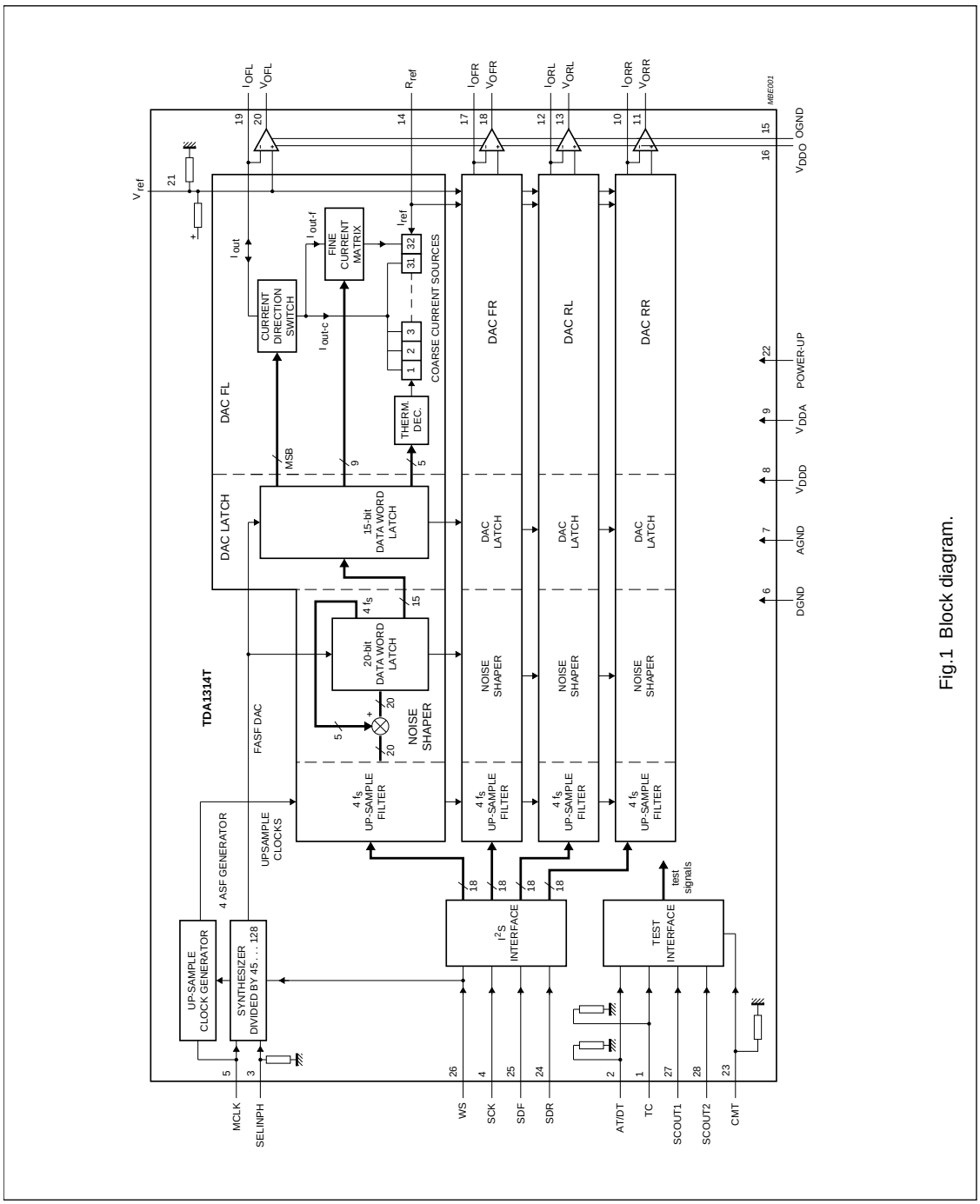


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TC	1	test control signal input (test/operational)
AT/DT	2	analog test/digital test select input
SELINPH	3	select in-phase $4f_{as}$ mode/scan input signal 1 in test mode
SCK	4	serial clock input; I^2S-bus
MCLK	5	master clock input; $f_i = N \times 4f_{as}$ ($45 \leq N \leq 128$)
DGND	6	digital ground
AGND	7	analog ground
V_{DDD}	8	digital supply voltage
V_{DDA}	9	analog supply voltage
I_{ORR}	10	DAC output current; rear right
V_{ORR}	11	DAC output voltage; rear right
I_{ORL}	12	DAC output current; rear left
V_{ORL}	13	DAC output voltage; rear left
R_{ref}	14	resistor reference input for DACs current
OGND	15	operational amplifier ground
V_{DDO}	16	operational amplifier supply
I_{OFR}	17	DAC output current; front right
V_{OFR}	18	DAC output voltage; front right
I_{OFL}	19	DAC output current; front left
V_{OFL}	20	DAC output voltage; front left
V_{ref}	21	reference voltage input ($\frac{1}{2}$ operational amplifier supply voltage)
POWER-UP	22	analog mute input for all DACs
CMT	23	current mirror input test signal
SDR	24	serial data input for rear DACs (I^2S-bus); scan input signal 2 in test mode
SDF	25	serial data input for front DACs (I^2S-bus)
WS	26	word select input (I^2S-bus)
SCOUT1	27	scan output signal 1 in test mode; $4f_{as}$ signal
SCOUT2	28	scan output signal 2 in test mode; PLL lock indicator

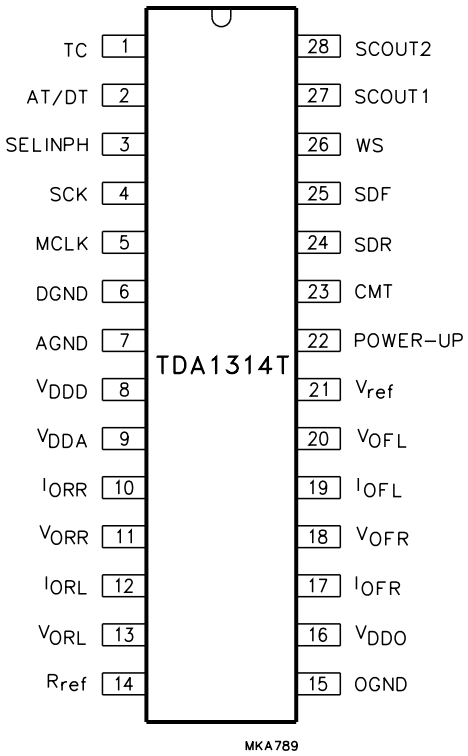


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

I²S-bus interface

The word select input (pin 26) is connected to the word select line of the I²S-bus interface. This interface has a standard I²S-bus specification as described in the Philips *"I²S-bus specification"* (ordering number 9398 332 10011). Figure 4 shows an excerpt of the Philips I²S-bus specification interface report with respect to the general timing and format of the I²S-bus. WS logic 0 means left channel word, logic 1 means right channel word.

The serial clock input (pin 4) must be in accordance with the I²S-bus specification, i.e. a continuous clock.

Serial data front (SDF, pin 25) and serial data rear (SDR, pin 24) are the I²S-bus serial data lines to be processed in the DACs for the loudspeakers of the car (see Fig.2, blocks DACFL and DACFR for the front loudspeakers and blocks DACRL and DACRR for the right loudspeakers). FL stands for Front Left, FR for Front Right, RL for Rear Left and RR for Rear Right. In order to utilize the capabilities of this IC fully, the data word length should be 18 bits. Signals derived from this block are 4×18-bit parallel data words which are applied to the $4f_s$ up-sample filters.

4ASF generator

SYNTHESIZER

SELINPH (pin 3) and WS (pin 26) are the data inputs for this block which generates the FASFDAC, this being the $4f_{as}$ signal (at 4 times the audio sample frequency), which is used to latch the data words to the DACs and as a reference to the clock generator block for the up-sample filters. It consists of a digital PLL operating at the master clock signal MCLK (pin 5). In normal mode (i.e. in the event that the MCLK signal on pin 5 is a jitter free clock, with a frequency of integer multiples between 45 and 128, of 4 times the frequency of the WS signal) this block is able to generate a jitter free FASFDAC signal for optimum performance of the DAC. This mode is called the free running mode.

If, in some applications, there is considerable jitter on the MCLK while WS is more stable (less jitter), the phase-locked mode should be selected. This mode is normally not used and is not recommended.

UP-SAMPLE GENERATOR

This block generates the clocks for the up-sample filters.The external pinning of the $4f_{as}$ generator block is:

- MCLK (see Fig.4), which is a jitter free (maximum 30 ns jitter) external clock at any multiple integer from 45 to 128 times $4f_{as}$ (4 times the frequency of WS) of the I^2S-bus input, thus for a sample frequency of 38 kHz this clock frequency will range from 6.840 MHz to 19.456 MHz in multiples of 152 kHz.
- The select in-phase (SELINPH) or free running mode of the synthesizer 45 to 128. In the normal application the free-running mode is used and this pin is not connected (this pin is pulled down by an internal resistor). The phase-locked mode can be selected by hard-wiring this pin to V_{DDD} (pin 8). However, this mode is not recommended.

Test interface

This block controls the circuit in the test mode, which can be either an analog or digital test mode. Test pins TC (pin 1), AT/DT (pin 2), CMT (pin 23), SCOUT1 (pin 27) and SCOUT2 (pin 28) are not connected in Fig.6.

Up-sample filter and noise shaper

The signal flow applied to the up-sample filter and noise shaper blocks is the 4×18-bit parallel data words in two's complement format from the I^2S-bus interface at the audio sampling frequency. The signal flow from these blocks is the 4×15-bit parallel data words in two's complement format at a frequency of $4f_{as}$. Each of the four digital filters is a four times up-sampling filter. This up-sampling filter is an elliptic filter of 8th order.

The filters produce an attenuation of 29 dB (min) for signals outside the audio band. The noise shaper operates at $4f_{as}$ and reduces the word length from 22 bits to 15 bits which is the word length of the DAC.

DAC input signals

The following signals are input to the DAC blocks FL, FR, RL and RR:

- DATA WORD (bits 10 to 14). These 5 bits are used to control, via a thermometer decoder, the current of the 32 coarse current sources of the analog DAC part. The value of this data word determines the total coarse current flowing to the DAC current output. The value of the current of each coarse current source is determined by the following:

  R_{ref}; this is the current reference input at pin 14 and is at the same voltage level as V_{ref}. A resistor connected to OGND results in a current. This being the reference current of the coarse current sources and subsequently of the DAC in total.
- DATA WORD (bits 1 to 9). A current from one of the coarse current sources is fed into a 512 transistor matrix. The value of the DATA WORD (bits 1 to 9) determines which part of one coarse current flows to the DAC current output.
- DATA WORD (bit 15). This data word MSB controls the direction of the flow of the DAC output current by switching the current direction switch.
- V_{ref}. Voltage reference pin internally connected to a resistor divider to obtain half of the power supply voltage. This voltage is buffered and used as reference voltage input for the operational amplifiers and as a reference voltage in the DAC.
- POWER-UP. The analog signal on this pin controls the current biasing circuit of the DACs. This pin is connected internally via a high value resistor to V_{DDA}. Together with an external capacitor a soft switch-on of the DAC output currents is obtained. This pin can also be used as the analog mute input for all DAC output currents by pulling it to ground.

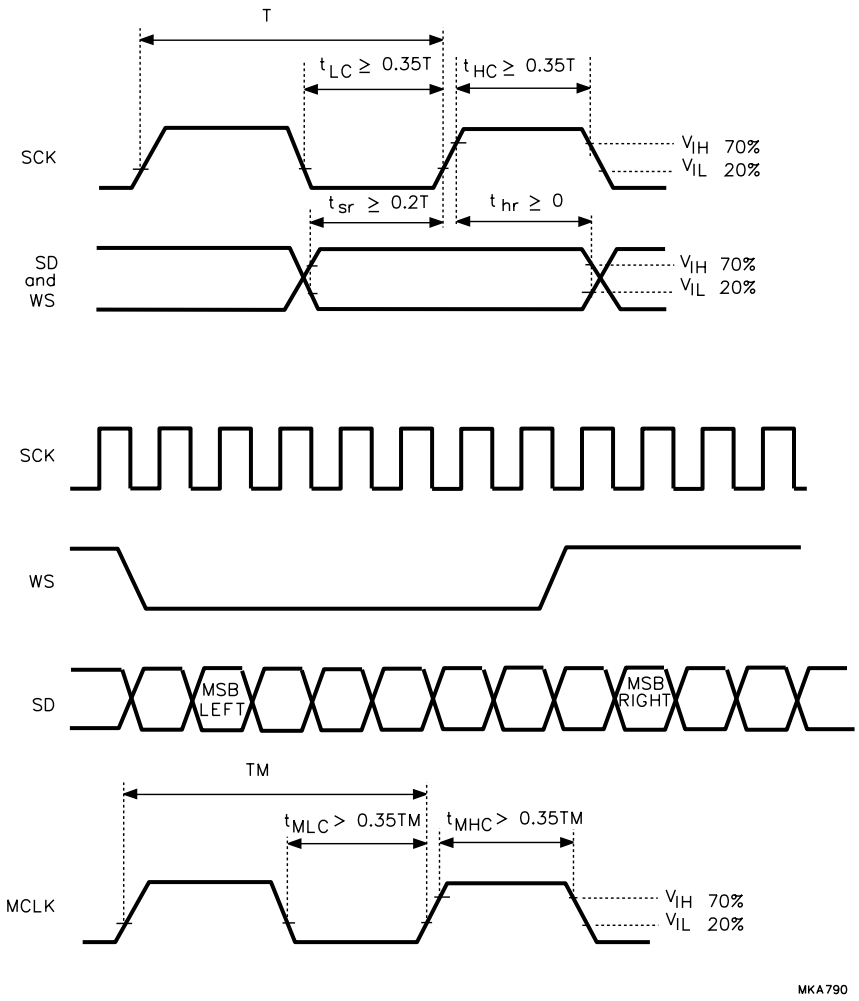


Fig.3 I²S-bus timing and format.

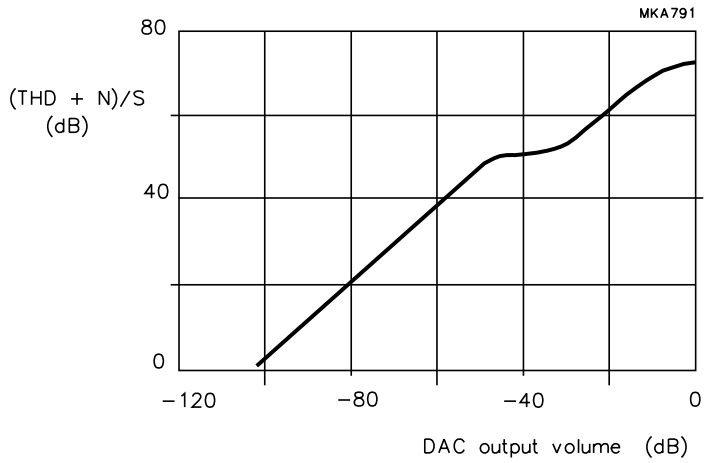


Fig.4 Total harmonic distortion plus noise-to-signal ratio as a function of output volume.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage	note 1	0	6.0	V
V_{DDA}	analog supply voltage	note 1	0	6.0	V
V_{DDO}	operational amplifier supply voltage	note 1	0	6.0	V
V_n	voltage on any other pin		0	V_{DD}	V
T_{xtal}	crystal temperature		–	+150	°C
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{es}	electrostatic handling	note 2	−2000	+2000	V

Notes

1. All voltages (pins 6, 7 and 15) referenced to ground.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	76	K/W

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{DDA} = V_{DDO} = 4.75 to 5.25 V; all voltage referenced to ground (pins 6, 7 and 15); measured in test circuit of Fig.6; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
V_{DDA}	analog supply voltage		4.75	5.0	5.25	V
V_{DDO}	operational amplifier supply voltage		4.75	5.0	5.25	V
I_{DDD}	digital supply current	MCLK = 6.84 MHz	–	10	17	mA
I_{DDA}	analog supply current	at digital silence	–	5	8	mA
I_{DDO}	operational amplifiers supply current	no operational amplifier load resistor	–	2	4	mA
P_{tot}	total power dissipation	MCLK = 6.84 MHz; at digital silence; no operational amplifier load resistor	–	85	145	mW
V_{IH}	HIGH level input voltage pins 1 to 5 and 23 to 26		$0.7V_{DDD}$	–	–	V
V_{IL}	LOW level input voltage pins 1 to 5 and 23 to 26		–	–	$0.2V_{DDD}$	V
V_{OH}	HIGH level output voltage pins 27 and 28	V_{DDD} = 4.5 V; I_O = –4 mA	4.1	–	–	V
		V_{DDD} = 5.5 V; I_O = –4.5 mA	5.1	–	–	V
V_{OL}	LOW level output voltage pins 27 and 28	V_{DDD} = 4.5 V; I_O = 4 mA	–	–	0.4	V
		V_{DDD} = 5.5 V; I_O = 4.5 mA	–	–	0.4	V
V_{ref}	reference input voltage	with respect to OGND	$0.45V_{DDO}$	$0.5V_{DDO}$	$0.55V_{DDO}$	V
Z_I	input impedance at pin 21	with respect to V_{DDO}	15	20	30	kΩ
		with respect to OGND	15	20	30	kΩ
V_I	input voltage pin 14	with respect to OGND	$0.43V_{DDO}$	$0.5V_{DDO}$	$0.57V_{DDO}$	V
$I_{ODAC(max)}$	maximum output current from DACs pins 10, 12, 17 and 19	R_{ref} = 20.5 kΩ; V_{DDO} = 5 V	400	500	600	µA
$V_{O(os)}$	DC offset voltage at pins 10, 12, 17 and 19	with respect to V_{ref}	–	5	–	mV
$V_{OH(O)}$	HIGH level output voltage of operational amplifiers at pins 11, 13, 18 and 20	note 1; R_L > 5 kΩ; R_{fb} = 3 kΩ; maximum signal	V_{DDO} – 1.3	V_{DDO} – 1	V_{DDO} – 0.45	V
$V_{OL(O)}$	LOW level output voltage of operational amplifiers at pins 11, 13, 18 and 20	note 1; R_L > 5 kΩ; R_{fb} = 3 kΩ; maximum signal	0.45	1.0	1.3	V
R_{pu}	internal resistance at pin 22	with respect to V_{DDO}	110	160	240	kΩ
R_{pd}	internal resistance at pins 1 to 3 and 23	V_i = V_{DDD}; with respect to DGND	27	–	80	kΩ

Note

1. R_L is the AC impedance of the external circuitry connected to the audio outputs in the application diagram of Fig.6.

AC CHARACTERISTICS

$V_{DDD} = V_{DDA} = V_{DDO} = 5$ V; $T_{amb} = 25$ °C; all voltages referenced to ground (pins 6, 7 and 15) measured in test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ANALOG						
DACs						
SVRR	supply voltage ripple rejection pins 9 and 16	f_{ripple} = 1 kHz; V_{ripple} = 100 mV (peak); C_{Vref} = 22 μF	30	46	–	dB
$\Delta I_{O(DAC)}$	maximum deviation of output level of the 4 DAC output currents with respect to the average of the 4 outputs	maximum volume	–	–	0.38	dB
α_{DAC}	crosstalk between the 4 DAC current outputs	2 outputs at digital silence; 2 outputs at maximum volume	–	–90	–60	dB
RES	DAC resolution		–	–	18	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz; 0 dB signal	–	–66	–56	dB
		f_i = 1 kHz; –60 dB signal; A-weighted	–	–36	–32	dB
DR	dynamic range	f_i = 1 kHz; –60 dB signal; A-weighted	92	96	–	dB
DS	digital silence	f_i = 20 Hz to 17 kHz; A-weighted	–	–110	–100	dB
Operational amplifiers						
G_v	open loop voltage gain		–	85	–	dB
PSRR	power supply ripple rejection	f_{ripple} = 3 kHz; V_{ripple} = 100 mV (peak)	–	90	–	dB
(THD + N)/S	total harmonic distortion plus noise as a function of the operational amplifiers signal	R_L > 5 kΩ (AC); R_{fb} = 3 kΩ; V_O = 0.28 V (p-p); f_i = 1 kHz; A-weighted	–	–82	–	dB
f_{ug}	unity gain frequency	open loop	–	4.5	–	MHz
Z_o	output impedance	R_L > 5 kΩ	–	1.5	150	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DIGITAL						
I^2S-BUS, UP-SAMPLING FILTER AND NOISE SHAPER						
f_{SCK}	serial clock input frequency	ASF = 38 kHz	1.368	–	19.456	MHz
t_{LC}	serial clock LOW time	at 20% V_{DDD}; $T = \frac{1}{f_{SCK}}$	0.35T	–	–	µs
t_{HC}	serial clock HIGH time	at 70% V_{DDD}; $T = \frac{1}{f_{SCK}}$	0.35T	–	–	µs
f_{WS}	word select input frequency		38	44.1	48	kHz
t_{sr}	set-up time from SDF, SDR and WS to HIGH going edge of SCK	$T = \frac{1}{f_{SCK}}$	0.2T	–	–	µs
t_{hr}	hold time from SDF, SDR and WS to HIGH going edge of SCK	$T = \frac{1}{f_{SCK}}$	0	–	–	µs
f_{MCLK}	master clock input frequency	$N \times 4 \times f_{WS}$; where N = integer	$45 \times 4f_{WS}$	$64 \times 4f_{WS}$	$128 \times 4f_{WS}$	kHz
t_{MLC}	master clock LOW time	$TM = \frac{1}{f_{SCK}}$	0.35TM	–	–	µs
t_{MHC}	master clock HIGH time	$TM = \frac{1}{f_{SCK}}$	0.35TM	–	–	µs
PR	pass band ripple of digital filter	with sample-and-hold from DAC	–	0.46	–	dB
α_{SB}	stop band attenuation	f_i > 22 kHz; no post filter	29	–	–	dB

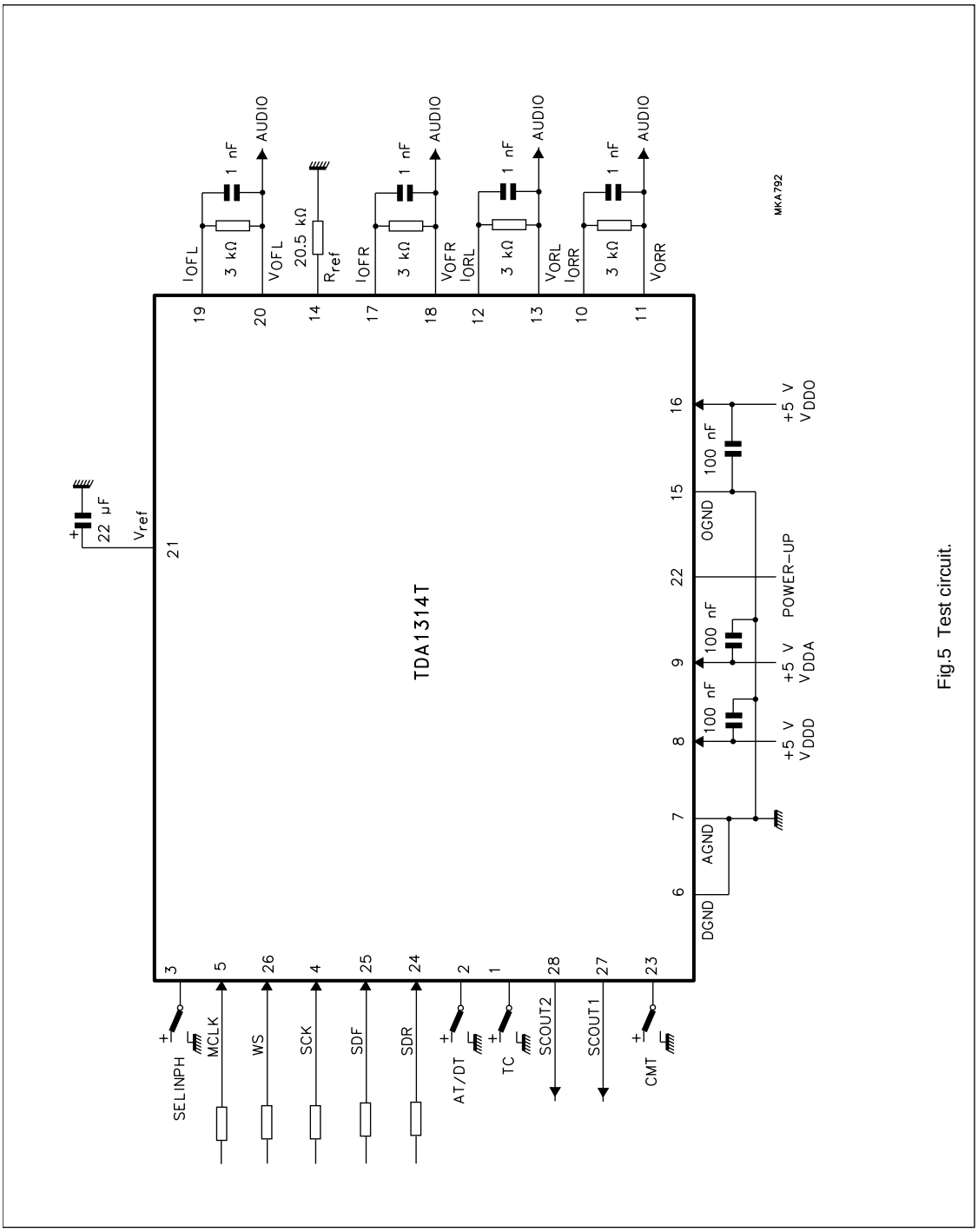


Fig.5 Test circuit.

APPLICATION INFORMATION

The application diagram is illustrated in Fig.6.

All pins used for testing (pins 1, 2, 23, 27 and 28 need not to be connected due to internal resistors being connected to ground or being used as test outputs. In the normal free-running mode it is also not required to connect pin 3.

Jitter on the clock edges of MCLK must be as low as possible so as not to deteriorate the DAC THD performance. The jitter time must not be greater than 30 ns.

V_{ref} is the voltage reference pin with an internal resistor divider. A capacitor of 22 μF is used to get the specified power ripple rejection ratio.

The output operational amplifiers are current-to-voltage converters by means of the 3 kW resistors connected between the DAC current outputs (pins 10, 12, 17 and 19) and the voltage outputs (pins 11, 13, 18 and 20) respectively. The voltage on the DAC current outputs is equal to the operational amplifiers virtual ground at V_{ref} in the event that the operational amplifier is used according to the application diagram of Fig.6.

Care should be taken, in order to reduce the electromagnetic compatibility (EMC) that the bandwidth of the digital signals being applied to pins MCLK, WS, SCK, SDF and SDR is not larger than necessary. This can be achieved by controlling the slew rate of the digital source outputs or connecting a series resistor close to the digital source output of the driving circuits.

The resistor connected between R_{ref} (pin 14) and ground is the current reference of the DACs. The voltage on R_{ref} is equal to V_{ref}.

On the printed-circuit board V_{SSA} (pin 7) is also the substrate and has the most negative voltage of the IC, a large as possible ground plane is therefore recommended. The connection between V_{SSA}, V_{SSD} and V_{SSO} must be as short as possible. Pins V_{DDO} and V_{DDA} (pins 9 and 16) must have capacitors connected to the V_{SSA} ground plane closest to the chip. Pin V_{DDD} (pin 8) is fed via a small series resistor (25 Ω). This resistor must be connected as close as possible to pin 8.

The POWER-UP (pin 22) is connected via an electrolytic capacitor to ground. This results in a smooth rising of the DAC output currents at power-on. If this is not required then this capacitor can be omitted.

Suppression of the higher harmonics by the up-sample filter should be sufficient to protect the amplifiers and the tweeter loudspeakers from excessive HF noise. The band around $4f_s$ cannot be attenuated by the 4ASF filter and is only attenuated by the sample-and-hold effect of the DAC. At frequencies above 100 kHz, additional attenuation achieved by the 1st order post filter, which is built around the buffer operational amplifiers. In total a 2nd order level of filtering can be found above 100 kHz. In terms of power the audio out-of-band power is approximately 15×10^{-4} of the audio in-band power.

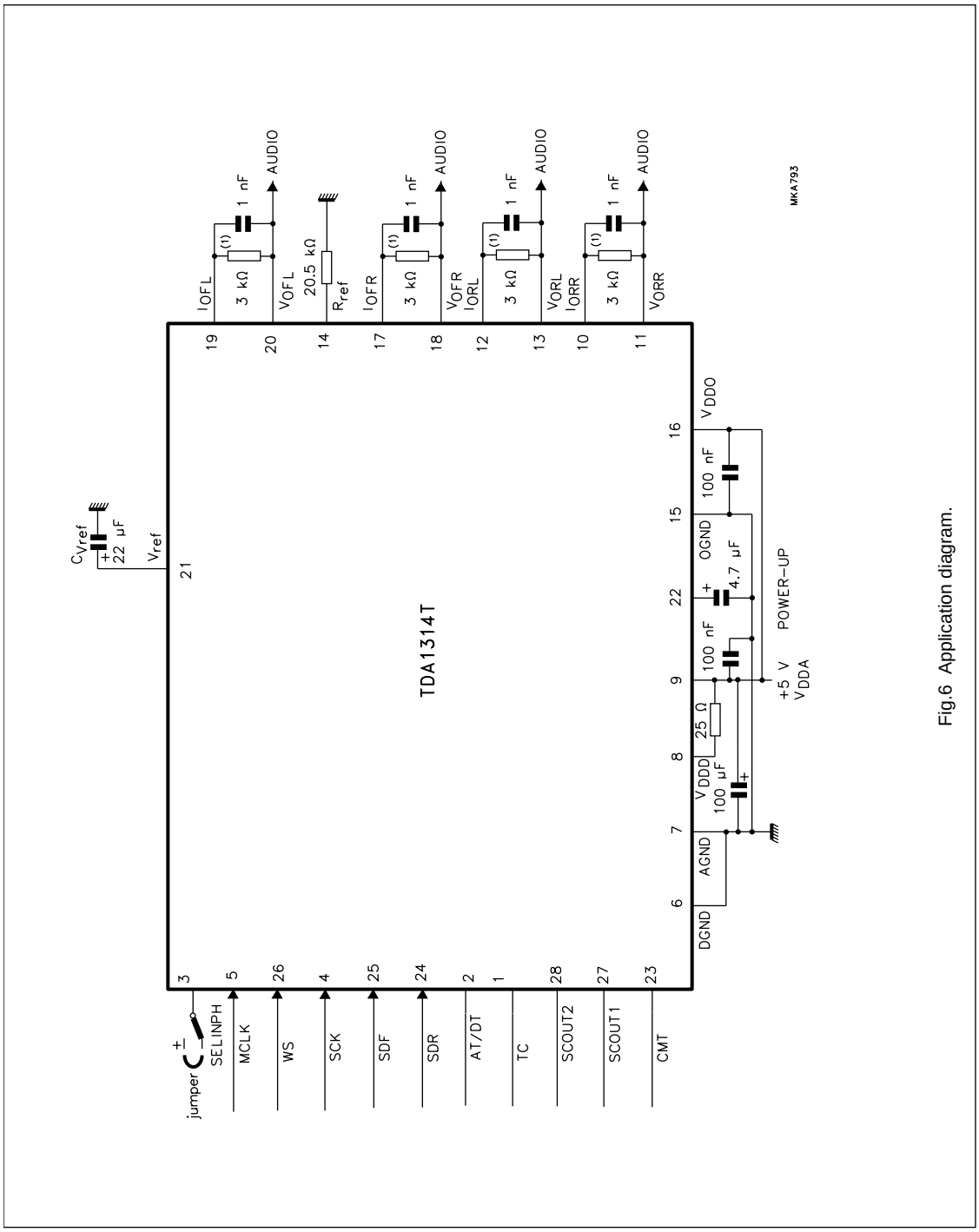
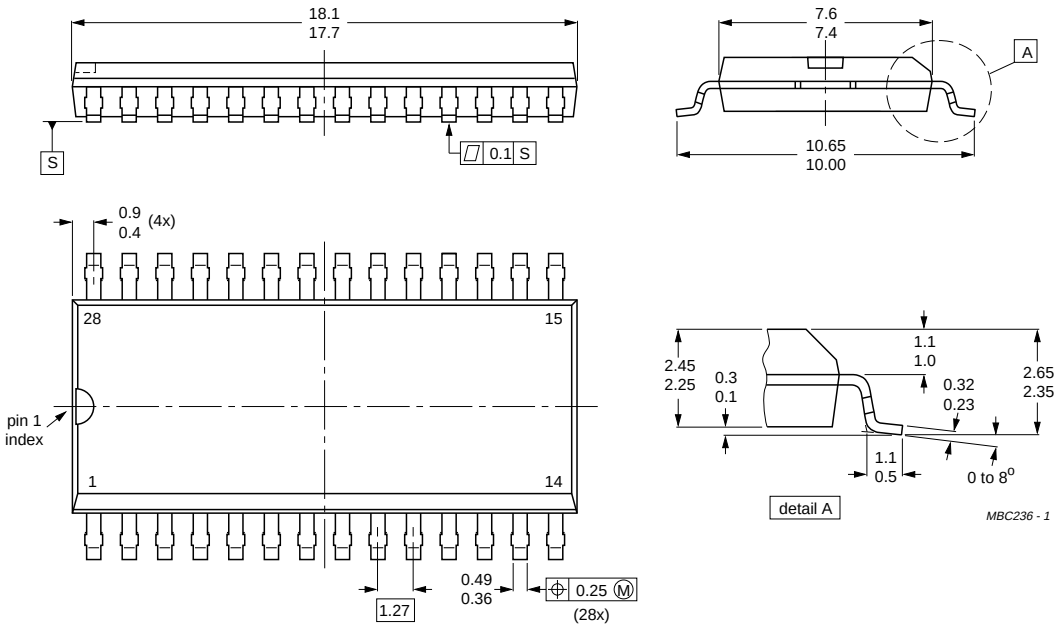


Fig.6 Application diagram.

PACKAGE OUTLINE



Dimensions in mm.

Fig.7 Plastic small outline package; 28 leads; body width 7.5 mm (SO28; SOT136-1).

SOLDERING INFORMATION

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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