DATA SHEET

SAA2521
Masking threshold processor for MPEG layer 1 audio compression applications

Preliminary specification
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

Masking threshold processor for MPEG layer 1 audio compression applications

SAA2521

FEATURES

- Stereo or 2-channel mono encoding
- Status may be read continuously
- Microcontroller interface
- I^2S-interfaces
- Allocation algorithm including optional emphasis correction (for 44.1 kHz)
- Reduced power consumption
- 4 V nominal operating voltage capability.

GENERAL DESCRIPTION

The SAA2521 performs the adaptive allocation and scaling function for calculating the masking thresholds and sub-band sample accuracy in MPEG layer 1 applications. The SAA2521 is intended for use in conjunction with the stereo filter codec SAA2520.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA2521GP	44	QFP	plastic	SOT205AG(1)

Note

1. SOT205-1; 1996 August 23.

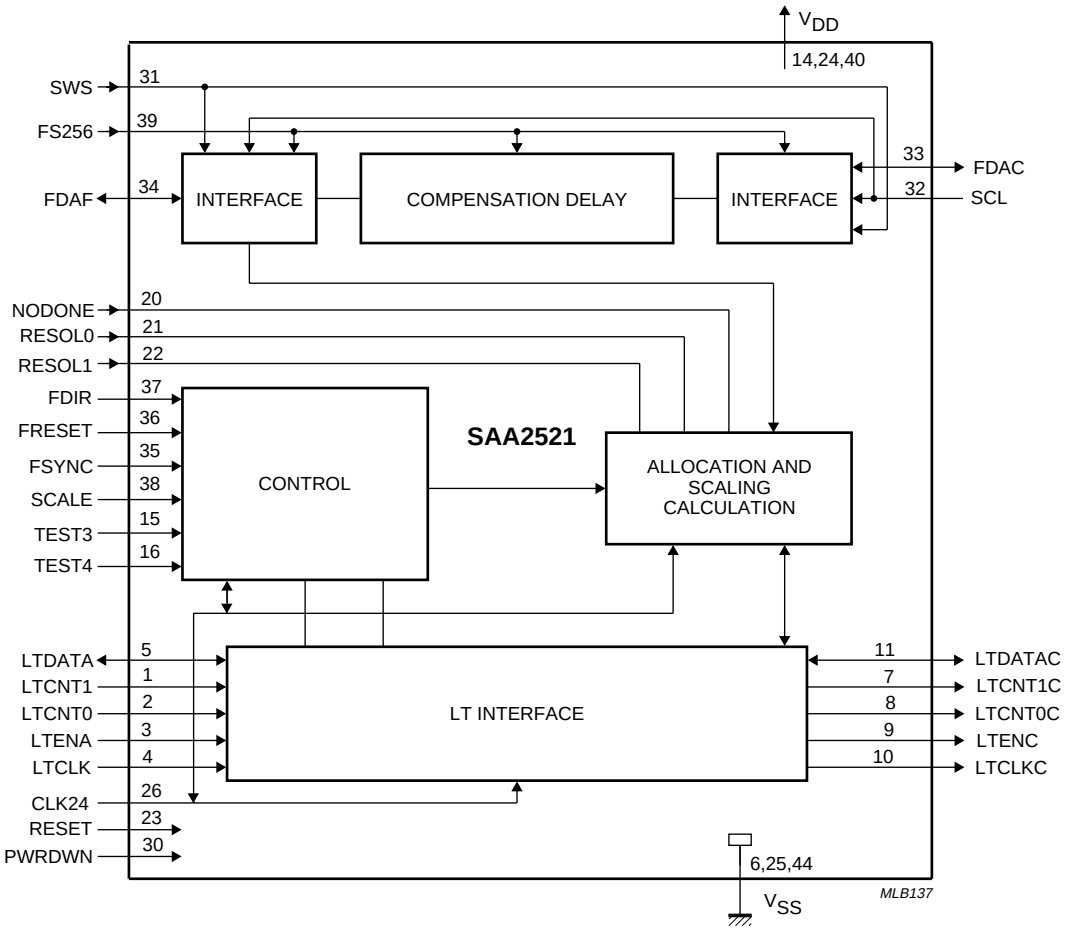


Fig.1 Block diagram.

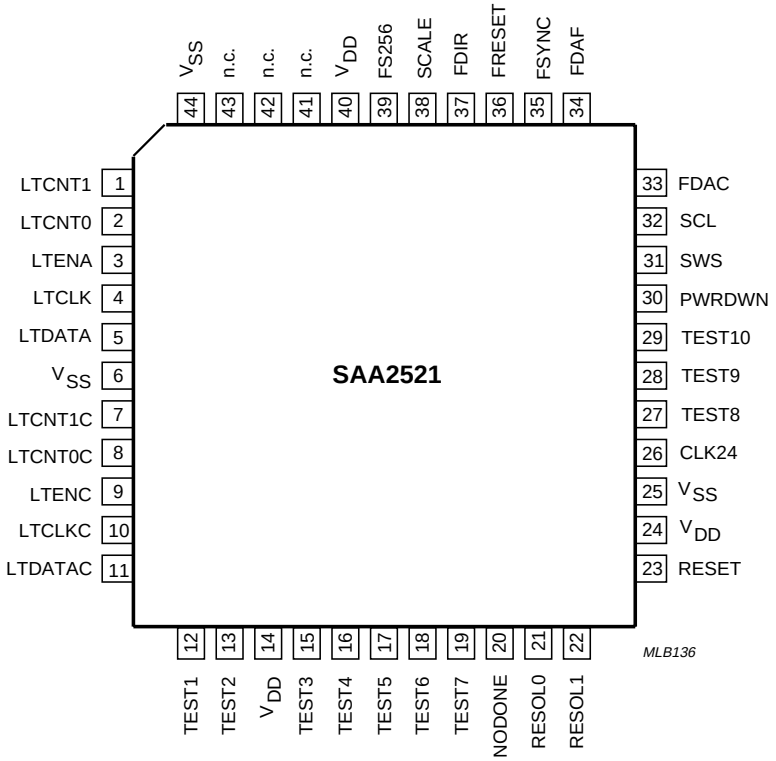


Fig.2 Pin configuration.

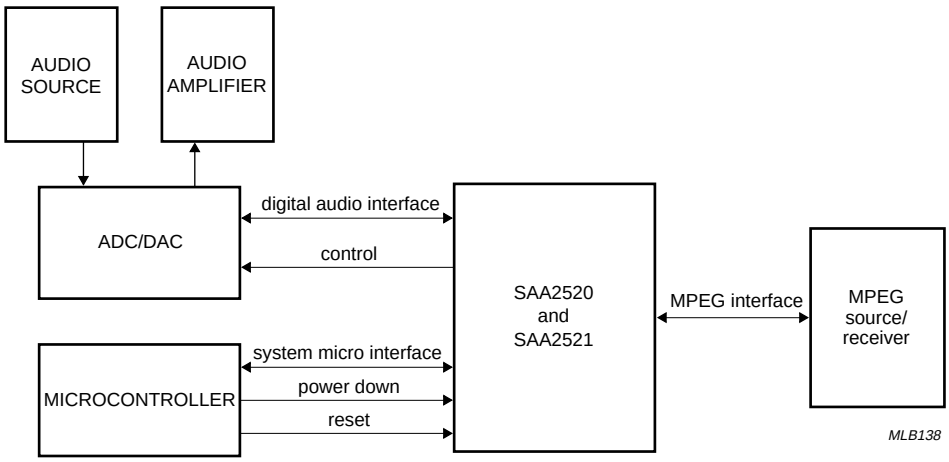


Fig.3 MPEG codec system data flow diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE
LTCNT1	1	mode control 1, microcontroller interface input	I
LTCNT0	2	mode control 0, microcontroller interface input	I
LTENA	3	enable microcontroller interface input	I
LTCLK	4	bit clock microcontroller interface input	I
LTDATA	5	data, microcontroller interface (3-state inputs/outputs)	I/O
V_{SS}	6	supply ground (0 V)	
LTCNT1C	7	control 1; microcomputer interface	O
LTCNT0C	8	control 0; microcomputer interface	O
LTENC	9	enable microcontroller interface	O
LTCLKC	10	bit clock; microcontroller interface	O
LTDATAC	11	data; microcontroller interface, (3-state inputs/outputs)	I/O
TEST1	12	test output; do not connect	
TEST2	13	test output; do not connect	
V_{DD}	14	positive supply voltage (+ 5 V)	
TEST3	15	test mode input; to be connected to V_{DD}	
TEST4	16	test mode input; to be connected to V_{DD}	
TEST5	17	test input; to be connected to V_{SS}	
TEST6	18	test input; to be connected to V_{SS}	
TEST7	19	test input; to be connected to V_{SS}	
NODONE	20	no done state selection input	I
RESOL0	21	resolution selection 0 input	I
RESOL1	22	resolution selection 1 input	I
RESET	23	active HIGH reset input	I
V_{DD}	24	positive supply voltage (+ 5 V)	
V_{SS}	25	supply ground (0 V)	
CLK24	26	24.576 MHz processing clock input	I
TEST8	27	test input; to be connected to V_{SS}	
TEST9	28	test input; to be connected to V_{SS}	
TEST10	29	test input; to be connected to V_{SS}	
PWRDWN	30	power-down input	I
SWS	31	word selection input; (Filtered) - I^2S-interface	I
SCL	32	bit clock input; (Filtered) - I^2S-interface	I
FDAC	33	filtered data (Filtered) - I^2S-interface (3-state inputs/outputs)	I/O
FDAF	34	filtered data (Filtered) - I^2S-interface (3-state inputs/outputs)	I/O
FSYNC	35	sub-band synchronization on (Filtered) - I^2S-interface, input	I
FRESET	36	reset signal input from SAA2520	I
FDIR	37	direction of the I^2S-interface; input	I
SCALE	38	scale factor index select (note 1)	I
FS256	39	system clock input; sample frequency $\times$ 256	I
V_{DD}	40	positive supply voltage (+ 5 V)	

SYMBOL	PIN	DESCRIPTION	TYPE
n.c.	41	not connected	
n.c.	42	not connected	
n.c.	43	not connected	
V_{SS}	44	supply ground (0 V)	

Note to the Pinning Description

1. The scale input must be set LOW for use with the SAA2521.

FUNCTIONAL DESCRIPTION

Coding System

This efficient MPEG audio encoder is used in conjunction with the SAA2520 filter codec (bit rates of 384, 256, 192 and 128 k bits/s). The encoder utilizes a system producing sub-band samples from an incoming digital audio signal. This relies upon the audibility of signals above a given level and upon high amplitude signals masking those of lower amplitude. Although each sub-band signal is of approximately 750 Hz bandwidth, it possesses considerable overlap with those adjacent to it.

During the process of encoding, the masking threshold processor analyses the broadband audio signal at sampling frequency f_S by splitting it into 32 sub-band signals at a sampling frequency (f_S/32).

The coded signal consists of frames conveying the information corresponding to the sub-band samples. These also include a synchronization pattern identifying the start of each new frame. The allocation information for the 32 sub-bands is transferred as 4-bit values. If the amplitude of a sub-band signal is below the masking threshold it will be omitted from the coded signal.

The duration of a MPEG frame depends upon sampling frequency and is adjusted to 384 divided by f_S.

Adaptive Allocation and Scaling

The coding system calculates the masking power of the sub-band signals and adds the masking threshold. Sub-band signals with power below this threshold denote information to be discarded. Non-masked signals are coded using floating point notation in which a mantissa corresponds in length to the difference between peak power and masking threshold. The process is repeated for every MPEG frame and is known as the Adaptive Allocation of the available capacity.

Encoding Mode

Signal FDIR sets the data flow direction on the Filtered-I^2S-interface. In the encoding mode (FDIR LOW) the device will accept samples from FDAF. These will be delayed by a number of sample periods depending upon the setting of the SCALE input. In the instance of operation with the SAA2520 (SCALE = logic 0) this delay will be 480 SWS periods. This will ensure alignment of the data with the computed allocations.

After the delay the samples will be presented on FDAC (pin 33). The circuit also performs all the calculations required to build the allocation table which is used in the codec (SAA2520). When used with the SAA2520 the calculated scale factor indices are sent via the LT interface. These operations are performed for every frame of the sub-band codec.

In order to synchronize with the codec and utilize the correct tables for the calculations the SAA2521 frequently requests the status of the codec. It monitors the bit-rate, sample frequency, operation mode and the emphasis information and uses the 'ready to receive' bit of the codec to determine the moment of the transfer of allocation information.

Decoding Mode

In the decoding mode (FDIR HIGH) the SAA2521 will take samples from FDAC which will be presented on the FDAF after a delay of 160 SWS periods. The LT interface between microcontroller and codec (SAA2520) will only be affected by the 'ready to receive' bit from the codec (SAA2520).

Microcontroller Interface Operation

Information on the interface between microcontroller and codec (SAA2520) will flow in a regular sequence synchronized with the codec (SAA2520):

- with every FSYNC the SAA2521 will read the status of the codec (SAA2520)
- Following the calculation of the allocation and scale factors the SAA2521 will send the first allocation information unit (16-bits). It will then continuously read the codec (SAA2520) status to ascertain when it is able to receive further allocation information units. When the transfer of these units is complete the SAA2521 will send settings and (for SCALE = logic 0) scale factor indices.
- The extended settings will be sent to the codec as soon as possible after reception from the microcontroller.

The microcontroller communicates with the SAA2521 in a similar fashion:

- status can be read continuously. The SAA2521 will output a copy of the codec (SAA2520) status on the LTDATA line except for the 'ready to receive' bits which are generated by the SAA2521. These indicate whether the SAA2521 is ready to receive the next settings or extended settings.
- settings can be sent following every occasion that the 'ready to receive' bit 'S' changes to logic 1.
- extended settings can be sent following each occasion that the 'ready to receive' bit 'E' changes to logic 1.

Mode Control

Operation is controlled by the FRESET and FDIR signals. FRESET causes a general reset. The FDIR signal is sampled at the falling edge of the FRESET signal to determine the operation mode:

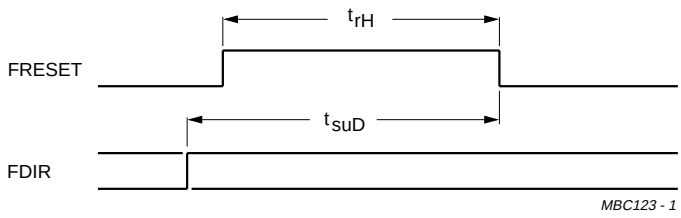
FDIR = logic 1	decoding mode, SAA2521 in feed-through mode
FDIR = 0	encoding mode, SAA2521 in calculation mode

Fig.4 shows the timing diagram for FRESET and FDIR.

Resolution Selection

The (SAA2521) is designed for operation with input devices (ADCs) which may possess a different sample resolution capability, i.e. audio sample inputs into the sub-band filters. Pins RESOL0 and RESOL1 (respectively pins 21 and 22) may be utilized to adjust the allocation information calculation to the resolution of the samples.

With the instance of pin 20 (NODONE) being HIGH, all available bits in the bit-pool will be allocated. If NODONE is LOW, no bits will be allocated to the sub-bands with energy levels below the theoretical threshold for the selected resolution.



$T_{rH} > 5T_{CLK24} = 210$ ns (for CLK24 = 24.576 MHz) min. time FRESET HIGH
$T_{sD} < 0$ ns min. set-up time FDIR to FRESET = LOW

Fig.4 Timing: FRESET and FDIR.

Power-down Mode Switching

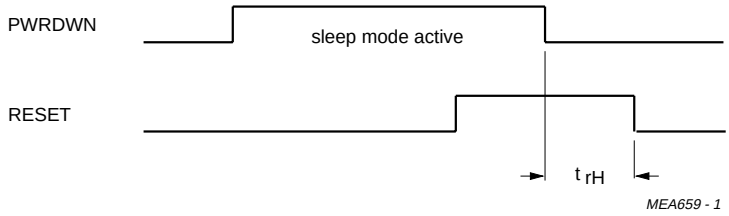
When the potential on the RESET pin (pin 23) is held HIGH for at least $5T_{CLK24}$ clock periods, the device will be reset after which it will operate in its decoding mode.

The power-down mode is activated when the PWRDWN pin (pin 30) is held HIGH. The 3-state buffers will be set to a high impedance while the normal outputs will retain the state attained prior to this mode being entered. This mode can only be used if other associated circuits react accordingly. The power-down mode is de-activated by a reset action.

Fig.5 shows the operation for the power-down mode switching.

Table 1 Resolution selection.

RESOL1	RESOL0	RESOLUTION
0	0	16-bits
0	1	18-bits
1	0	14-bits
1	1	15-bits



$T_{rH} > 5T_{CLK24}$ = 210 ns (for CLK24 = 24.576 MHz) minimum time RESET HIGH

Fig.5 Power-down mode switching.

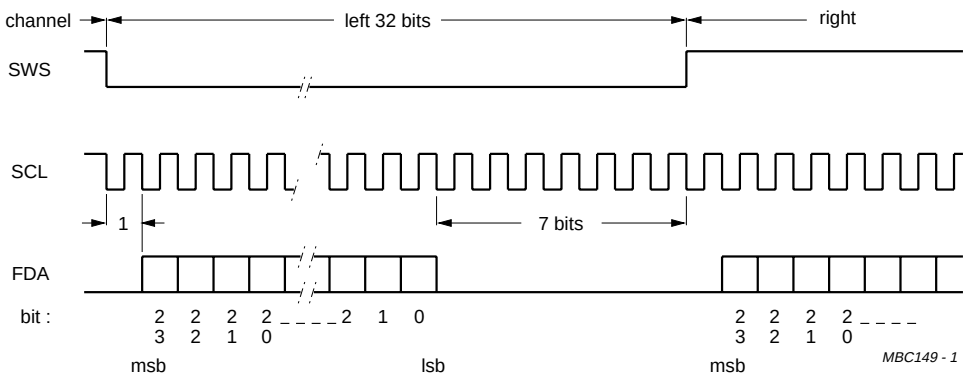


Fig.6 Format for transferring filtered data.

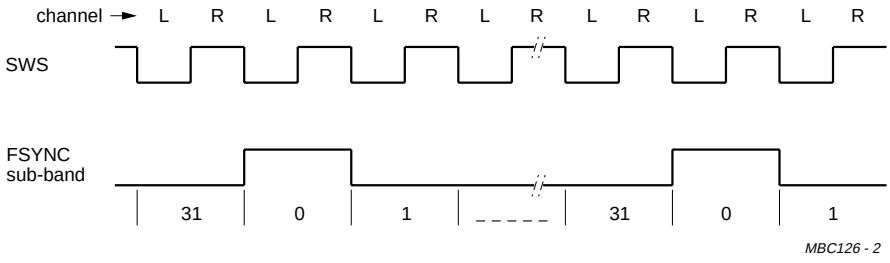


Fig.7 FSYNC related to SWS 0 data transfer period.

Table 2 The (Filtered) - I^2S-interface.

SWS	input	word selection	F_S
SCL	input	bit clock	64 F_S
FDAF	bi-directional	filtered data to/from the filter section of SAA2520	
FDAC	bi-directional	filtered data to/from the codec section of SAA2520	
FSYNC	input	filter synchronization	F_S/32

Table 3 The (Filtered) - I^2S-interface.

FRESET	input	reset
FDIR	input	Filtered - I^2S-interface direction of data flow

(Filtered) - I^2S-interfaces

Interfaces with the sub-band filter and codec (SAA2520) consist of the following signals.

Fig.6 shows the format for transferring filtered data.

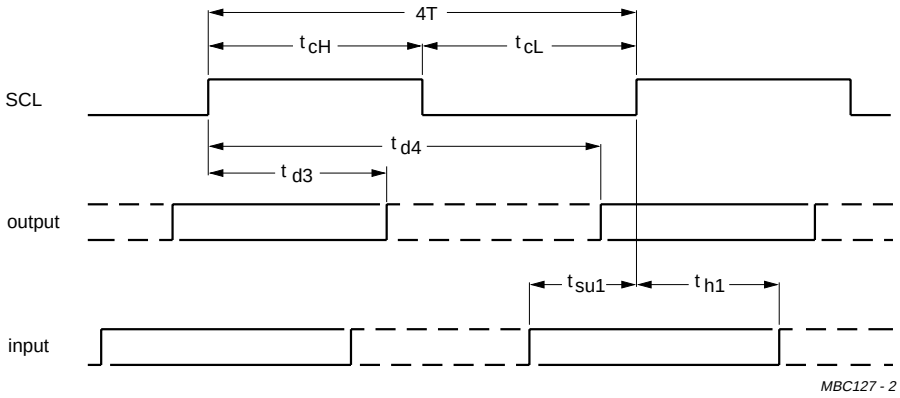
F_S 256 must be provided as system clock. This frequency is used by the interfaces with the SAA2520.

The frequency of the SWS signal (pin 31) is equal to the sample frequency F_S. Bit clock SCL (pin 32) is 64 times the sample frequency; thus each SWS period contains 64 data bits, 48 of which are actually used in data transfer. The half period during which SWS is logic 0 is used to transfer Left-channel information while that during which it is 1 permits transfer of Right-channel data.

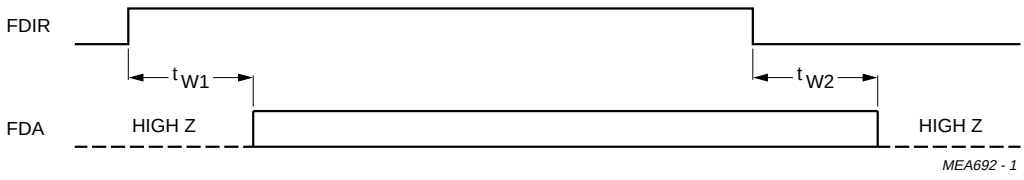
The 24-bit samples are transferred with the most significant bit first. This bit is transferred during the bit clock period, one bit time after the change in SWS.

FSYNC signal is provided for the purposes of synchronization and indicates the portion of the SWS period during which the samples of sub-band 0 are transferred.

Fig.7 shows the relationship between FSYNC and the SWS 0 data transfer period.



OUTPUT applies to FDAF and FDAC in the output mode.
INPUT applies to FDAF and FDAC in the input mode, SWS and FSYNC.
T = one F_s256 cycle time
$t_{cH} \geq T + 35$ ns minimum HIGH time SCL
$T_{cL} \geq T + 35$ ns minimum LOW time SCL
$t_{d3} \geq 2T - 10$ ns hold time output after SCL HIGH
$t_{d4} \leq 3T + 60$ ns delay time output after SCL HIGH
$t_{s1} \geq 20$ ns set-up time input before SCL HIGH
$t_{h1} \geq T + 35$ ns hold time input after SCL HIGH



$t_{w1} \geq 3T$ minimum time high impedance to FDA enabled
$t_{w2} \geq 2T + 35$ ns maximum time FDA enabled to high impedance

Fig.8 (Filtered) - I^2S-interface timing.

Table 4 SAA2521 interface with microcontroller.

LTCLK	input	bitclock
LTDATA	bi-directional	data
LTCNT0	input	control line 0
LTCNT1	input	control line 1
LTENA	input	enable

Table 5 SAA2521 interface with SAA2520.

LTCLKC	output	bit clock
LTDATAC	bi-directional	data
LTCNT0C	output	control line 0
LTCNT1C	output	control line 1
LTENC	output	enable

Table 6 SAA2521 interface control lines functions.

LTCNT1(C)	LTCNT0(C)	MODE	FROM	TO	TRANSFER OF
0	0	extended settings	microcontroller	SAA2520	8-bits
0	1	allocation (see note)	SAA2521	SAA2520	16/48 × 16-bits
1	0	settings	microcontroller	SAA2520	16-bits
1	1	status	codec	microcontroller	8 or 16-bits

Microcontroller Interface

Two microcontroller interfaces are provided; one for connection to the microcontroller interface of the SAA2520, the other to connect to the system controller. Information is conveyed via the SAA2521 which executes monitoring and extracts signals (e.g. settings and synchronization) essential to its operation. Additionally it also sends allocation information to the SAA2520. However, the SAA2521 does not monitor the external settings bits from the microcontroller (see Extended Settings).

The SAA2521 is a slave on the interface with the microcontroller which is active only when the enable signal LTENA (pin 3) is logic 1. This permits connection of this interface to other devices. Only the enable signal is not common to all devices.

SAA2521 is master on the interface with the SAA2520 and provides all signals with the exception of the data in the instance of status transfer from SAA2520 to SAA2521.

Information conveyed via these interfaces is transferred in 8 or 16-bit serial units with the type of information designated by the control lines (LTCNT1(C) and LTCNT0(C)).

A transfer of information begins when the master sets the control lines for the required action. It then sets the LTENA/C line to logic 1. Once this signal is established the slave determines the kind of action required and prepares for the transfer of data.

When the master supplies the LTCLK/C signal, data is transferred either to or from the slave in units of 8-bits; the least significant bit is always transferred first. A transfer of 16-bits is made in two, 8-bit units with the most significant 8-bit unit first. In between the two 8-bit units the LTENA/C signal remains logic 1.

Fig.9 shows an example of information transfer via SAA2521 interfaces.

Note to Table 6

This mode only on the interface between SAA2521 and SAA2520.

If SCALE = logic 1 then 16 × 16-bits

If SCALE = logic 0 then 48 × 16-bits

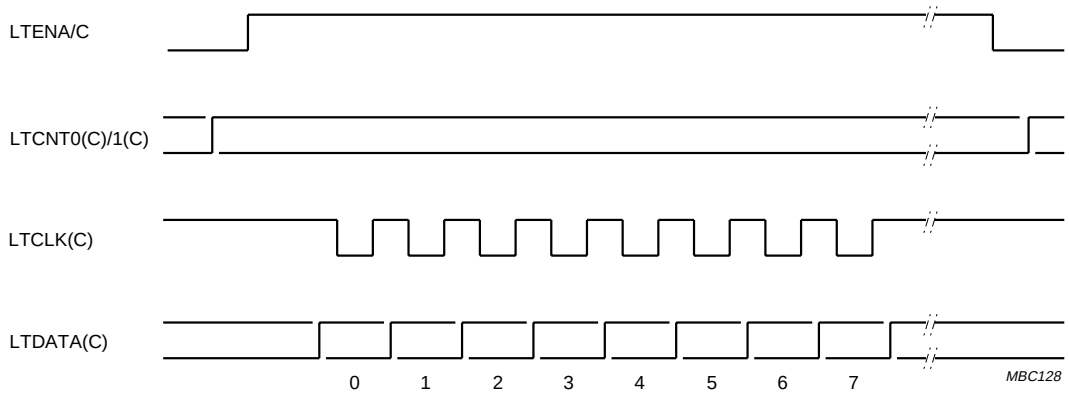
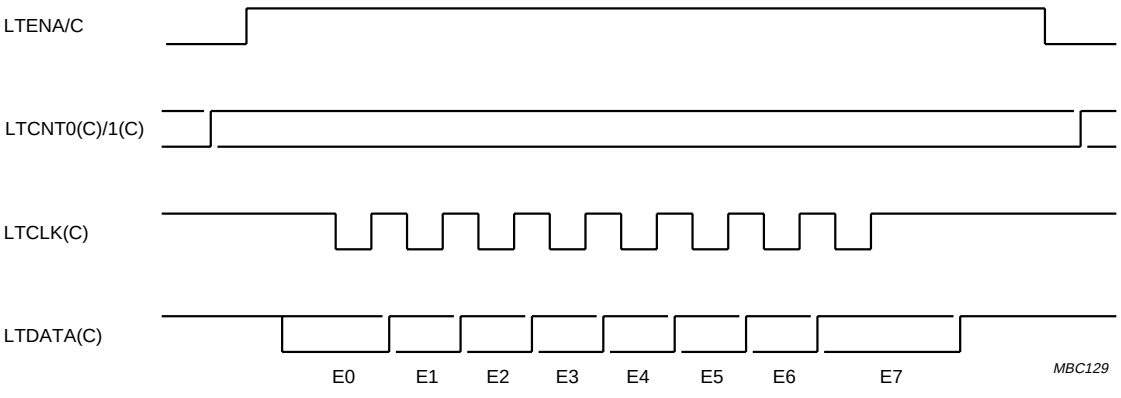


Fig.9 Example of information transfer via SAA2521 interfaces.



Refer to the SAA2520 description for the meaning of these bits as they pass SAA2521 unchanged.

Fig.10 Extended settings (LTCNT1 and LTCNT0)

Extended settings (LTCNT1(C) = logic 0, LTCNT0(C) = logic 0)

Eight information bits, generated by the microcontroller, are transferred in this mode. The SAA2521 will transfer these bits to the SAA2520 as soon as possible but does not monitor this information.

Fig.10 shows the relationship of the extended settings.

Allocation and SCALING information (LTCNT1C = logic 0, LTCNT0C = logic 1)

In the encoding mode (FDIR = logic 0) the SAA2521 will transfer allocation information to the SAA2520. This will occur once for every SAA2520 frame.

The information will consist of 16 transfers each of 16-bits. To synchronize the SAA2521 operation with that of the SAA2520, following the first 16-bit transfer of allocation data the SAA2521 checks the SAA2520 status to ensure it is ready to receive the remainder of the allocation information. Transfer of allocation data is completed by sending settings. Between 16-bit transfers the LTENC line returns to 0 as shown in Fig.11.

Fig.12 shows the order in which the bits occur on the interface during allocation information transfer.

The 4-bit sub-band allocation unit contains the number of bits allocated to the sub-band MINUS 1. A value of 0000 indicates no bits allocated to that sub-band.

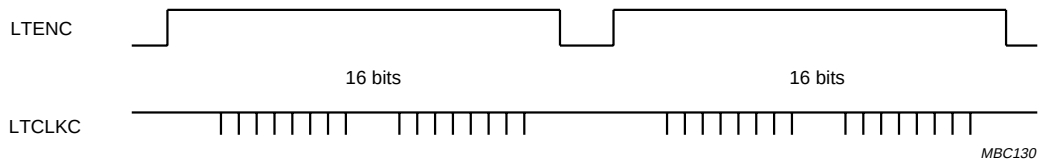


Fig.11 LTENC behaviour for 16-bit transfers.

Table 7 Allocation and SCALING information.

MSB			BITS			LSB	CHANNEL	SUB-BAND	
A15	–	A14	–	A13	–	A12	L	2 *	COUNT
A11	–	A10	–	A9	–	A8	R	2 *	COUNT
A7	–	A6	–	A5	–	A4	L	(2 *	COUNT) + 1
A3	–	A2	–	A1	–	A0	R	(2 *	COUNT) + 1

Table 8 Allocation and SCALING information.

MSB		BITS		LSB	CHANNEL	CONTENTS
SL15	–	SL14	–		---	00
SL13	–	SL12 - SL11 - SL10 - SL9	–	SL8	L	SCALE FACTOR (COUNT)
SL7	–	SL6			---	00
SL5	–	SL4 - SL3 - SL2 - SL1	–	SL0	R	SCALE FACTOR(COUNT)

With stereo encoding, Left and Right channels are designated **L** and **R.** This changes to channels I or II for 2-channel mono mode. If SCALE = logic 0 the transfer of allocation information will be followed by the transfer of scale factors. Each 16-bit transfer contains two scale factor indices.

Algorithm showing the process of information transfer:

COUNT: = logic 0

SEND ALLOCATION (COUNT)

REPEAT

READ STATUS

UNTIL

READY-TO-RECEIVE

FOR COUNT: = 1 to 15

DO

SEND ALLOCATION (COUNT)

SEND SETTINGS

IF SCALE = logic 0

THEN

FOR COUNT; = logic 0 TO 31

DO

SEND SCALE FACTORS (COUNT)

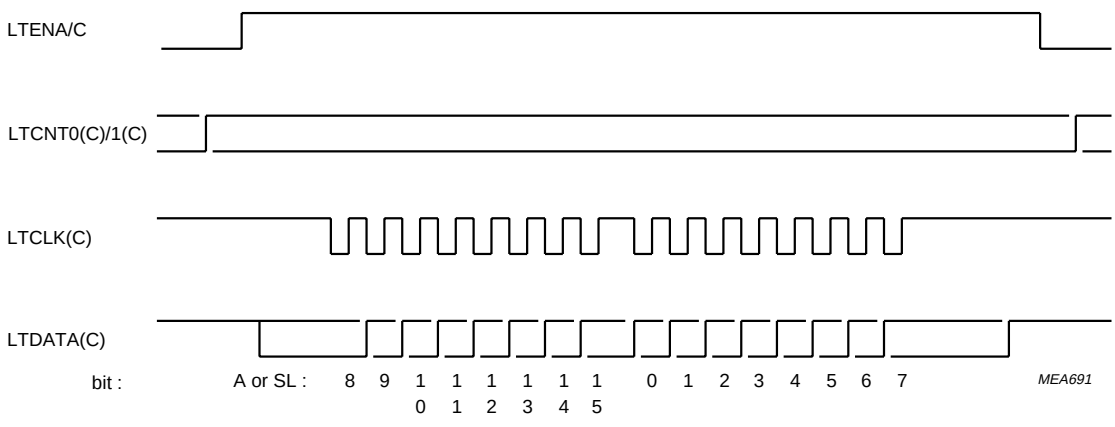


Fig.12 Order of interface bits during allocation information transfer.

SETTINGS (LTCNT1(C) = logic 1, LTCNT0(C) = logic 0)

Without using the information, the SAA2521 transfers microcontroller settings to the SAA2520.

Prior to sending settings, the microcontroller would utilize the SAA2521 status readings to ensure its readiness to accept and convey the data.

Following reception of the settings the SAA2521 will cause the ready-to-receive bit to be logic 0 until the settings have been sent to the SAA2520. The microcontroller can only send this data when this bit is logic 1.

Fig.13 shows the order of the bits on the interface.

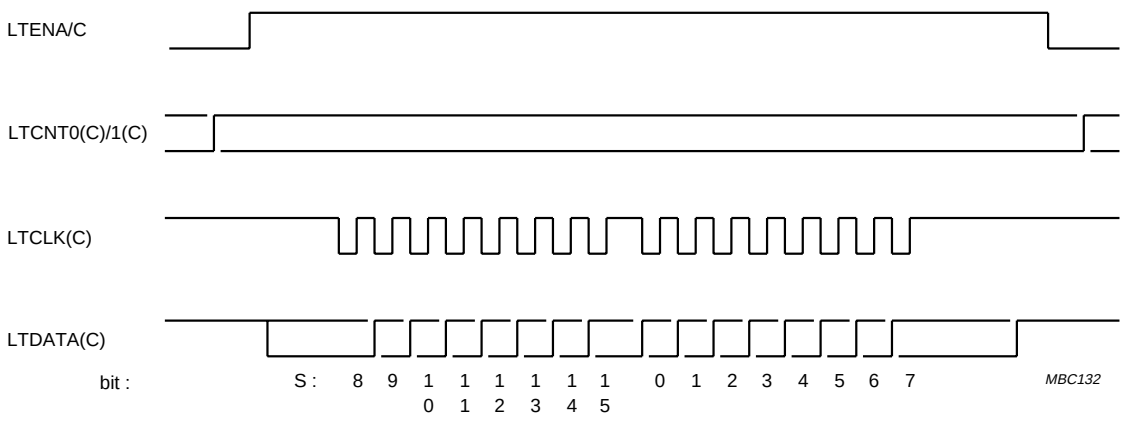


Fig.13 The order of bits on the interface.

Table 9 Microprocessor settings applied to the SAA2520 via the SAA2521.

MSB	BITS	LSB	NAME	FUNCTION	VALID IN
S15 – S14 – S13 – S12			bitrate index	bitrate indication	encode
S11 – S10			sample frequency	44.1, 48 or 32 kHz indic.	encode
S9			DECODE	1 - decode; 0 - encode	enc/dec
S8			ext 256f_s	1 - ext; 0 - int	enc/dec
S7			2-ch mono	1 - 2 ch mono; 0 - stereo	encode
S6			MUTE	1 - mute; 0 - no mute	enc/dec
S5			not used	–	enc/dec
S4			CH I	1 - CH I; 0 - CH II	decode
S3 – S2			Tr0 - Tr1	transparent bits	encode
S1 – S0			EMPHASIS	emphasis indication	encode

Status (LTCNT1(C) = logic 1, LTCNT0(C) = logic 1)

The SAA2520 and SAA2521 operation may be checked by reading these bits. All, except the ready-to-receive bits, are generated by the SAA2520.

The bit rate index indicates the bit rate of the sub-band signal in units of 32 kbits/s. The SAA2521 is designed for bit rates of 384, 256, 192 and 128 kbits/s only.

With EMPHASIS activated (S1 = T1 = 0 and S0 = T0 = 1) only bit rates 384 and 256 kbits/s can be used.

A ready-to-receive **S** or **E** indicates whether or not the SAA2521 can receive new settings or extended settings respectively from the microcontroller and should be checked prior to sending new information.

The SAA2521 can only be used to encode stereo (mode 00) signals and 2-channel mono (mode 10) signals.

During the decoding mode this bit indicates if the operation of the SAA2520 is in synchronization with the MPEG coded signal. Should this not be the case the SAA2520 cannot perform the decoding.

CLKOK indicates whether or not the F_S256 clock corresponds with the specified sample frequency.

EMPHASIS indication may be used to apply correct de-emphasis. During the encoding 50 / 15 μs mode the SAA2521 will correct the calculated allocation if emphasis is applied for a 44.1 kHz sampling frequency.

Table 10 Order of SAA2520 bits as they appear on the interface (see also Fig.14).

MSB			BITS			LSB	NAME	FUNCTION	VALID IN
T15	-	T14	–	T13	–	T12	bitrate index	bitrate indication	enc/dec
T11	-	T10					sample frequency	44.1, 48 or 32 kHz indic.	enc/dec
T9							ready-to-rec S	1 - ready; 0 - not ready	enc/dec
T8							ready-to-rec E	1 - ready; 0 - not ready	enc/dec
T7	–	T6					MODE	sub-band signal mode ID	enc/dec
T5							SYNC	synchronization indic.	dec
T4							CLKOK	1 - OK; 0 - not OK	enc/dec
T3	–	T2					Tr0 - Tr1	transparent bits	enc/dec
T1	–	T0					EMPHASIS	emphasis indication	enc/dec

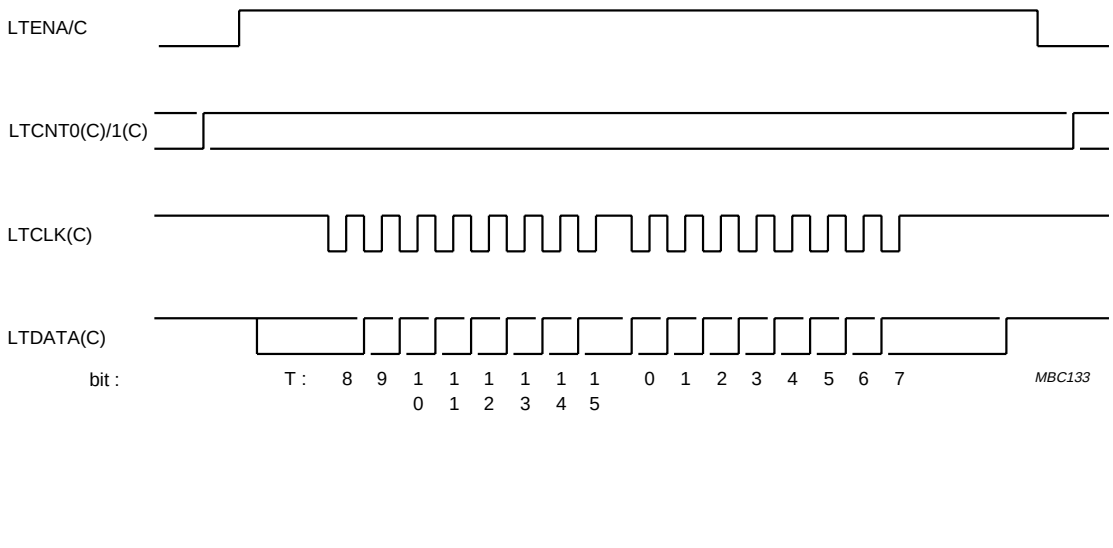


Fig.14 Order of appearance of bits on the interface.

Sample frequency indication.

MSB	LSB	
00	44.1 kHz	default value
01	48 kHz	
10	32 kHz	
11	--	do not use

MODE identification.

MSB LSB	MODE	OUTPUT
00	stereo	**L** and **R**
01	joint stereo	**L** and **R**
10	2 - channel mono	**I** or **II** as selected
11	1 - channel mono	mono, no selection

Frequency Range Limitation

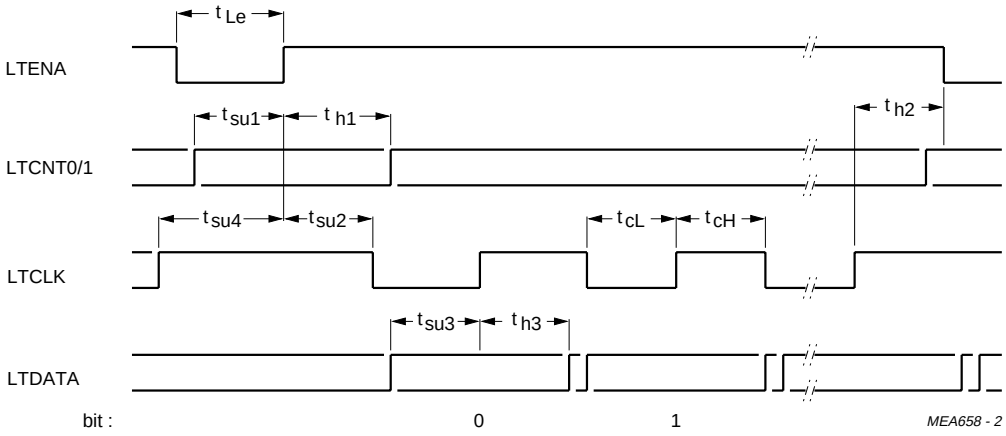
In encode mode the frequency range will be limited at lower rates. This is implemented by making the samples of higher frequency sub-bands equal to logic 0 before the allocation calculation. This automatically ensures that these sub-bands do not get any bits allocated.

The following table shows the sub-bands affected and the resulting frequency range.

The transfer of either 8-bits or 16-bits is permitted for the transfer of status information. When only 8-bits are transferred, these will always form the first byte and may be used in checking the ready-to-receive bit.

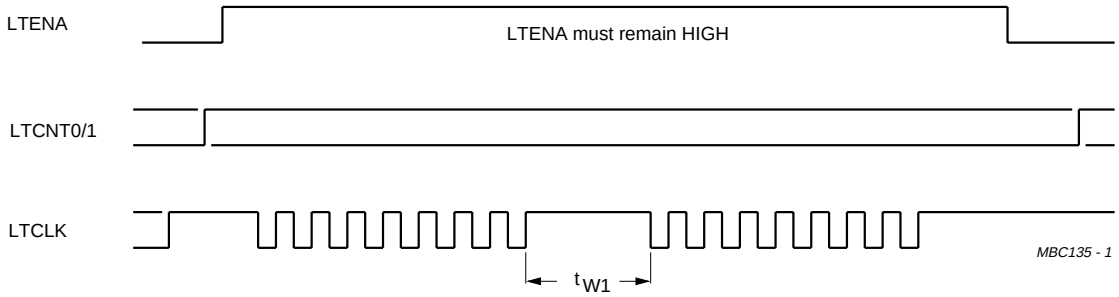
Table 11 Frequency examples.

BIT RATE	F_S	SUB-BANDS SET TO 0	@ FREQUENCY
256 kbit/s	48 kHz	29, 30, 31	> 21750 Hz
192 kbit/s	48 kHz	20, 21, ... , 30, 31	> 15000
	44.1 kHz	22, 23, ... , 30, 31	> 15159
128 kbit/s	48 kHz	12, 13, ... , 30, 31	> 9000
	44.1 kHz	13, 14, ... , 30, 31	> 8957
	32 kHz	20, 21, ... , 30, 31	>10000



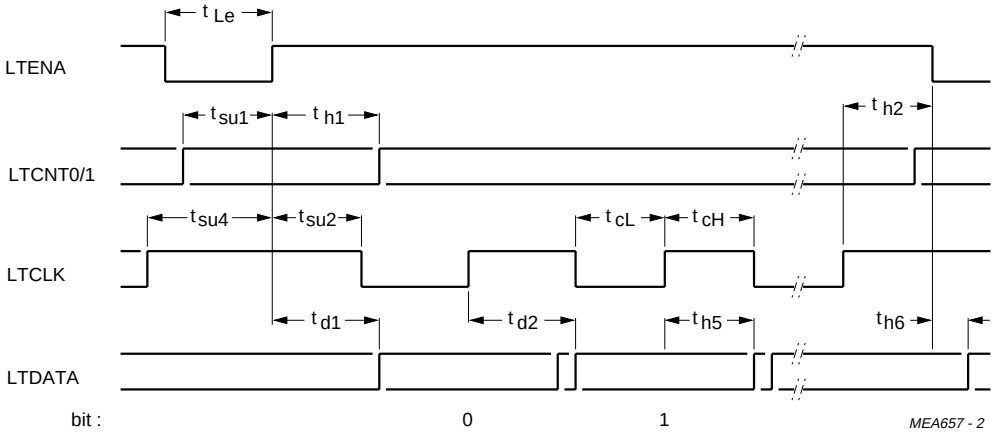
t_{le} > 210 ns minimum LOW time LTENA prior to transfer
t_{s1} > 50 ns set-up time LTCNT0, 1 before LTENA HIGH
t_{h1} > 210 ns hold time LTCNT0, 1 after LTENA HIGH
t_{s2} > 210 ns set-up time LTENA before LTCLK LOW
t_{h2} > 210 ns hold time LTENA after LTCLK HIGH
t_{lc} > 210 ns minimum LOW time LTCLK
t_{hc} > 210 ns minimum HIGH time LTCLK
t_{s3} > 210 ns set-up time LTDATA before LTCLK HIGH
t_{h3} > 50 ns hold time LTDATA after LTCLK HIGH
t_{s4} > 210 ns set-up time LTCLK before LTENA HIGH

Fig.15 Microcontroller to SAA2521 timing.



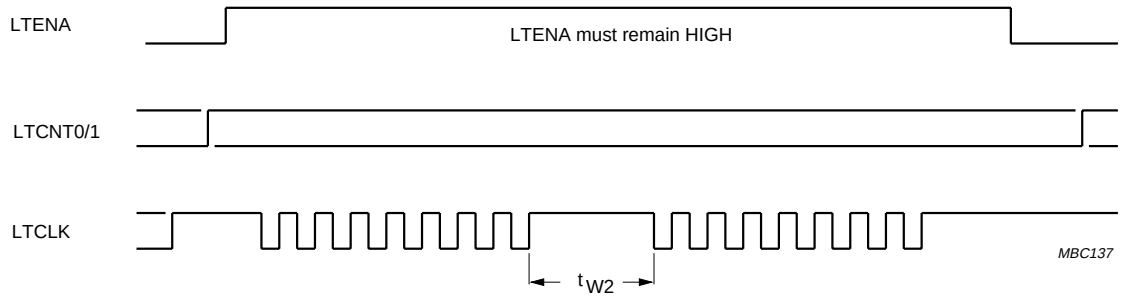
t_{w1} > 550 ns minimum time between two 8-bit transfers

Fig.16 16-bit transfers.



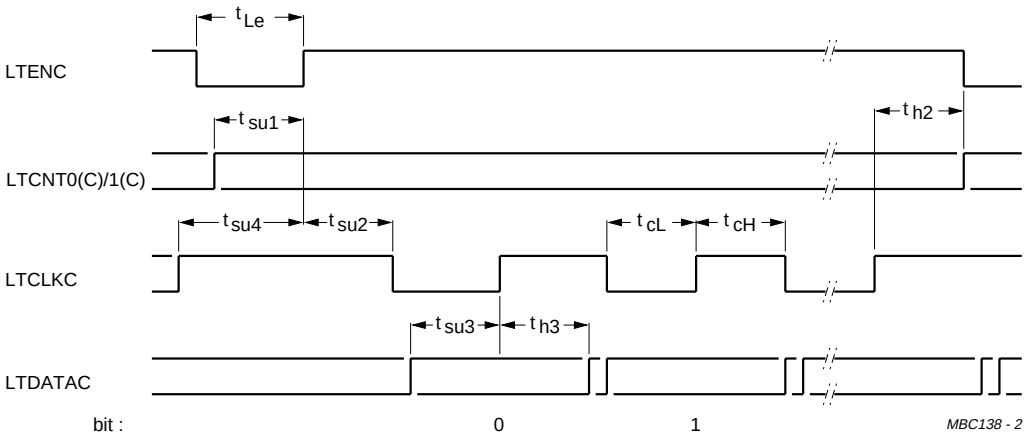
t_{le} > 210 ns minimum LOW time LTENA prior to transfer
t_{s1} > 50 ns set-up time LTCNT0, 1 before LTENA HIGH
t_{h1} > 210 ns hold time LTCNT0, 1 after LTENA HIGH
t_{s2} > 210 ns set-up time LTENA before LTCLK LOW
t_{h2} > 210 ns hold time LTENA after LTCLK HIGH
t_{lc} > 210 ns minimum LOW time LTCLK
t_{hc} > 210 ns minimum HIGH time LTCLK
t_{d1} < 385 ns maximum delay LTDATA after LTENA HIGH
t_{d2} < 385 ns maximum delay LTDATA after LTCLK HIGH
t_{h5} > 145 ns hold time LTDATA after LTCLK HIGH
t_{S4} > 210 ns set-up time LTCLK before LTENA HIGH
t_{h6} > 0 ns hold time LTDATA after LTENA LOW

Fig.17 SAA2521 to Microcontroller timing.



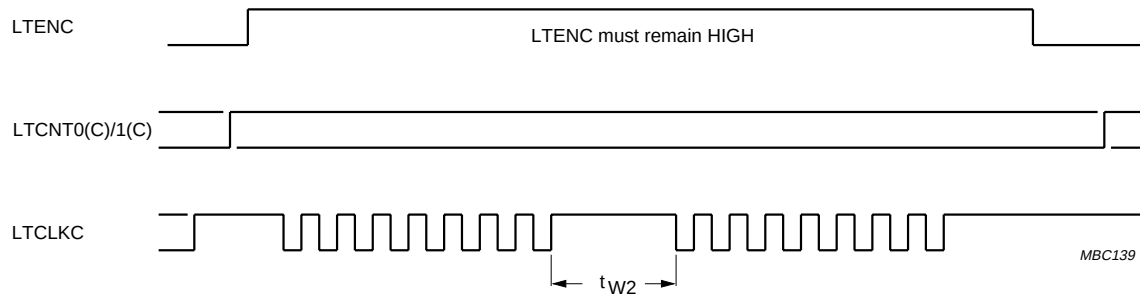
t_{w2} > 550 ns minimum time between two 8-bit transfers

Fig.18 16-bit transfers.



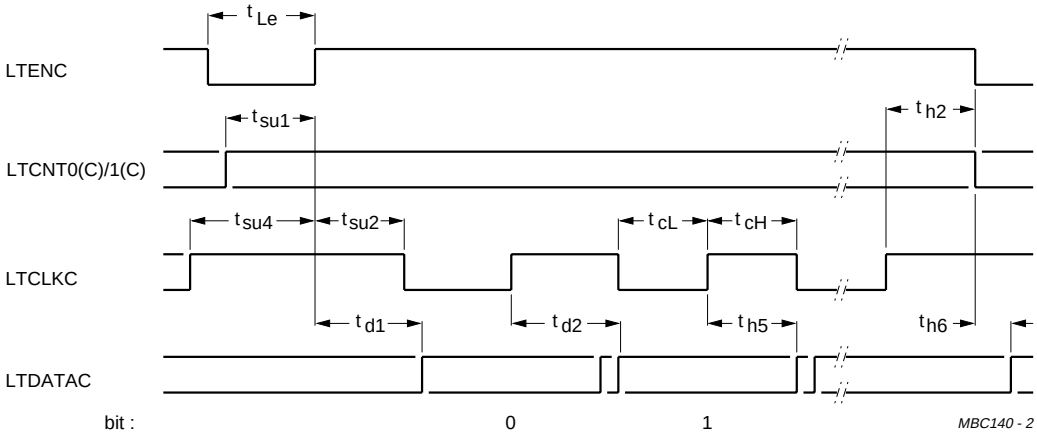
t_{le} > 400 ns minimum LOW time LTENA prior to transfer
t_{s1} > 400 ns set-up time LTCNT0, 1C before LTENC HIGH
t_{s2} > 200 ns set-up time LTENC before LTCLKC LOW
t_{h2} > 400 ns hold time LTENC after LTCLK HIGH
t_{lc} > 210 ns minimum LOW time LTCLKC
t_{hc} > 210 ns minimum HIGH time LTCLKC
t_{s3} > 210 ns set-up time LTDATAC before LTCLKC HIGH
t_{h3} > 160 ns hold time LTDATAC after LTCLKC HIGH
t_{s4} > 900 ns set-up time LTCLKC before LTENC HIGH

Fig.19 SAA2521 to SAA2520 timing.



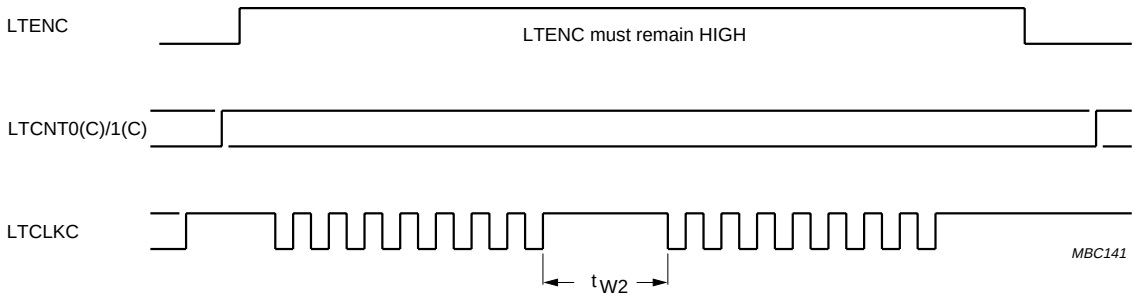
t_{w2} > 600 ns minimum time between two 8-bit transfers

Fig.20 16-bit transfers.



t_{le} > 400 ns minimum LOW time LTENC prior to transfer
t_{s1} > 400 ns set-up time LTCNT0, 1C before LTENC HIGH
t_{s2} > 200 ns set-up time LTENC before LTCLKC LOW
t_{h2} > 400 ns hold time LTENC after LTCLKC HIGH
t_{lc} > 210 ns minimum LOW time LTCLKC
t_{hc} > 210 ns minimum HIGH time LTCLKC
t_{d1} < 300 ns maximum delay LTDATAC after LTENC HIGH
t_{d2} < 300 ns maximum delay LTDATAC after LTCLKC HIGH
t_{s4} > 900 ns set-up time LTCLKC before LTENC HIGH
t_{h5} > 160 ns hold time after LTCLKCC HIGH
t_{h6} > 0 ns hold time LTDATAC after LTENC LOW

Fig.21 SAA2520 to SAA2521 timing.



t_{w1} > 600 ns minimum time between two 8-bit transfers

Fig.22 16-bit transfers.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	6.5	V
V_I	input voltage (note 1)	–0.5	V_{DD} + 0.5	V
I_{DD}	supply current	–	100	mA
I_I	input current	–	± 10	mA
I_o	output current	–	± 40	mA
P_{tot}	total power dissipation	–	550	mW
T_{stg}	storage temperature	–55	+ 150	°C
T_{amb}	operating ambient temperature	–40	+ 85	°C
V_{es1}	electrostatic handling (note 2)	–1500	1500	V
V_{es2}	electrostatic handling (note 3)	–70	70	V

Notes

1. Input voltage should not exceed 6.5 V unless otherwise specified.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

DC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.8	5	5.5	V
I_{DD}	operating current	V_{DD} = 3.8 V	–	15	30	mA
I_{DD}	operating current	V_{DD} = 5 V	–	25	50	mA
I_{PWRDWN}	stand-by current	in power-down mode	–	100	–	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD}	V
I_I	input current		–	–	10	µA
Outputs						
V_{OL}	LOW level output voltage	note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	note 1	V_{DD} – 0.5	–	–	V
3-state outputs						
I_{oz}	OFF state current	V_i = 0 to 5.5 V	–	–	10	µA

Note

1. Maximum load current for LTDATA, LTCNT1C, LTCNT0C, LTENC, LTCLKC, TEST1, TEST2, FDAC, FDAF = 2 mA; for LTDATAC = 3 mA.

AC CHARACTERISTICS

V_{DD} = 3.8 to 5.5 V; T_{amb} = –40 to 85 °C.

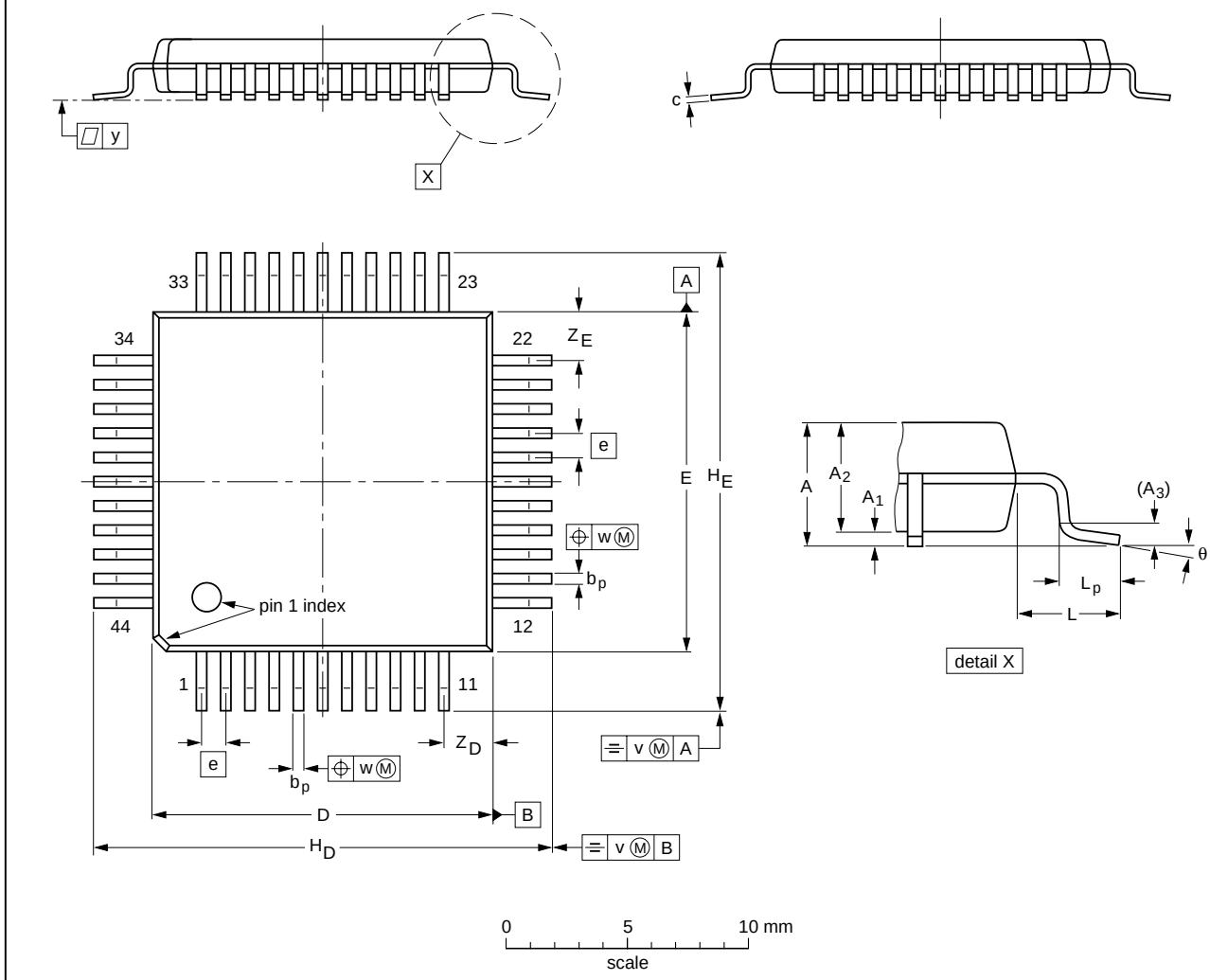
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLOCK CLK24						
f_s	frequency		23	24.576	26	MHz
CLOCK F_s256						
f_s	frequency	f_s = 48 kHz	–	–	13	MHz
Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA, LTDATAC, FDAF, FDAC, SCL, SWS						
C_I	input capacitance		–	–	10	pF
INPUT SET-UP TIME						
t_{SU}	set-up time of inputs related to CLK24 rising edge	note 1	15	–	–	ns
t_{SU}	set-up time of inputs related to $256f_s$ rising edge	note 2	15	–	–	ns
INPUT HOLD TIME						
t_{HD}	hold time of inputs related to CLK24 rising edge	note 1	20	–	–	ns
t_{HD}	hold time of inputs related to $256f_s$ rising edge	note 2	10	–	–	ns
Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC, LTCLKC, FDAF, FDAC						
C_o	output capacitance		–	–	10	pF
t_d	output delay time related to CLK24 rising edge	C_L = 25 pF; note 3	–	–	45	ns
t_d	output delay time related to $256f_s$ rising edge	C_L = 25 pF; note 4	–	–	30	ns
3-state outputs						
t_{PHZ}	disable time HIGH-to-Z	C_L = 25 pF	–	–	65	ns
t_{PLZ}	disable time LOW-to-Z	C_L = 25 pF	–	–	65	ns
t_{PZH}	enable time Z-to-HIGH	C_L = 25 pF	–	–	65	ns
t_{PZL}	enable time Z-to-LOW	C_L = 25 pF	–	–	65	ns

Notes

1. Inputs FSYNC, SWS, LTCNT1, LTCNT0, LTENA, LTCLK, LTDATA, LTDATAC
2. Inputs FDAF, FDAC, SCL, SWS
3. Outputs LTDATA, LTDATAC, LTCNT1C, LTCNT0C, LTENC, LTCLK
4. Outputs FDAF, FDAC

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.