

PowerMOS transistor
Logic level TOPFET

BUK101-50DL

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 3 pin plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving

- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Lower operating input current permits direct drive by micro-controller
- ESD protection on input pin
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	26	A
P_D	Total power dissipation	75	W
T_j	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	60	mΩ
I_{ISL}	Input supply current $V_{IS} = 5\text{ V}$	650	μA

FUNCTIONAL BLOCK DIAGRAM

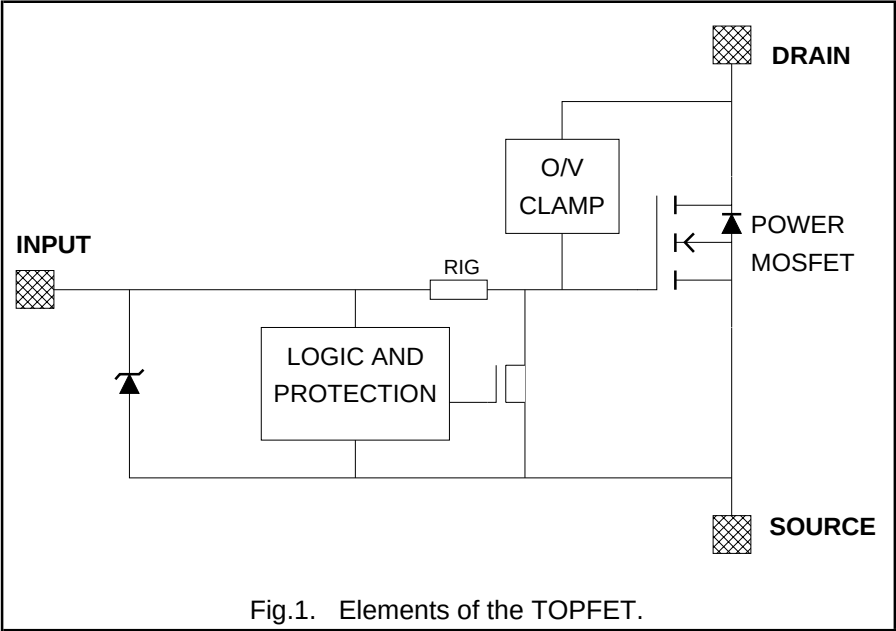
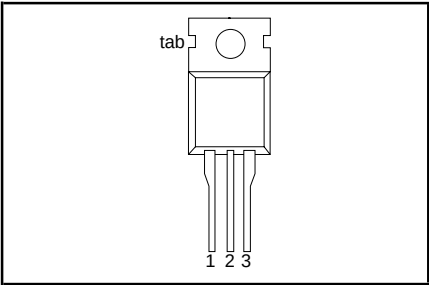


Fig.1. Elements of the TOPFET.

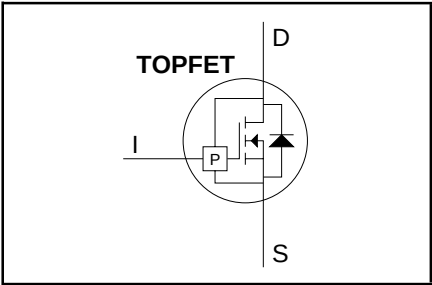
PINNING - TO220AB

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



PowerMOS transistor

Logic level TOPFET

BUK101-50DL

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Continuous drain source voltage ¹	-	-	50	V
V_{IS}	Continuous input voltage	-	0	6	V
I_D	Continuous drain current	$T_{mb} \leq 25\text{ }^{\circ}\text{C}; V_{IS} = 5\text{ V}$	-	26	A
I_D	Continuous drain current	$T_{mb} \leq 100\text{ }^{\circ}\text{C}; V_{IS} = 5\text{ V}$	-	16	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25\text{ }^{\circ}\text{C}; V_{IS} = 5\text{ V}$	-	100	A
P_D	Total power dissipation	$T_{mb} \leq 25\text{ }^{\circ}\text{C}$	-	75	W
T_{stg}	Storage temperature	-	-55	150	$^{\circ}\text{C}$
T_j	Continuous junction temperature ²	normal operation	-	150	$^{\circ}\text{C}$
T_{sold}	Lead temperature	during soldering	-	250	$^{\circ}\text{C}$

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from two types of overload.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{ISP}	Protection supply voltage ³	for valid protection	4	-	V
	Over temperature protection				
$V_{DDP(T)}$	Protected drain source supply voltage	$V_{IS} = 5\text{ V}$	-	50	V
	Short circuit load protection⁴				
$V_{DDP(P)}$	Protected drain source supply voltage ⁵	$V_{IS} = 5\text{ V}$	-	20	V
P_{DSM}	Instantaneous overload dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	1.3	kW

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DROM}	Repetitive peak clamping current	$V_{IS} = 0\text{ V}$	-	26	A
E_{DSM}	Non-repetitive clamping energy	$T_{mb} \leq 25\text{ }^{\circ}\text{C}; I_{DM} = 26\text{ A};$ $V_{DD} \leq 20\text{ V};$ inductive load	-	625	mJ
E_{DRM}	Repetitive clamping energy	$T_{mb} \leq 95\text{ }^{\circ}\text{C}; I_{DM} = 8\text{ A};$ $V_{DD} \leq 20\text{ V}; f = 250\text{ Hz}$	-	40	mJ

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; $C = 250\text{ pF}; R = 1.5\text{ k}\Omega$	-	2	kV

¹ Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

² A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

³ The input voltage for which the overload protection circuits are functional.

⁴ For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

⁵ The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM} , which is always the case when V_{DS} is less than $V_{DDP(P)}$ maximum.

PowerMOS transistor

Logic level TOPFET

BUK101-50DL

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance Junction to mounting base	-	-	1.3	1.67	K/W
$R_{th\ j-a}$	Junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\text{ V}$; $I_D = 10\text{ mA}$	50	-	-	V
$V_{(CL)DSS}$	Drain-source clamping voltage	$V_{IS} = 0\text{ V}$; $I_{DM} = 2\text{ A}$; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$	-	-	70	V
I_{DSS}	Zero input voltage drain current	$V_{DS} = 12\text{ V}$; $V_{IS} = 0\text{ V}$	-	0.5	10	μA
I_{DSS}	Zero input voltage drain current	$V_{DS} = 50\text{ V}$; $V_{IS} = 0\text{ V}$	-	1	20	μA
I_{DSS}	Zero input voltage drain current	$V_{DS} = 40\text{ V}$; $V_{IS} = 0\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$	-	10	100	μA
$R_{DS(ON)}$	Drain-source on-state resistance ¹	$V_{IS} = 5\text{ V}$; $I_{DM} = 13\text{ A}$; $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$	-	45	60	m Ω

OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off when one of the overload thresholds is reached. It remains latched off until reset by the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$E_{DS(TO)}$	Short circuit load protection² Overload threshold energy	$T_{mb} = 25\text{ }^{\circ}\text{C}$; $L \leq 10\text{ }\mu\text{H}$; $R_L = 10\text{ m}\Omega$ $V_{DD} = 13\text{ V}$; $V_{IS} = 5\text{ V}$	-	0.4	-	J
$t_{d\ sc}$	Response time	$V_{DD} = 13\text{ V}$; $V_{IS} = 5\text{ V}$	-	0.8	-	ms
$I_{D(SC)}$	Drain current ³	$V_{DD} = 13\text{ V}$; $V_{IS} = 5\text{ V}$	-	45	-	A
$I_{DM(SC)}$	Peak drain current ⁴	$V_{IS} = 5\text{ V}$; $V_{DD} = 13\text{ V}$	-	105	-	A
$T_{j(TO)}$	Over temperature protection Threshold junction temperature	$V_{IS} = 5\text{ V}$; from $I_D \geq 1\text{ A}$ ⁵	150	-	-	$^{\circ}\text{C}$

TRANSFER CHARACTERISTIC

 $T_{mb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 10\text{ V}$; $I_{DM} = 13\text{ A}$ $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.01$	10	16	-	S

¹ Continuous input voltage. The specified pulse width is for the drain current.

² Refer to OVERLOAD PROTECTION LIMITING VALUES.

³ Continuous drain-source supply voltage. Pulsed input voltage.

⁴ Continuous input voltage. Momentary short circuit load connection. (The higher peak current is due to the effect of capacitance Cgd).

⁵ The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

PowerMOS transistor Logic level TOPFET

BUK101-50DL

INPUT CHARACTERISTICS

$T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified. The supply for the logic and overload protection is taken from the input.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{IS(TO)}$	Input threshold voltage	$V_{DS} = 5\text{ V}$; $I_D = 1\text{ mA}$	1.0	1.5	2.0	V
I_{IS}	Input supply current	normal operation; $V_{IS} = 5\text{ V}$	100	200	350	μA
		$V_{IS} = 4\text{ V}$	-	160	270	μA
V_{ISR}	Protection reset voltage ¹	$T_j = 25\text{ }^{\circ}\text{C}$	2.0	2.6	3.5	V
		$T_j = 150\text{ }^{\circ}\text{C}$	1.0	-	-	
I_{ISL}	Input supply current	protection latched; $V_{IS} = 5\text{ V}$	-	330	650	μA
		$V_{IS} = 3.5\text{ V}$	-	240	430	μA
$V_{(BR)IS}$	Input breakdown voltage	$I_I = 10\text{ mA}$	6	-	-	V
R_{IG}	Input series resistance to gate of power MOSFET	$T_j = 25\text{ }^{\circ}\text{C}$	-	33	-	$\text{k}\Omega$
		$T_j = 150\text{ }^{\circ}\text{C}$	-	50	-	$\text{k}\Omega$

SWITCHING CHARACTERISTICS

$T_{mb} = 25\text{ }^{\circ}\text{C}$. $R_I = 50\text{ }\Omega$. Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{don}	Turn-on delay time	$V_{DD} = 13\text{ V}$; $V_{IS} = 5\text{ V}$	-	17	-	μs
t_r	Rise time	resistive load $R_L = 2.1\text{ }\Omega$	-	75	-	μs
t_{doff}	Turn-off delay time	$V_{DD} = 13\text{ V}$; $V_{IS} = 0\text{ V}$	-	60	-	μs
t_f	Fall time	resistive load $R_L = 2.1\text{ }\Omega$	-	70	-	μs

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	$T_{mb} \leq 25\text{ }^{\circ}\text{C}$; $V_{IS} = 0\text{ V}$	-	26	A

REVERSE DIODE CHARACTERISTICS

$T_{mb} = 25\text{ }^{\circ}\text{C}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDO}	Forward voltage	$I_S = 26\text{ A}$; $V_{IS} = 0\text{ V}$; $t_p = 300\text{ }\mu\text{s}$	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable ²	-	-	-	-

¹ The input voltage below which the overload protection circuits will be reset.

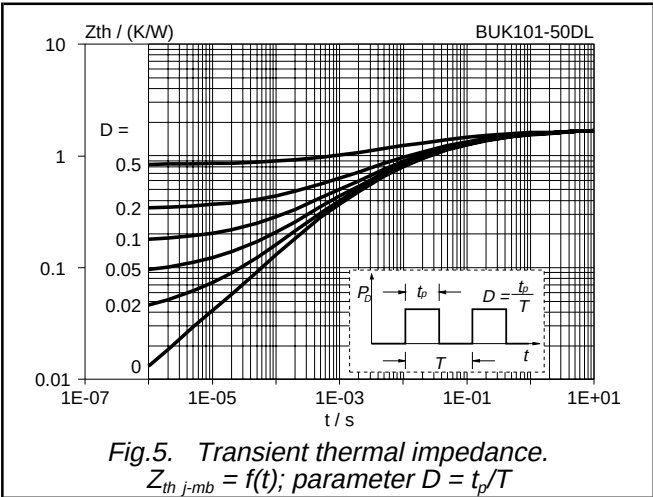
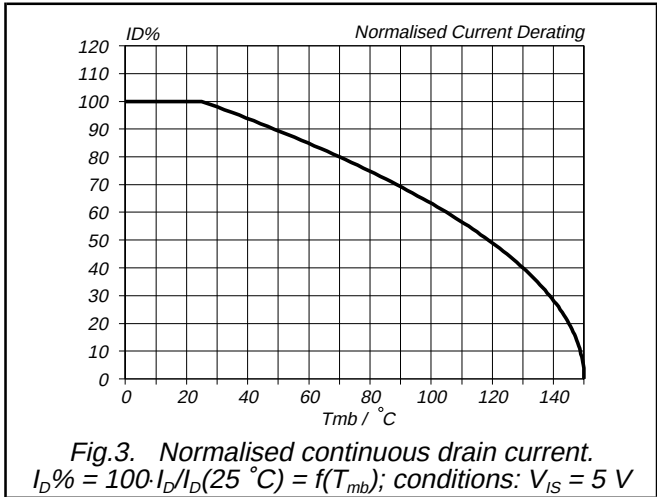
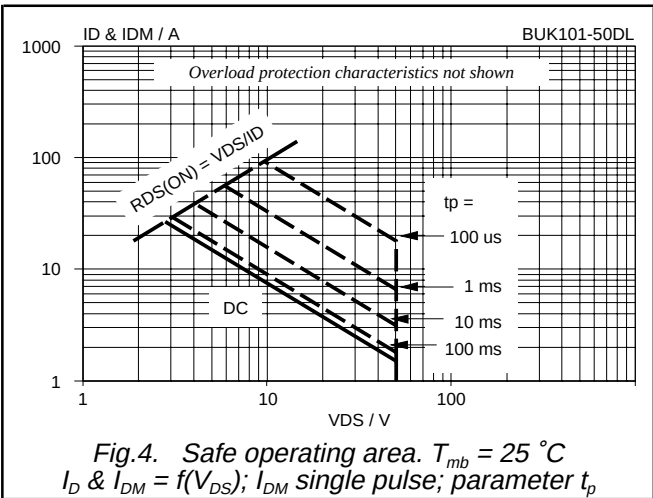
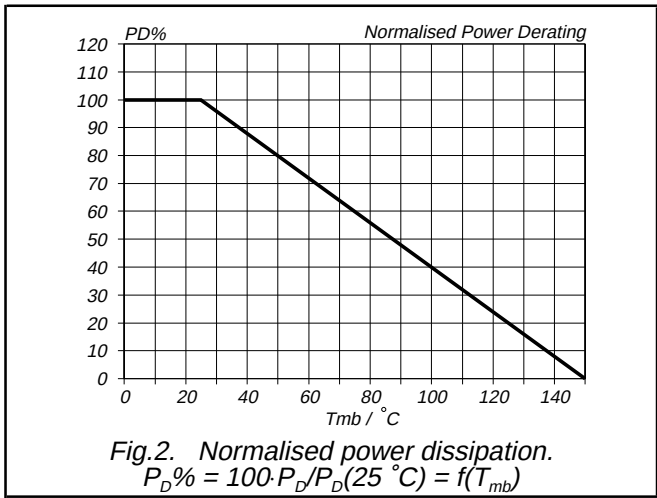
² The reverse diode of this type is not intended for applications requiring fast reverse recovery.

PowerMOS transistor
Logic level TOPFET

BUK101-50DL

ENVELOPE CHARACTERISTICS

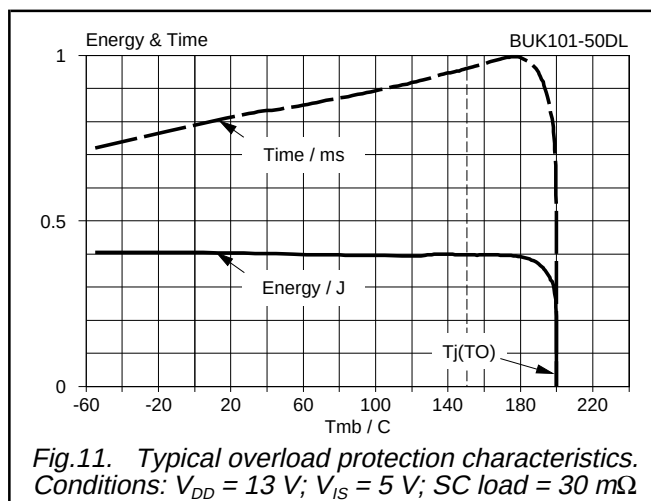
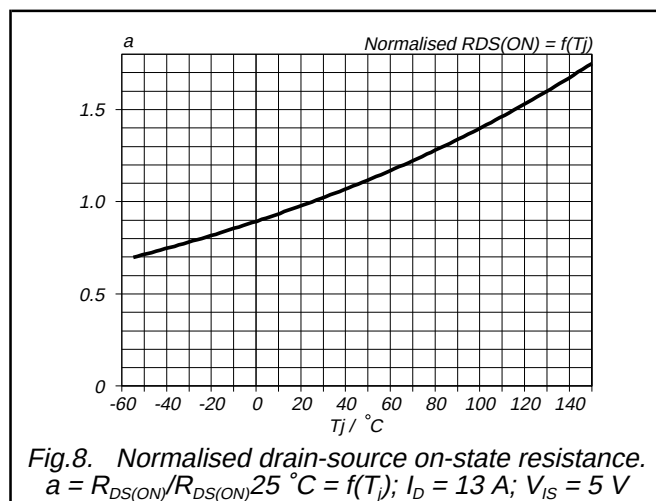
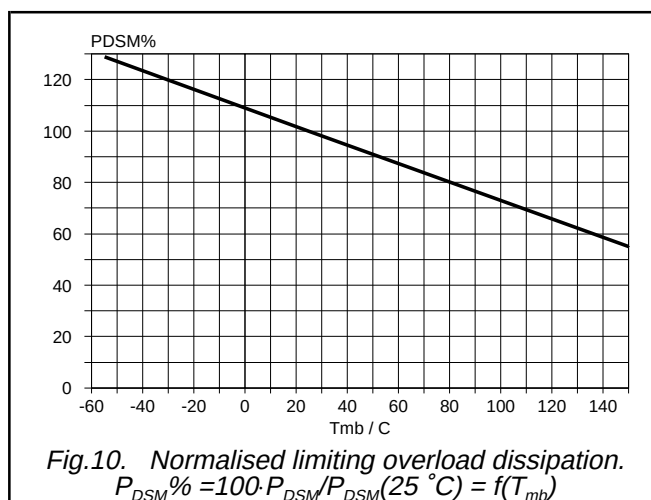
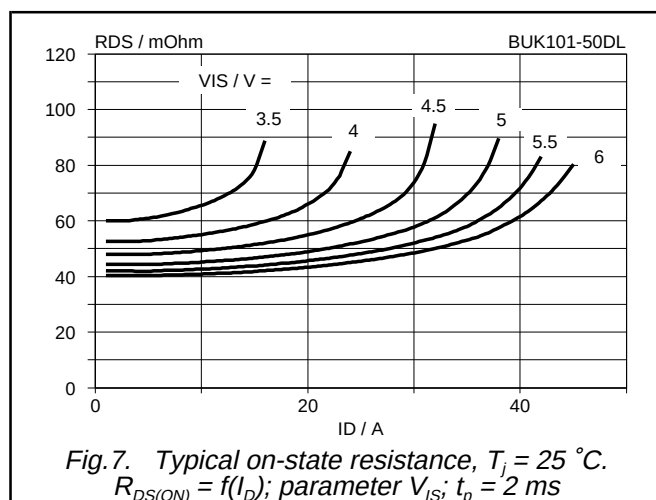
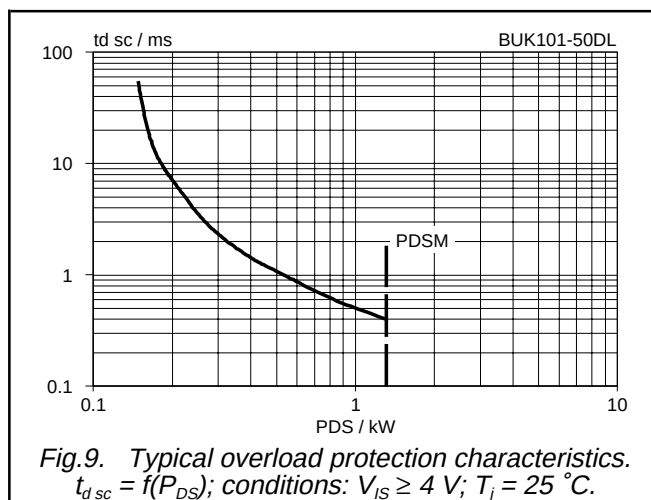
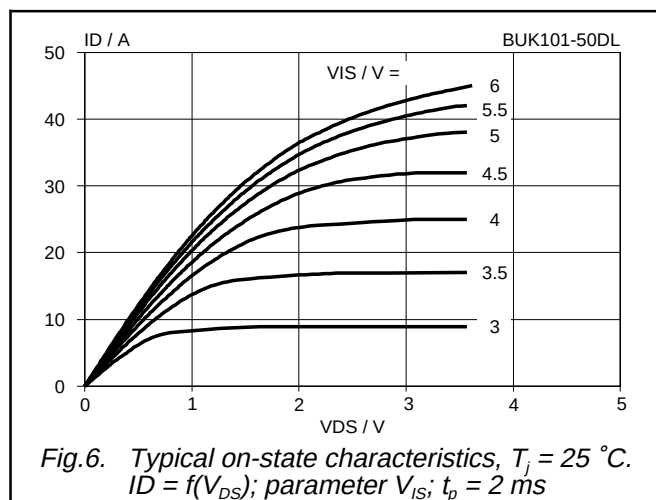
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH



PowerMOS transistor

Logic level TOPFET

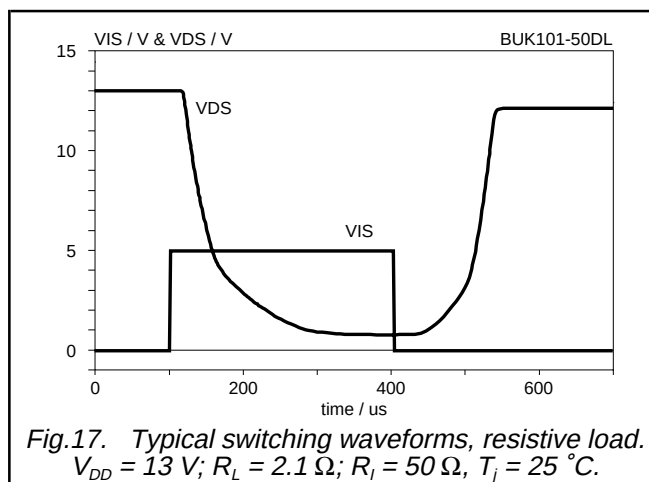
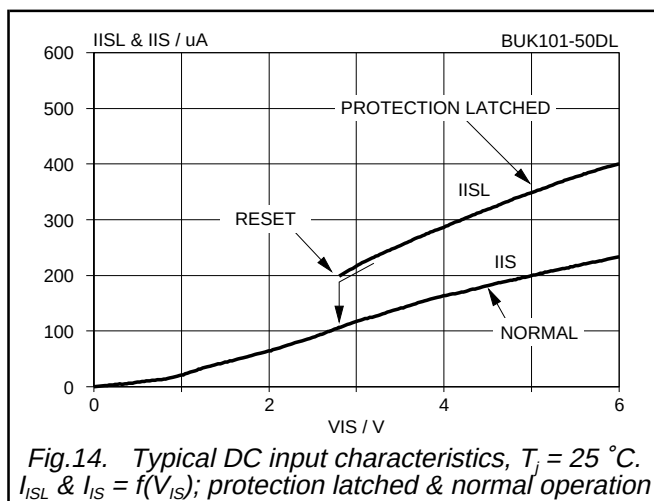
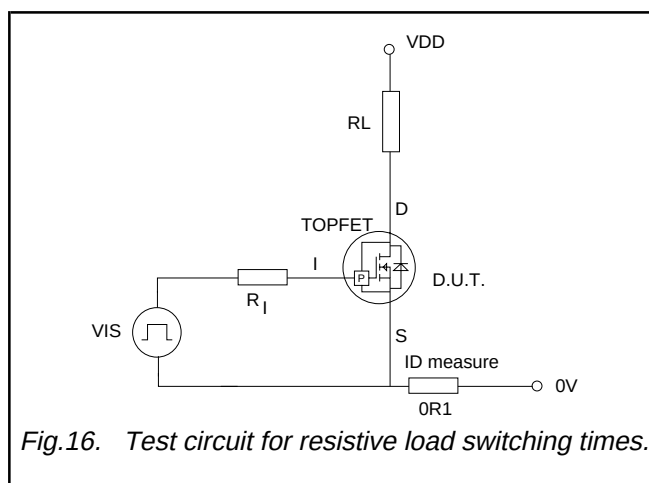
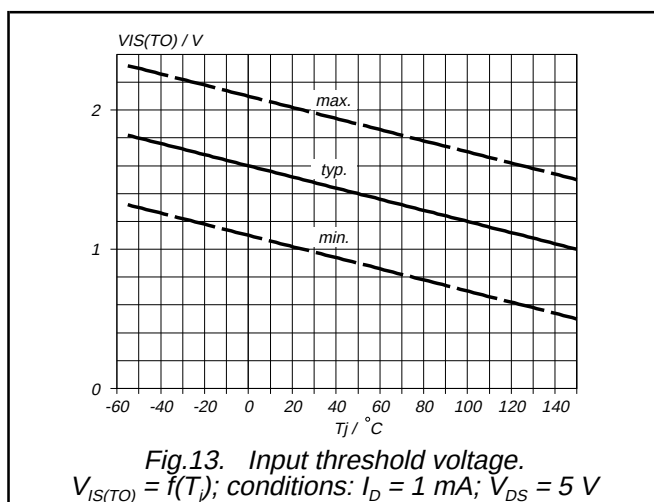
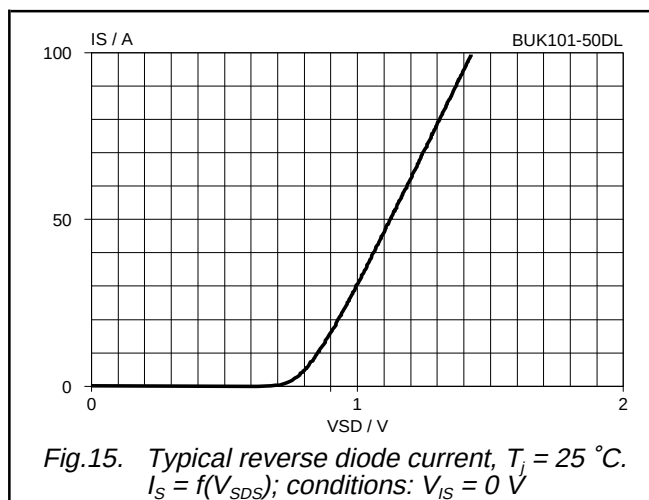
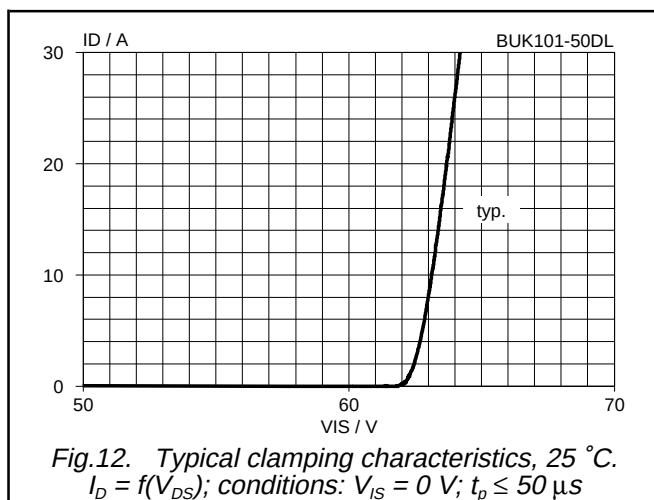
BUK101-50DL



PowerMOS transistor

Logic level TOPFET

BUK101-50DL



PowerMOS transistor

Logic level TOPFET

BUK101-50DL

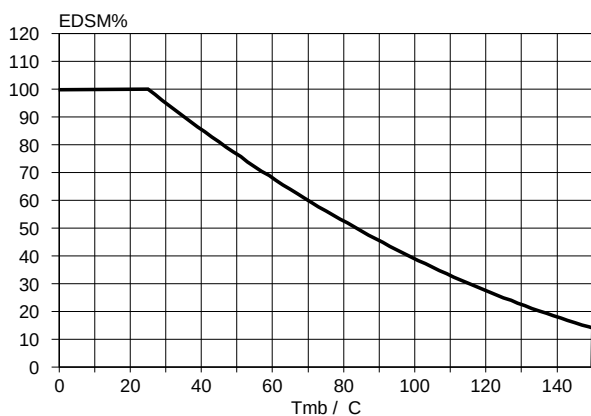


Fig.18. Normalised clamping energy rating.
 $E_{DSM}\% = f(T_{mb})$; conditions: $I_D = 26\text{ A}$; $V_{IS} = 5\text{ V}$

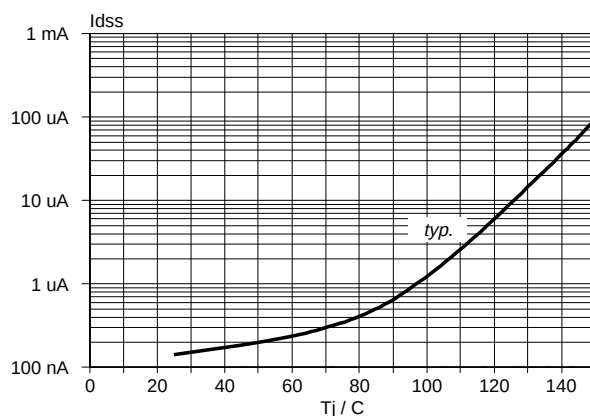


Fig.20. Typical off-state leakage current.
 $I_{DSS} = f(T_j)$; Conditions: $V_{DS} = 40\text{ V}$; $I_{IS} = 0\text{ V}$.

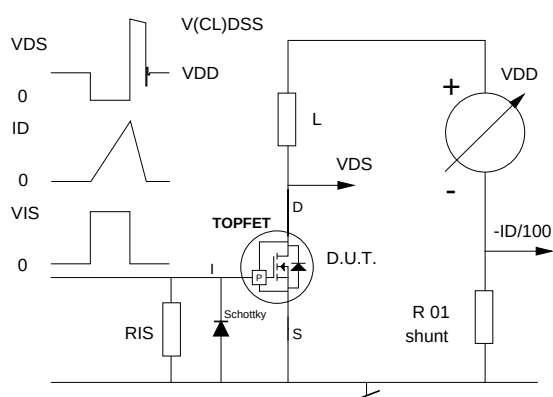


Fig.19. Clamping energy test circuit, $R_{IS} = 50\ \Omega$.
 $E_{DSM} = 0.5 \cdot L I_D^2 \cdot V_{(CL)DSS} / (V_{(CL)DSS} - V_{DD})$

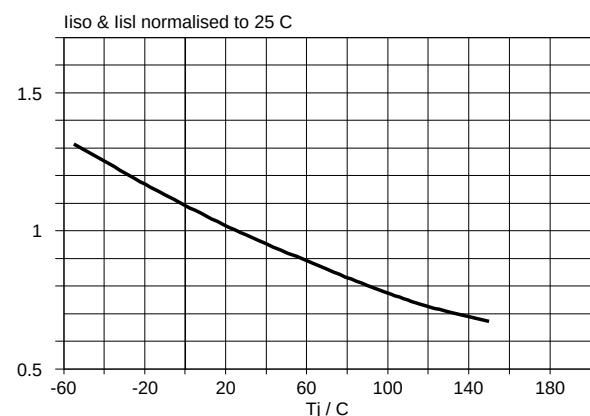


Fig.21. Normalised input currents (normal & latched).
 $I_{ISO}/I_{ISO\ 25^\circ\text{C}}$ & $I_{ISL}/I_{ISL\ 25^\circ\text{C}} = f(T_j)$; $V_{IS} = 5\text{ V}$

PowerMOS transistor

Logic level TOPFET

BUK101-50DL

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

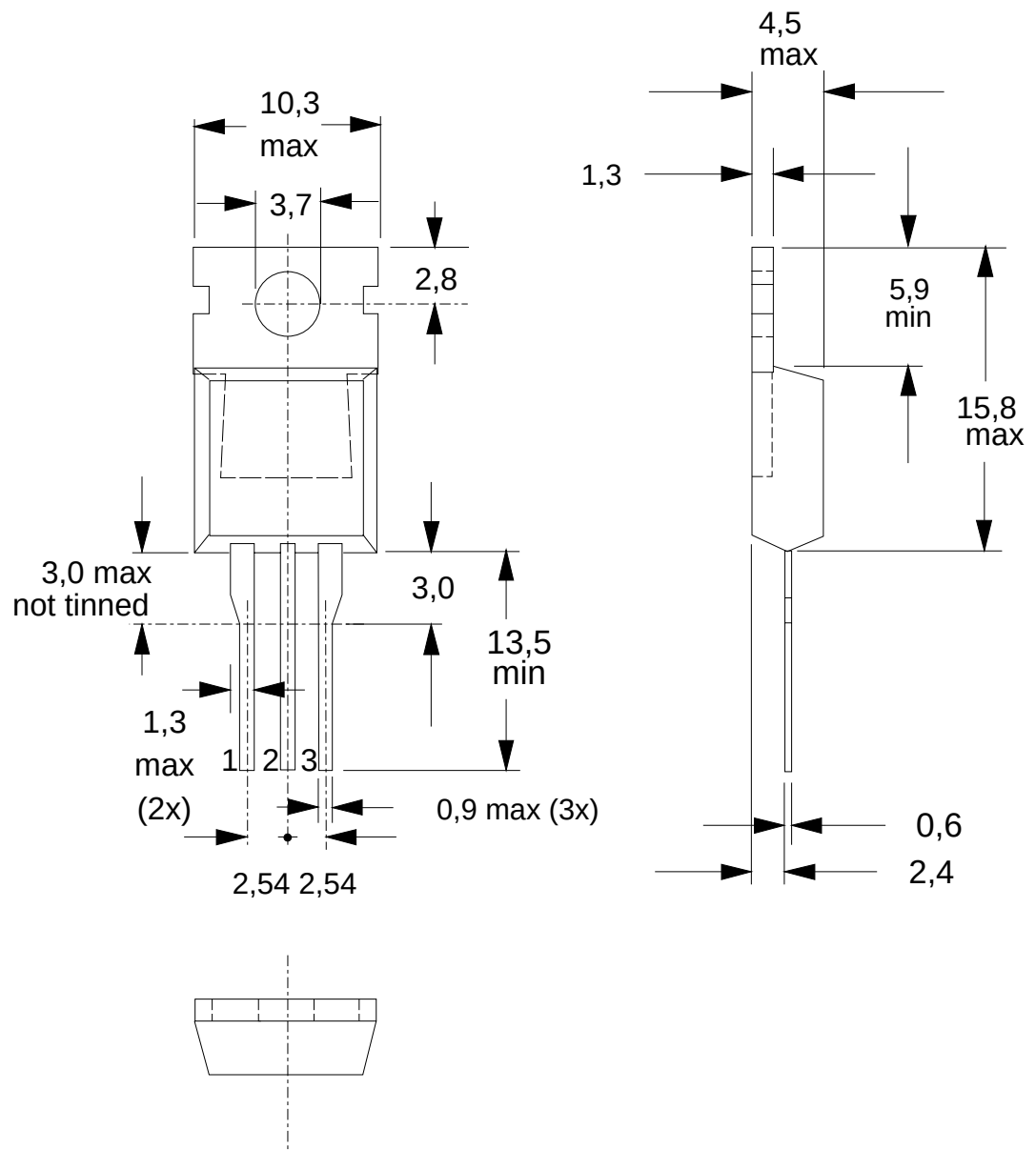


Fig.22. TO220AB; pin 2 connected to mounting base.

Notes

1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

PowerMOS transistor
Logic level TOPFET

BUK101-50DL

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1996	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.