

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT594

8-bit shift register with output register

Product specification
File under Integrated Circuits, IC06

December 1991

8-bit shift register with output register

74HC/HCT594

FEATURES

- Synchronous serial input and output
- 8-bit parallel output
- Shift and storage register have independent direct clear and clocks
- 100 MHz (typ.)
- Output capability:
 - parallel outputs: bus driver
 - serial outputs: standard
- I_{CC} category: MSI

APPLICATIONS

- Serial-to parallel data conversion
- Remote control holding register

DESCRIPTION

The 74HC/HCT594 are high-speed, Si-gate CMOS devices, and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74HC/HCT594 contain an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided on both the shift and storage registers. A serial output (Q_7') is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 250\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay SH_{CP} to Q_7'	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	13	15	ns
	ST_{CP} to Q_n		13	15	ns
	$\overline{SH}_R$ to Q_n		11	14	ns
	$\overline{ST}_R$ to Q_n		11	14	ns
f_{max}	maximum clock frequency SH_{CP} , ST_{CP}		100	100	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	84	89	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$, where:
 f_i = input frequency in MHz; f_o = output frequency in MHz;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs;
 C_L = output load capacitance in pF; V_{CC} = supply voltage in V.
2. For HC, the condition is $V_I = \text{GND to } V_{CC}$; for HCT, the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$.

ORDERING INFORMATION

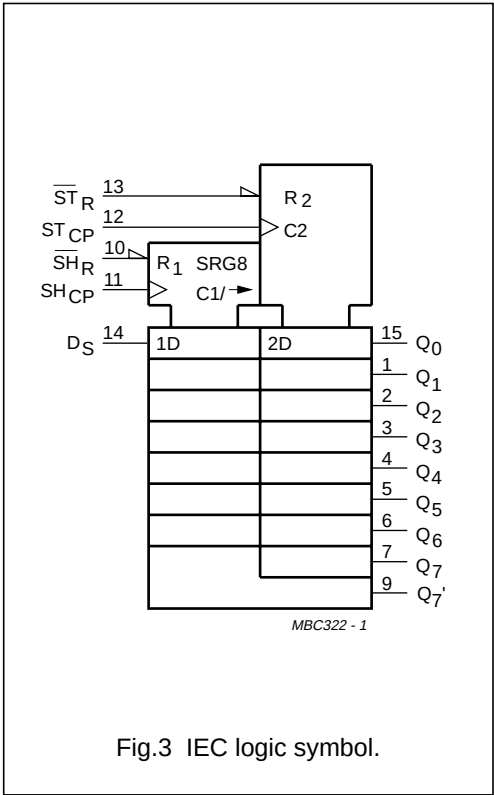
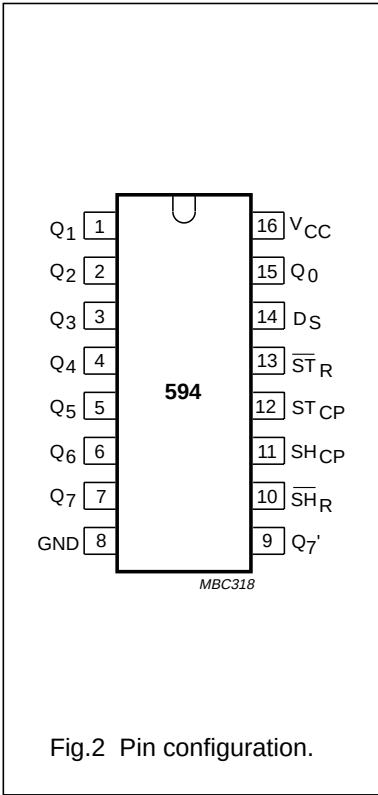
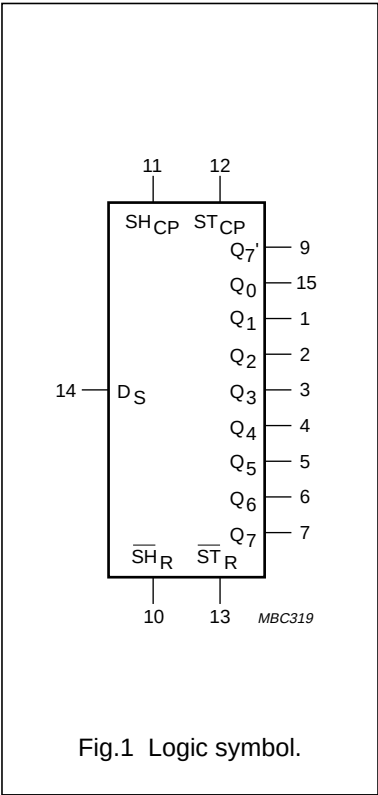
EXTENDED TYPE NUMBER	PACKAGES			
	PINS	PIN POSITION	MATERIAL	CODE
PC74HC/HCT594P	16	DIL	plastic	SOT38C, P
PC74HC/HCT594T	16	SO	plastic	SOT109A

8-bit shift register with output register

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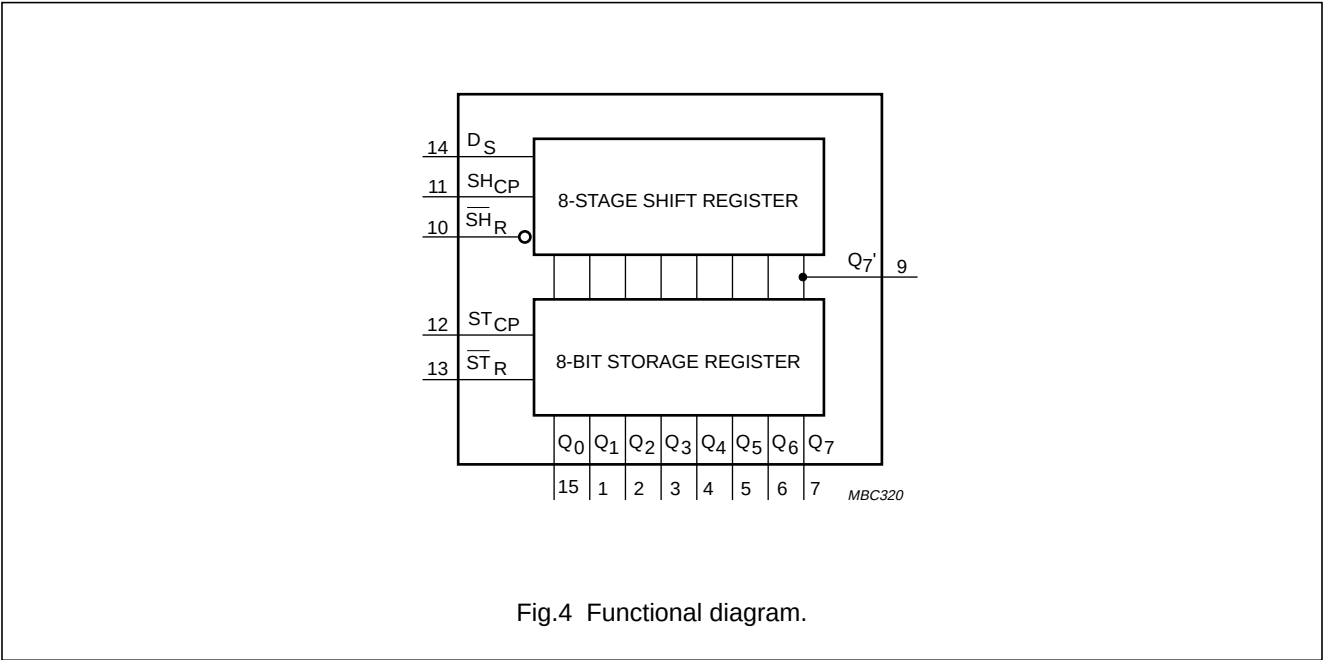
PINNING

SYMBOL	PIN	DESCRIPTION
Q ₀ to Q ₇	15 & 1 to 7	parallel data outputs
GND	8	ground (0 V)
Q ₇ '	9	serial data output
$\overline{\text{SH}}_{\text{R}}$	10	shift register reset (active LOW)
SH _{CP}	11	shift register clock input
ST _{CP}	12	storage register clock input
$\overline{\text{ST}}_{\text{R}}$	13	storage register reset active (LOW)
D _s	14	serial data input
V _{CC}	16	supply voltage



8-bit shift register with output register

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FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTION
SH _{CP}	ST _{CP}	SH _R	ST _R	D _S	Q ₇ '	Q _n	
X	X	L	X	X	L	NC	a LOW level on SH _R only affects the shift registers.
X	X	X	L	X	NC	L	a LOW level on ST _R only affects the storage registers.
X	↑	L	H	X	L	L	empty shift register loaded into storage register.
↑	X	H	X	H	Q ₆ '	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q ₆ ') appears on the serial output (Q ₇ ').
X	↑	H	H	X	NC	Q _n '	contents of shift register stages (internal Q _n ') are transferred to the storage register and parallel output stages.
↑	↑	H	H	X	Q _{6n}	Q _n '	contents of shift register shifted through. Previous contents of shift register transferred to the storage register and the parallel output stages.

Note

1.
- H = HIGH voltage level
- L = LOW voltage level
- ↑ = LOW-to-HIGH transition
- NC = no change
- X = don't care.

8-bit shift register with output register

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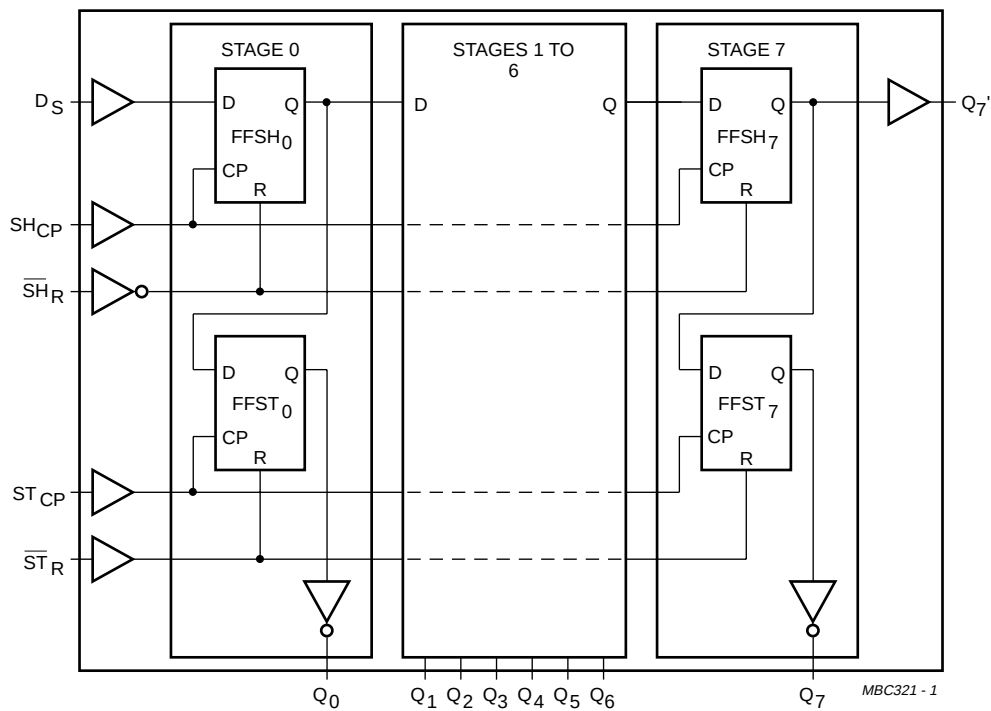


Fig.5 Logic diagram.

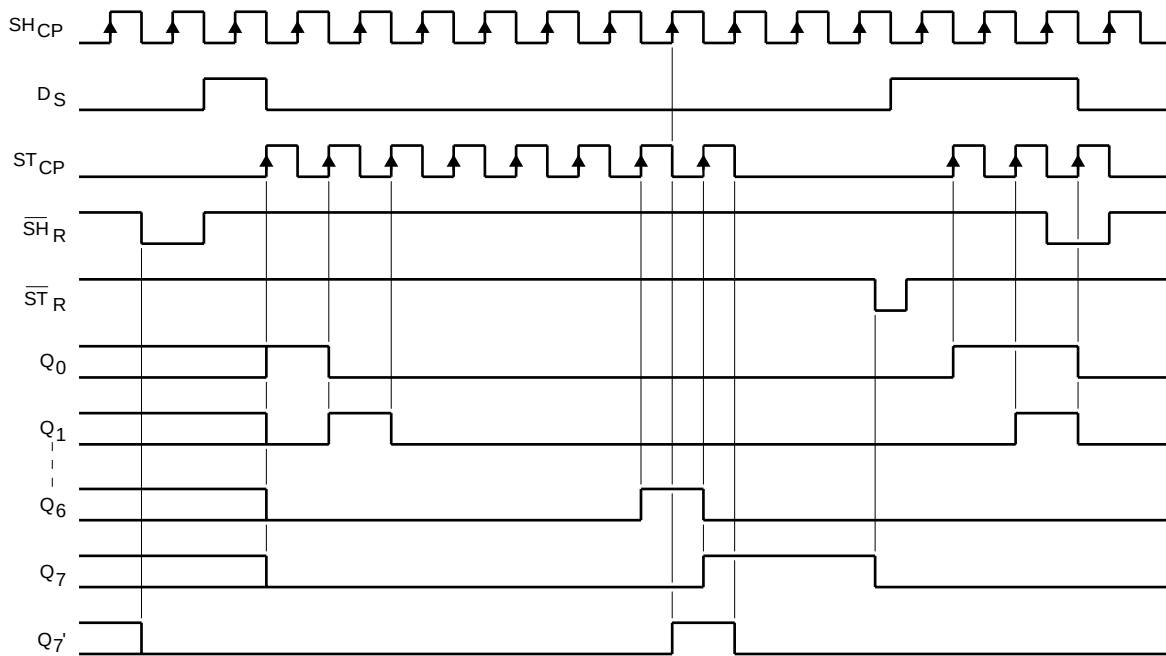


Fig.6 Timing diagram.

8-bit shift register with output register

74HC/HCT594

DC CHARACTERISTICS FOR 74HC

For the DC characteristics, see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard.

I_{CC} category: MSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	—	44	150	—	185	—	225	ns	2.0	Fig.7
		—	16	30	—	37	—	45	ns	4.5	
		—	14	26	—	31	—	38	ns	6.0	
	propagation delay ST _{CP} to Q _n	—	44	150	—	185	—	225	ns	2.0	Fig.8
		—	16	30	—	37	—	45	ns	4.5	
		—	14	26	—	31	—	38	ns	6.0	
t _{PHL}	propagation delay SH _R to Q ₇ '	—	39	150	—	185	—	225	ns	2.0	Fig.11
		—	14	30	—	37	—	45	ns	4.5	
		—	12	26	—	31	—	38	ns	6.0	
	propagation delay ST _R to Q _n	—	39	125	—	155	—	185	ns	2.0	Fig.12
		—	14	25	—	31	—	37	ns	4.5	
		—	12	21	—	26	—	31	ns	6.0	
t _w	shift clock pulse width HIGH or LOW	80	10	—	100	—	120	—	ns	2.0	Fig.7
		16	4	—	20	—	24	—	ns	4.5	
		14	3	—	17	—	20	—	ns	6.0	
	storage clock pulse width HIGH or LOW	80	10	—	100	—	120	—	ns	2.0	Fig.8
		16	4	—	20	—	24	—	ns	4.5	
		14	3	—	17	—	20	—	ns	6.0	
	shift and storage reset pulse width HIGH or LOW	80	14	—	100	—	120	—	ns	2.0	Fig.11 and Fig.12
		16	5	—	20	—	24	—	ns	4.5	
		14	4	—	17	—	20	—	ns	6.0	
t _{su}	set-up time D _s to SH _{CP}	100	10	—	125	—	150	—	ns	2.0	Fig.9
		20	4	—	25	—	30	—	ns	4.5	
		17	3	—	21	—	26	—	ns	6.0	
	set-up time SH _R to ST _{CP}	100	14	—	125	—	150	—	ns	2.0	Fig.10
		20	5	—	25	—	30	—	ns	4.5	
		17	4	—	21	—	26	—	ns	6.0	
	set-up time SH _{CP} to ST _{CP}	100	17	—	125	—	150	—	ns	2.0	Fig.8
		20	6	—	25	—	30	—	ns	4.5	
		17	5	—	21	—	26	—	ns	6.0	

8-bit shift register with output register

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SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _h	hold time D _s to SH _{CP}	25	−8	−	30	−	35	−	ns	2.0	Fig.9
		5	−3	−	6	−	7	−	ns	4.5	
		4	−2	−	5	−	6	−	ns	6.0	
t _{rem}	removal time SH _R to SH _{CP} , ST _R to ST _{CP}	50	−14	−	65	−	75	−	ns	2.0	Fig.11 and Fig.12
		10	−5	−	13	−	15	−	ns	4.5	
		9	−4	−	11	−	13	−	ns	6.0	
f _{max}	maximum clock frequency SH _{CP} or ST _{CP}	6.0	30	−	4.8	−	4.0	−	MHz	2.0	Fig.7 and Fig.8
		30	92	−	24	−	20	−	MHz	4.5	
		35	109	−	28	−	24	−	MHz	6.0	

8-bit shift register with output register

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics, see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: parallel outputs, bus driver; serial output, standard.

I_{CC} category: MSI.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the following table.

INPUT	UNIT LOAD COEFFICIENT
D_s	0.25
$\overline{SH}_R$	1.50
SH_{CP}	1.50
ST_{CP}	1.50
$\overline{ST}_R$	1.50

AC CHARACTERISTICS FOR 74HCT

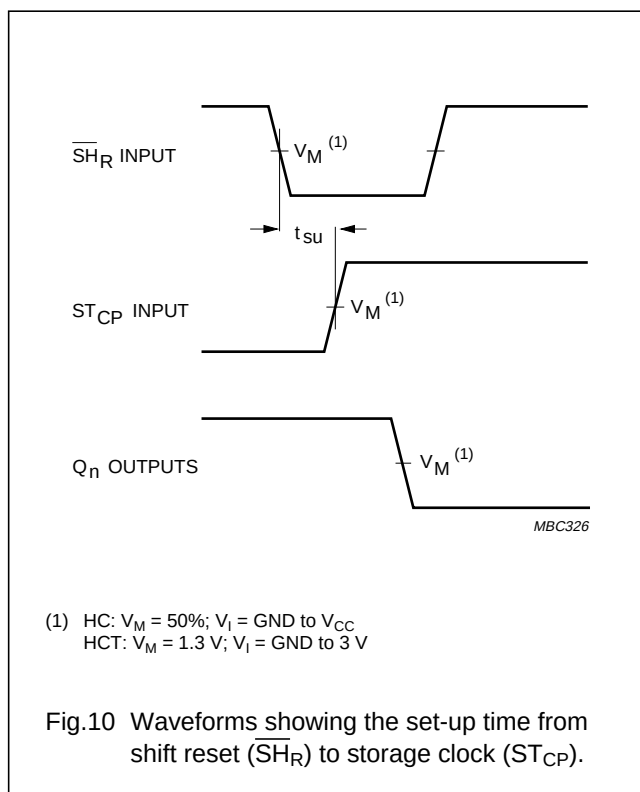
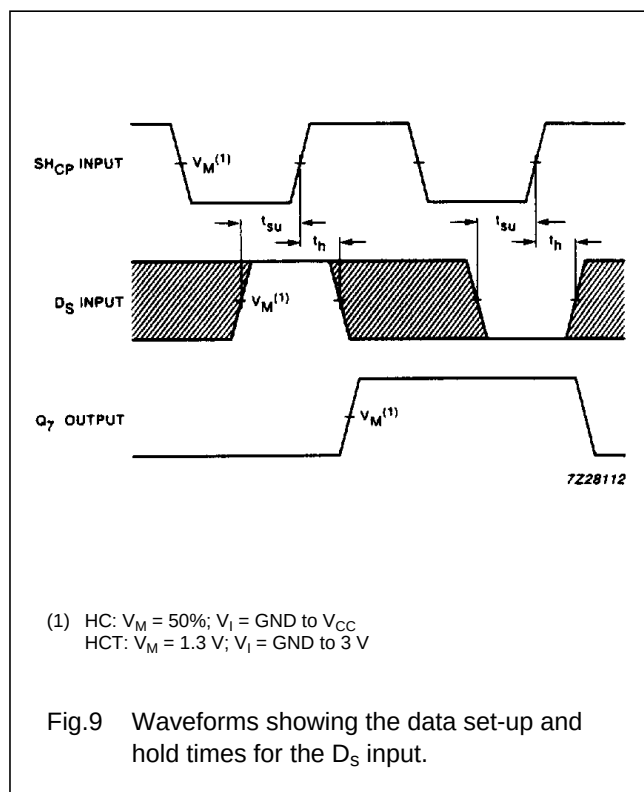
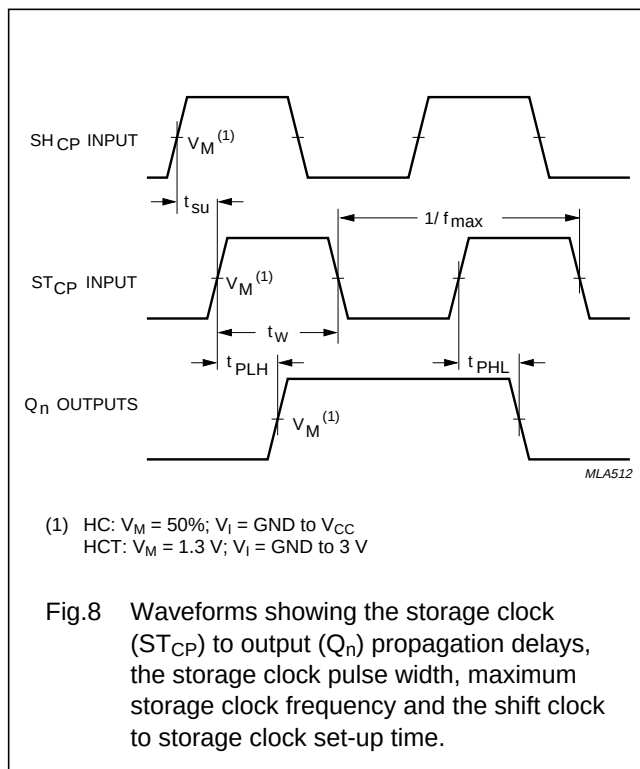
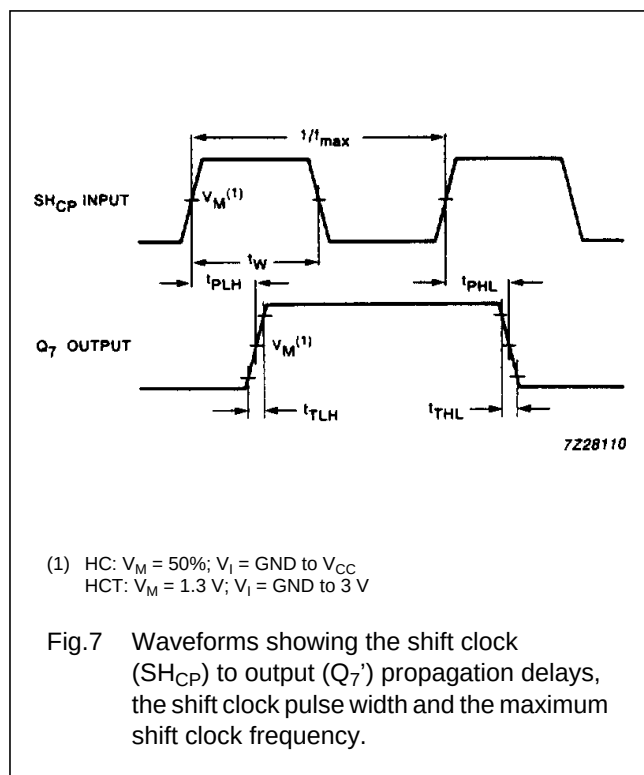
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		+25			−40 to +85		−40 to +125			V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} /t _{PLH}	propagation delay SH _{CP} to Q ₇ '	—	18	32	—	40	—	48	ns	4.5	Fig.7
	propagation delay ST _{CP} to Q _n	—	18	32	—	40	—	48	ns	4.5	Fig.8
t _{PHL}	propagation delay SH _R to Q ₇ '	—	17	30	—	38	—	45	ns	4.5	Fig.11
	propagation delay ST _R to Q _n	—	17	30	—	38	—	45	ns	4.5	Fig.12
t _W	shift clock pulse width HIGH or LOW	16	4	—	20	—	24	—	ns	4.5	Fig.7
	storage clock pulse width HIGH or LOW	16	4	—	20	—	24	—	ns	4.5	Fig.8
	shift and storage reset pulse width HIGH or LOW	16	6	—	20	—	24	—	ns	4.5	Fig.11 and Fig.12
t _{su}	set-up time D _s to SH _{CP}	20	4	—	25	—	30	—	ns	4.5	Fig.9
	set-up time SH _R to ST _{CP}	20	6	—	25	—	30	—	ns	4.5	Fig.10
	set-up time SH _{CP} to ST _{CP}	20	7	—	25	—	30	—	ns	4.5	Fig.8
t _h	hold time D _s to SH _{CP}	5	−3	—	6	—	7	—	ns	4.5	Fig.9
t _{rem}	removal time SH _R to SH _{CP} , ST _R to ST _{CP}	10	−5	—	13	—	15	—	ns	4.5	Fig.11 and Fig.12
f _{max}	maximum clock frequency SH _{CP} or ST _{CP}	30	92	—	24	—	20	—	MHz	4.5	Fig.7 and Fig.8

8-bit shift register with output register

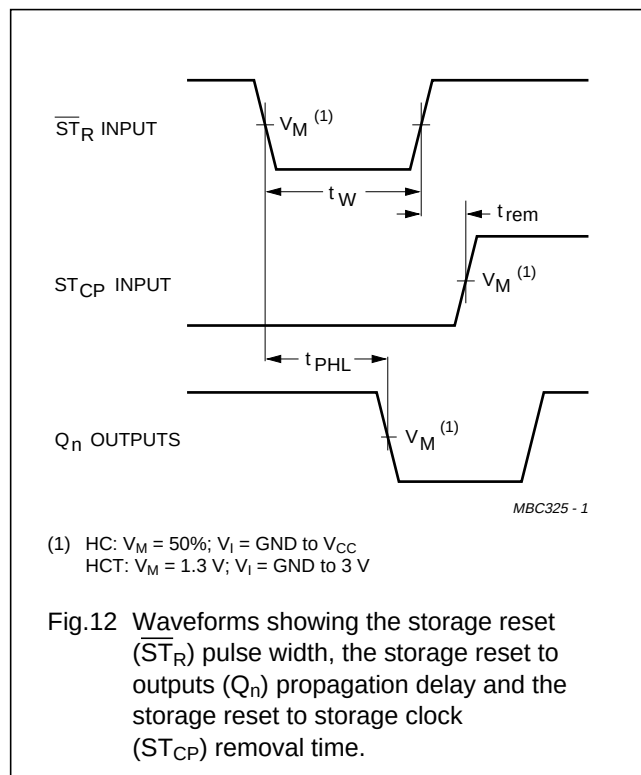
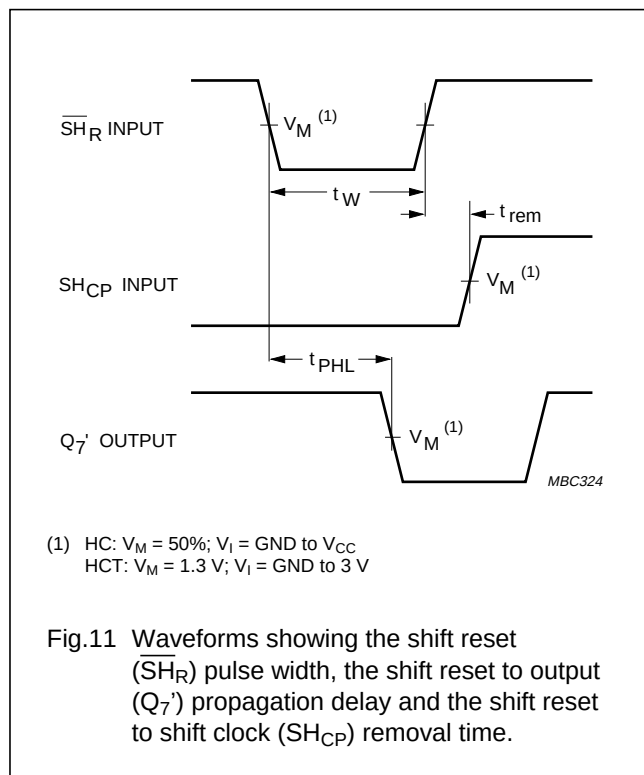
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AC WAVEFORMS



8-bit shift register with output register

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PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".