Peregrine Semiconductor

Preliminary Specification

# PE42660 DIE

**SP6T UltraCMOS™ 2.75 V Switch**
**100 – 3000 MHz**

## Features

- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonics performance: $2f_o$ = -88 dBc and $3f_o$ = -85 dBc
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.65 dB at 1900 MHz
- TX – RX Isolation of 48 dB at 900 MHz, 40 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- 41 dBm P1dB
- No blocking capacitors required

## Product Description

*The PE42660 is a HaRP™-enhanced SP6T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control, while high ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.*

*Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.*

**Figure 1. Functional Diagram**

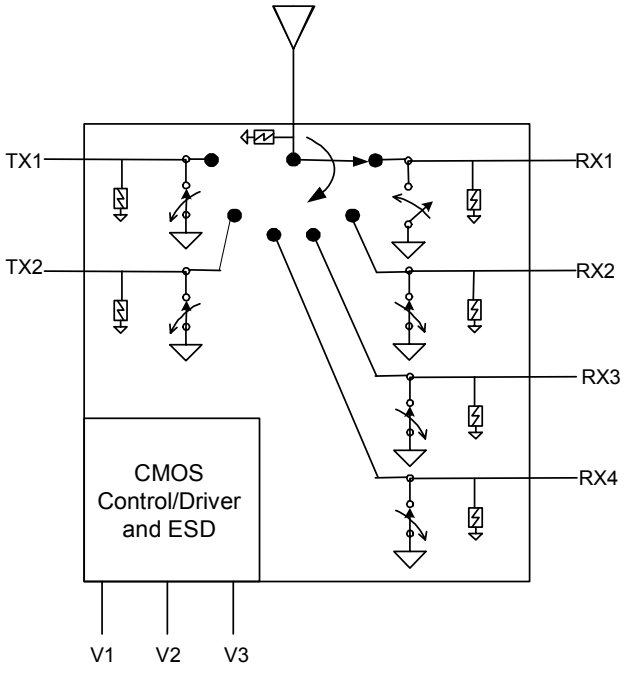
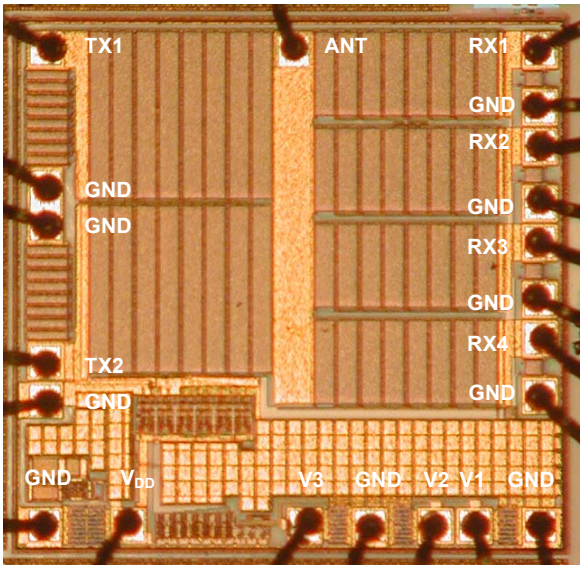



**Figure 2. Die Top View**



## Table 1. Electrical Specifications @ +25 °C, $V_{DD}$ = 2.75 V ($Z_S$ = $Z_L$ = 50 Ω)

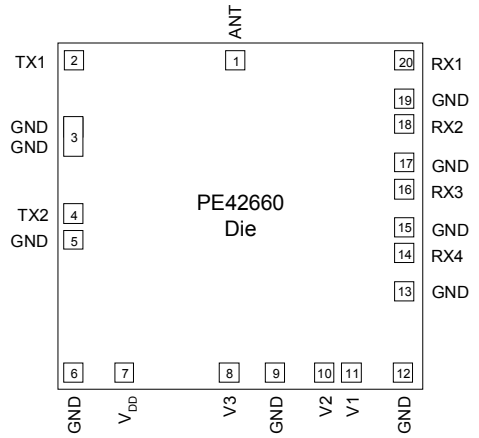
| Parameter | Conditions | Typical | Units |
|---|---|---|---|
| Operational Frequency | | 100-3000 | MHz |
| Insertion Loss | ANT - TX - 850 / 900 MHz<br>ANT - TX - 1800 / 1900 MHz<br>ANT - RX - 850 / 900 MHz<br>ANT - RX - 1800 / 1900 MHz | 0.55<br>0.65<br>0.90<br>1.00 | dB<br>dB<br>dB<br>dB |
| Isolation | TX - RX - 850 / 900 MHz<br>TX - RX - 1800 / 1900 MHz<br>TX - TX - 850 / 900 MHz<br>TX - TX - 1800 / 1900 MHz<br>ANT - TX - 850 / 900 MHz<br>ANT - TX - 1800 / 1900 MHz | 48<br>40<br>29<br>25<br>31<br>25 | dB<br>dB<br>dB<br>dB<br>dB<br>dB |
| Return Loss | 850 / 900 MHz<br>1800 / 1900 MHz | 22<br>23 | dB |
| 2nd Harmonic | 35 dBm TX Input - 850 / 900 MHz<br>33 dBm TX Input - 1800 / 1900 MHz | -88<br>-85 | dBc |
| 3rd Harmonic | 35 dBm TX Input - 850 / 900 MHz<br>33 dBm TX Input - 1800 / 1900 MHz | -85<br>-84 | dBc |
| Switching Time | (10-90%) (90-10%) RF | 2 | µs |

## Table 2. Operating Ranges

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Temperature range | $T_{OP}$ | -40 | | +85 | °C |
| $V_{DD}$ Supply Voltage | $V_{DD}$ | 2.65 | 2.75 | 2.85 | V |
| $I_{DD}$ Power Supply Current ($V_{DD}$ = 2.75 V) | $I_{DD}$ | | 13 | 20 | µA |
| TX input power[1] (VSWR ≤ 3:1) | $P_{IN}$ | | | +35 | dBm |
| RX input power[1] (VSWR ≤1:1) | $P_{IN}$ | | | +20 | dBm |
| Control Voltage High | $V_{IH}$ | 0.7 x $V_{DD}$ | | | V |
| Control Voltage Low | $V_{IL}$ | | | 0.3 x $V_{DD}$ | V |

Note: 1. Assumes RF input period of 4620 µs and duty cycle of 50%.

## Figure 3. Pin Configuration (Top View)




## Table 3. Pin Descriptions

| Pin No. | Pin Name | Description |
|---|---|---|
| 1[3] | ANT | RF Common – Antenna |
| 2[3] | TX1 | RF I/O - TX1 |
| 3[2] | GND | Ground (Requires two bond wires) |
| 4[3] | TX2 | RF I/O – TX2 |
| 5[2] | GND | Ground |
| 6[2] | GND | Ground |
| 7 | $V_{DD}$ | Supply |
| 8 | V3 | Switch control input, CMOS logic level |
| 9[2] | GND | Ground |
| 10 | V2 | Switch control input, CMOS logic level |
| 11 | V1 | Switch control input, CMOS logic level |
| 12[2] | GND | Ground |
| 13[2] | GND | Ground |
| 14[3] | RX4 | RF I/O – RX4 |
| 15[2] | GND | Ground |
| 16[3] | RX3 | RF I/O – RX3 |
| 17[2] | GND | Ground |
| 18[3] | RX2 | RF I/O – RX2 |
| 19[2] | GND | Ground |
| 20[3] | RX1 | RF I/O – RX1 |

Notes: 2. Bond wires should be physically short and connected to ground plane for best performance.

3. Blocking capacitors needed only when non-zero DC voltage present.

## Table 4. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on any input | -0.3 | $V_{DD}$+ 0.3 | V |
| $T_{ST}$ | Storage temperature range | -65 | +150 | °C |
| $P_{IN}$(50 Ω) | TX input power (50 Ω)[4,5] | | +38 | dBm |
| | RX input power (50 Ω) [4,5] | | +23 | |
| $P_{IN}$ (∞:1) | TX input power (VSWR ∞:1) [4,5] | | +35 | dBm |
| $V_{ESD}$ | ESD Voltage (HBM, MIL_STD 883 Method 3015.7) | | 1500 | V |
| | ESD Voltage at ANT Port (IEC 61000-4-2) | | 1700 | V |

Notes: 4. Assumes RF input period of 4620 µs and duty cycle of 50%.

5. $V_{DD}$ within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

## Table 5. Truth Table

| Path | V3 | V2 | V1 |
|---|---|---|---|
| ANT – RX1 | 0 | 0 | 0 |
| ANT – RX2 | 0 | 0 | 1 |
| ANT – RX3 | 0 | 1 | 0 |
| ANT – RX4 | 0 | 1 | 1 |
| ANT - TX1 | 1 | 0 | x |
| ANT - TX2 | 1 | 1 | x |

### Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

## Evaluation Kit

The SP6T Evaluation Kit board was designed to ease customer evaluation of the PE42660 RF switch.

The PE42660 has two high power TX ports and four high isolation RX ports. The TX ports are symmetric and are designed as paths for the 850, 900, 1800, or 1900 MHz bands. The RX ports are also symmetric and can be assigned to any of these frequency bands.

The ANT port connects through a 50 Ω transmission line to the top SMA connector, J1. The RX and TX ports connect through 50 Ω transmission lines to SMA connectors J2 – J7. A through 50 Ω transmission line between SMA connectors J9 and J10 allows estimation of the PCB losses over environmental conditions. An open transmission line connected to J11 is also provided.

J8 supplies DC power to the pin marked $V_{DD}$ and the bottom row of pins, which is GND. 1 MΩ pull-up resistors are connected from $V_{DD}$ to each of the three control logic inputs: V1, V2, and V3. These pull-up resistors are provided for ease of evaluation on this board and are not required for the PE42660 to operate.

Adding a jumper between a control pin and the adjacent GND pin on the bottom row of J8 will set a logic-0 on that control pin. Removing the jumper will set a logic-1. To evaluate the PE42660, add or remove jumpers according to the truth table in Table 5.

**Figure 4. Evaluation Board Layout**
Peregrine Specification 101/0205

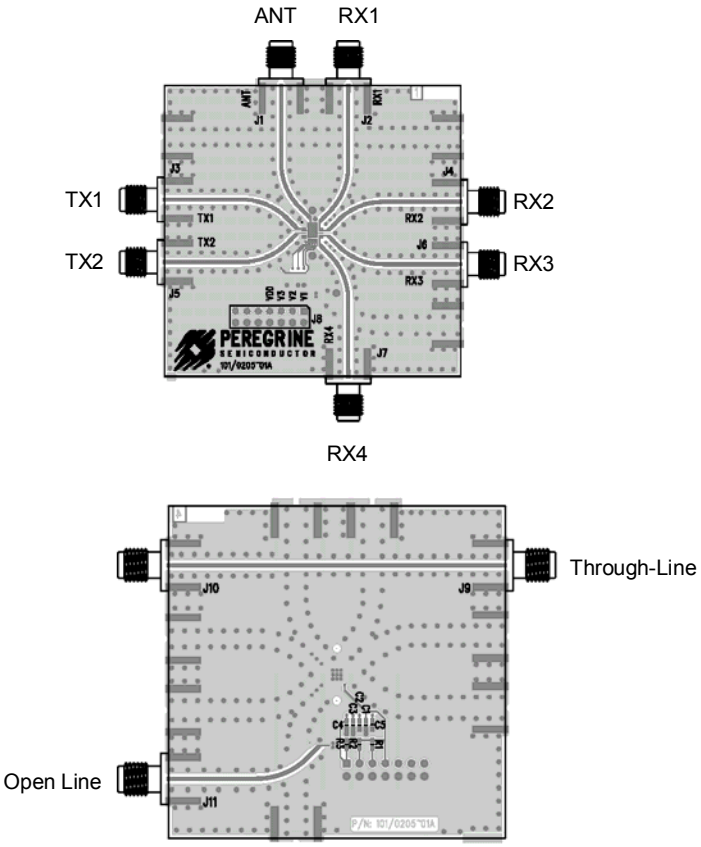
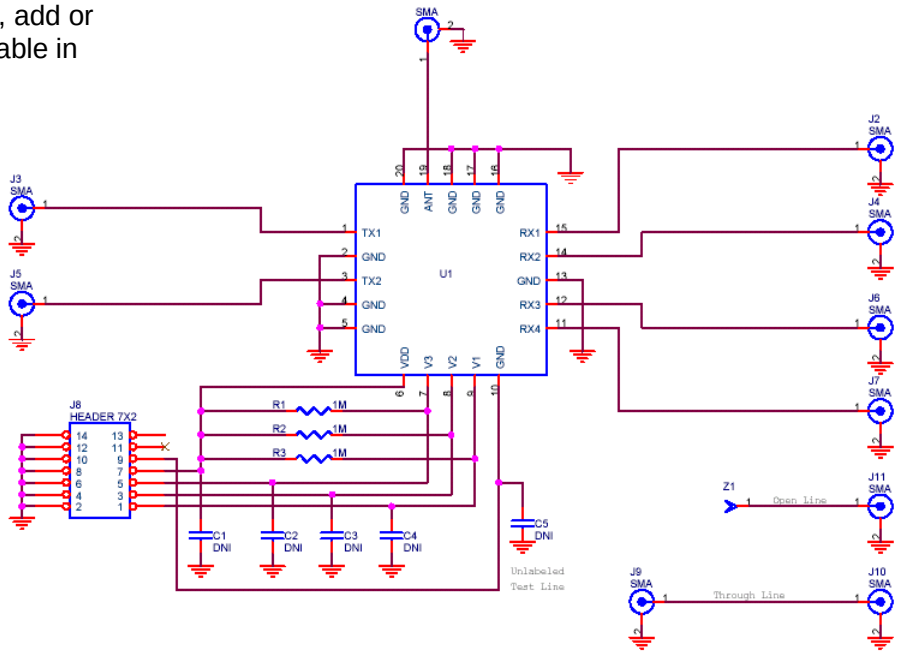



**Figure 5. Evaluation Board Schematic**
Peregrine Specification 102/0267



## Electrical Test and Performance Specifications

PE42660 dice are 100% electrically tested for the parameters listed below from Table 1 and Table 2. All other parameters are guaranteed through design and characterization.

- Insertion Loss (all ports)
- TX1 & TX2 Harmonics
- TX – RX Isolation
- $I_{DD}$ supply current
- Control pin leakages

## Wafer and Die Packaging

Peregrine Semiconductor has two methods for shipping dice to our customers. The shipping option used is based on the customer's requirements and the number of dice.

Peregrine offers product dice in two packaging options: Standard Die Carrier Packages (waffle pack) and dice on Film Frames.

## Wafer Mount/Dicing

In preparation for dicing, wafers are thinned and polished and 100% electrically probed prior to mounting on film frame tape and rings. Figure 6 shows a wafer mounted on film frame using PVC backed mounting tape. In preparation for shipment, wafers are visually inspected after singulation and shipped with an electronic map file providing good dice locations.

## Storage and Preservation

Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.

Product should be stored in the original unopened packaging or, once opened, in a nitrogen purged cabinet at room temperature (45% + 15% relative humidity controlled environment).

Singulated wafers mounted on film frames are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used for mounting the product. This product can be stored up to 30 days. This applies whether or not the material has remained in its original sealed container. To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.

**Figure 6. Wafer on Film Frame**

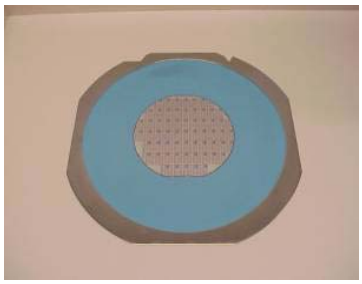


**Figure 7. Dice and Wafer Processing Flow**

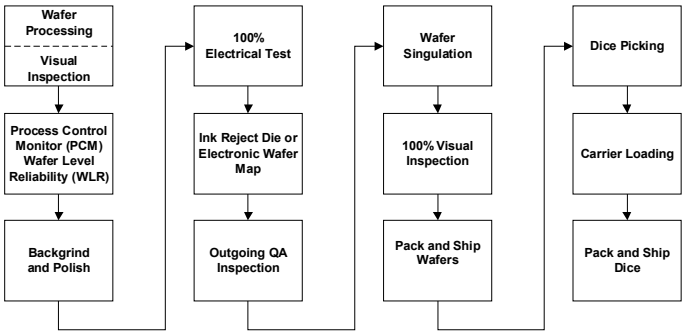
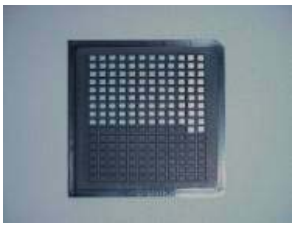



**Figure 8. Waffle Pack**



## Standard Die Carrier Package/Waffle Pack

Waffle packs are available to customers during product development and prototyping phase only. Orders will move to film frames at production launch or for large quantity requirements.

Dice have been 100% electrically probed, singulated, visually inspected and are packaged in a 2"x2" waffle pack (400 dice per waffle pack).

## Die Handling

All die products must be handled only at ESD safe workstations using standard ESD precautions. It is recommended that the die be handled only in a class 10,000 or better designated clean room environment.

Singulated dice are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip must be used.

## Recommended Dice Assembly Procedure

*Cleaning*

Dice do not require cleaning prior to assembly.

*Die Attach*

The PE42660 die substrate is sapphire – the recommended die attach operation for sapphire is epoxy die attach adhesive. An eutectic die attach method does not work with sapphire substrates.

*Bonding*

Thermo compression gold ball or aluminum ultrasonic bonding may be used. The ball should cover the bonding pad, but not excessively, or it may short out the surrounding metallization. Aluminum or gold 1-mil wire is recommended. Note the bonding pad material is aluminum.

## Shipping Method

Standard die carrier packages and wafer film frames are placed in a wafer container and then vacuum-sealed inside an ESD shielded bag. Sealed product is then placed inside a corrugated cardboard box surrounded by bubble wrap or foam for maximum protection during shipment.

## Table 6. Mechanical Specifications

| Parameter | Minimum | Typical | Maximum | Units | Test Conditions |
|---|---|---|---|---|---|
| Die Size (x,y) | | 1.146 x 1.106 | | mm | As drawn |
| Die Size (x,y) | | 1.25 x 1.21 | | mm | Including excess sapphire, max. tolerance = ±0.1mm in either dimension |
| Wafer Thickness | 180 | 200 | 220 | µm | |
| Wafer Size | | 150 | | mm | |

## Table 7. Pad Coordinates

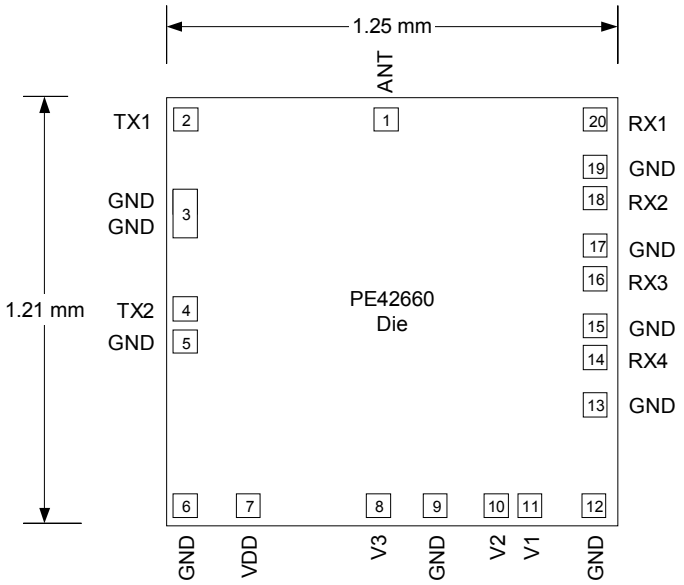
All pad locations originate from the die center and refer to the center of the pad.

All pad openings are 60 x 60 µm except for Pad #3 which is 140 x 60 µm. Minimum pad pitch is 80 µm.

Note 1. **-** Double pad, requires two bond wires.

| Pad # | Pad Name | Pad Center (µm) | |
|---|---|---|---|
| | | X | Y |
| 1 | ANT | 1.9 | 488.1 |
| 2 | TX1 | -511.3 | 491.3 |
| 3 | GND[1] | -511.3 | 168.9 |
| 4 | TX2 | -511.3 | -153.5 |
| 5 | GND | -511.3 | -233.5 |
| 6 | GND | -511.3 | -491.3 |
| 7 | VDD | -337.7 | -491.3 |
| 8 | V3 | 25.7 | -491.3 |
| 9 | GND | 160.9 | -491.3 |
| 10 | V2 | 296.1 | -491.3 |
| 11 | V1 | 376.1 | -491.3 |
| 12 | GND | 511.3 | -491.3 |
| 13 | GND | 511.3 | -223.7 |
| 14 | RX4 | 511.3 | -105.1 |
| 15 | GND | 511.3 | -25.1 |
| 16 | RX3 | 511.3 | 93.5 |
| 17 | GND | 511.3 | 173.5 |
| 18 | RX2 | 511.3 | 292.1 |
| 19 | GND | 511.3 | 372.1 |
| 20 | RX1 | 511.3 | 490.7 |

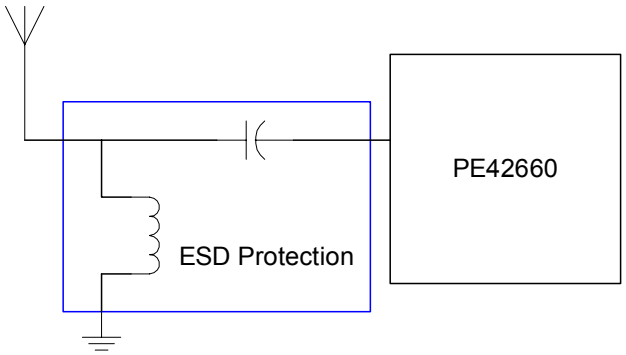
## Figure 9. Pad Numbering



## ESD Protection Circuit

Handset products must tolerate large ESD surges at the antenna interface without damage. The IEC 61000-4-2 standard specifies both 8 kV contact and 16 kV air discharges that typical handsets must survive. By itself, the PE42660 offers protection to 1.5 kV but with the addition of two inexpensive passive components, the switch can meet the levels as specified in the IEC spec. Figure 10 is the suggested solution for compliance with the IEC standards.

**Figure 10. ESD Protection Circuit**




L = 27 nH (muRata: LQG1127NJ00),

C = 33 pF (muRata: GRM33C0G330J50)

**Table 8. PE42660 Antenna Application Test Results (C=150 pF, R=330 Ω, IEC 61000-4-2 Standard)**

| Test Condition | Results |
|---|---|
| +8 kV contact discharge, 10 times with 1s intervals | Pass |
| -8 kV contact discharge, 10 times with 1s intervals | Pass |
| +16 kV air discharge, 10 times with 1s intervals | Pass |
| -16 kV air discharge, 10 times with 1s intervals | Pass |

**Table 9. Ordering Information**

| Order Code | Die ID | Description | Package | Shipping Method |
|---|---|---|---|---|
| 42660-90 | C9807_01 | PE42660-DIE-D | Film Frame | Wafer (Gross Die / Wafer Quantity) |
| 42660-99 | C9807_01 | PE42660-DIE-400G | Waffle Pack | 400 Dice / Waffle Pack |
| 42660-00 | C9807_01 | PE42660-DIE-1H | Evaluation Kit | 1/ box |

## Sales Offices

### *The Americas*

**Peregrine Semiconductor Corp.**
9450 Carroll Park Drive
San Diego, CA 92121
Tel 858-731-9400
Fax 858-731-9499

### *Europe*

**Peregrine Semiconductor Europe**
***Commercial Products:***
Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73
***Space and Defense Products:***
180 Rue Jean de Guiramand
13852 Aix-En-Provence cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

### *North Asia Pacific*

**Peregrine Semiconductor K.K.**
5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

### *South Asia Pacific*

**Peregrine Semiconductor**
28G, Times Square,
No. 500 Zhangyang Road,
Shanghai, 200122, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

## Data Sheet Identification

### *Advance Information*

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### *Product Specification*

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.