Product Specification
PE4261 FLIP CHIP

SP4T UltraCMOS™ 2.6 V Switch
100 – 3000 MHz

Figure 1. Functional Diagram

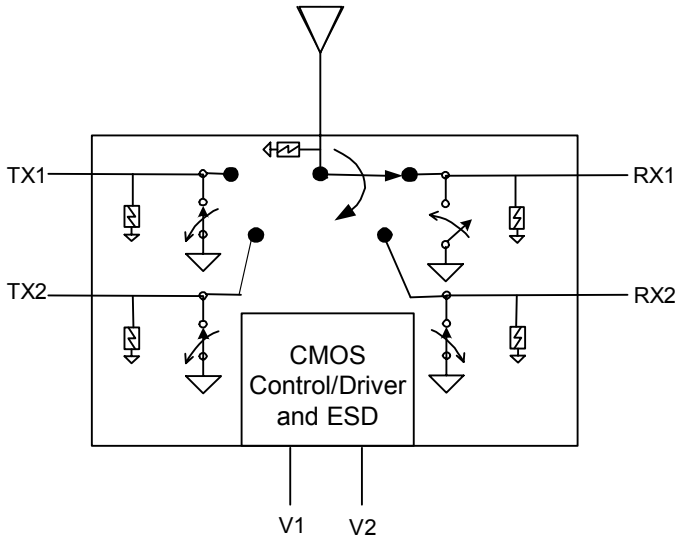
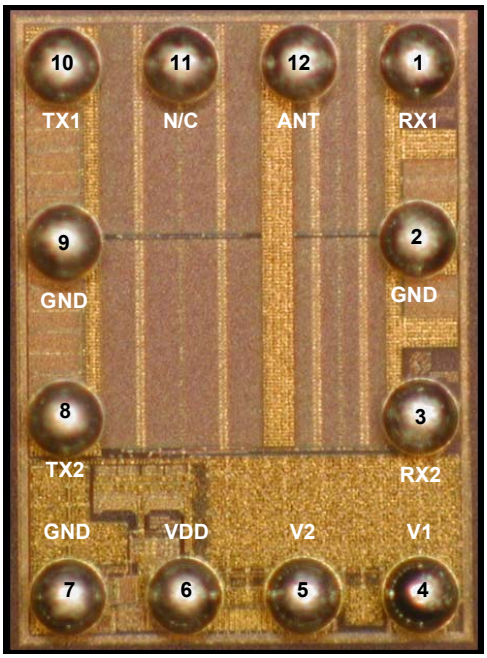


Figure 2. Die Top View



Features

- Two pin CMOS logic control inputs
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.70 dB at 1900 MHz
- Isolation of 39 dB at 900 MHz, 31 dB at 1900 MHz
- Low harmonics $2f_o$ = -82 dBc and $3f_o$ = -74 dBc at 35 dBm input power
- 1500 V HBM ESD tolerance
- Built in CMOS decoder/driver
- RX SAW over voltage protection circuit
- No blocking capacitors required

Product Description

The PE4261 SP4T RF UltraCMOS™ Flip Chip Switch is designed specifically to address the needs of the antenna switch module market for GSM Handsets. On-chip CMOS decode logic is used to facilitate two-pin, low voltage CMOS control inputs. High ESD tolerance of 1500 V at all ports, no blocking capacitor requirements and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ease of use.

The PE4261 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Table 1. PE4261 Electrical Specifications: Temp = 25°C, V_{DD} = 2.6 V

Parameter	Condition	Min	Typ	Max	Unit
Operational Frequency		100		3000	MHz
Insertion Loss	ANT - TX - 850 / 900 MHz ANT - TX - 1800 / 1900 MHz ANT - RX - 850 / 900 MHz ANT - RX - 1800 / 1900 MHz		0.55 0.7 0.85 1.05	0.65 0.8 1.0 1.2	dB dB dB dB
Isolation	TX - RX - 850 / 900 MHz (TX ON) TX - RX - 1800 / 1900 MHz (TX ON) TX1 - TX2 - 850 / 900 MHz (TX1 ON) TX1 - TX2 - 1800 / 1900 MHz (TX1 ON)	37 29 33 26	39 31 35 28		dB dB dB dB
Return Loss	850 / 900 MHz 1800 / 1900 MHz	18 14	20 16		dB dB
2nd Harmonic[1,2]	35 dBm TX Input Power - 850 / 900 MHz 33 dBm TX Input Power - 1800 / 1900 MHz		-82 -89	-78 -82	dBc dBc
3rd Harmonic[1,2]	35 dBm TX Input Power - 850 / 900 MHz 33 dBm TX Input Power - 1800 / 1900 MHz		-74 -68	-69 -65	dBc dBc
Switching time	(10-90%) (90-10%) RF		2	3	µs

Notes: 1. Measured in Pulsed Wave Mode.

2. Assumes RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005

Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RX1[3]	RF I/O – RX1
2	GND	Ground
3	RX2[3]	RF I/O – RX2
4	V1	Switch control input, CMOS logic level
5	V2	Switch control input, CMOS logic level
6	VDD	Supply
7	GND	Ground
8	TX2[3]	RF I/O - TX2
9	GND	Ground
10	TX1[3]	RF I/O - TX1
11	N/C	No Connect – Pin to be connected to an electrically isolated low capacitance pad
12	ANT[3]	RF Common – Antenna Input

Note: 3. Blocking capacitors needed only when non-zero DC voltage present.

Figure 3. Pin Configuration (Ball-Side Up)

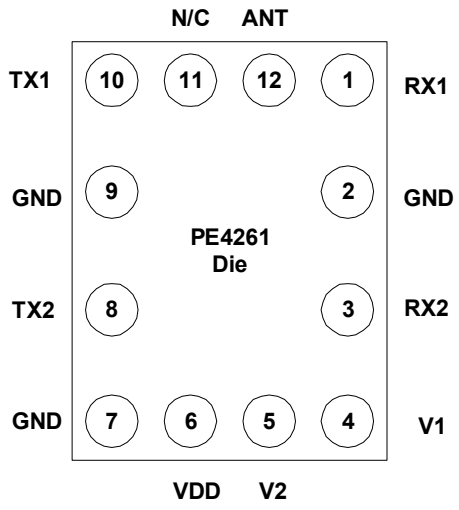


Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
T_{OP}	Operating temperature range	-40	+85	°C
P_{IN}	TX input power (50 Ω)		+38	dBm
	RX input power (50 Ω)		+23	
P_{IN} (∞:1)	TX input power (VSWR = (∞:1)[5,6] 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1)[5,6] 1710-1910 MHz		+33	
V_{ESD}[4]	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V
	ESD Voltage (CDM, JEDEC, JESD22-A114-B)		1500	V
	ESD Voltage (IEC 61000-4-2, ANT port)		2000	V

Note: 4. ANT port rated higher per Application note, see page 10.

5. Assumes RF input duty cycle of 50% and 4620 µs.

6. V_{DD} within operating range specified in Table 4.

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4. DC Electrical Specifications

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	2.4	2.6	2.8	V
I_{DD} Power Supply Current (V_{DD} = 2.6 V)		11	25	µA
Control Voltage High	0.7x V_{DD}			V
Control Voltage Low			0.3x V_{DD}	V

Table 5. Truth Table

Path	V2	V1
ANT - RX1	0	0
ANT - RX2	0	1
ANT - TX1	1	0
ANT - TX2	1	1

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Die ID	Description	Package	Shipping Method
PE4261-93	C9804_3	PE4261-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
PE4261-96	C9804_3	PE4261-DIE-255G	Waffle Pack	255 Dice / Waffle Pack
PE4261-10	C9804_3	PE4261-DIE-1H	Evaluation Kit	1 / Box

Sales Offices

The Americas

Peregrine Semiconductor Corporation
9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

Europe

Peregrine Semiconductor Europe
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73

Space and Defense Products

Americas:

Tel: 858-731-9453

Europe, Asia Pacific:

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

Peregrine Semiconductor, Korea
#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

South Asia Pacific

Peregrine Semiconductor, China
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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