

# NTMS4404N

## Power MOSFET

30 V, 12 A, Single N-Channel, SO-8

### Features

- High Density Power MOSFET with Ultra Low  $R_{DS(on)}$  for Higher Efficiency
- Miniature SO-8 Surface Mount Package Saving Board Space
- $I_{DSS}$  Specified at Elevated Temperature
- Diode Exhibits High Speed, Soft Recovery

### Applications

- Power Management for Battery Power Products
- Portable Products
- Computers, Printers, PCMCIA Cards
- Cell Phones, Cordless Telephones

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	30	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	9.6	A
		$T_A = 70^{\circ}\text{C}$		7.6	
	$t_p \leq 10\text{ s}$	$T_A = 25^{\circ}\text{C}$		12	
Power Dissipation (Note 1)	Steady State		$P_D$	1.56	W
	$t_p \leq 10\text{ s}$			2.5	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	7.0	A
		$T_A = 70^{\circ}\text{C}$		5.6	
Power Dissipation (Note 2)		$T_A = 25^{\circ}\text{C}$	$P_D$	0.83	W
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$ , DC = 2 %		$I_{DM}$	50	A
Operating Junction and Storage Temperature			$T_J$ , $T_{STG}$	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	6.0	A
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 20\text{ V}$ , $V_{GS} = 5\text{ V}$ , $I_{PK} = 7.25\text{ A}$ , $L = 19\text{ mH}$ , $R_G = 25\text{ }\Omega$ )			$E_{AS}$	500	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Junction-to-Ambient – $t = 10$ s (Note 1)	$R_{\theta JA}$	50	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	150	

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [1 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412 in sq.)

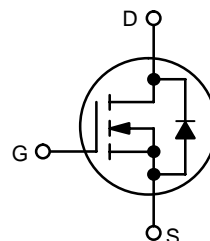


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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
30 V	9.7 m $\Omega$ @ 10 V	12 A
	15.5 m $\Omega$ @ 4.5 V	

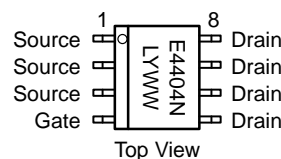
### N-Channel



### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



E4404N = Device Code  
L = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4404NR2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMS4404N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			25		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V	T <sub>J</sub> = 25°C		1.0	μA
			T <sub>J</sub> = 100°C		5.0	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	2.2	3.0	V
Gate Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-5.0		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A		9.7	11.5	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.0 A		15.5	17.5	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 12 A		17.5		S

### CHARGES AND CAPACITANCES

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 24 V		1975	2500	pF
Output Capacitance	C <sub>OSS</sub>			575	750	
Reverse Transfer Capacitance	C <sub>RSS</sub>			180	300	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 12 A		50	70	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			2.4		
Gate-to-Source Charge	Q <sub>GS</sub>			7.5		
Gate-to-Drain Charge	Q <sub>GD</sub>			16		

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 12 A, R <sub>G</sub> = 2.5 Ω		15	25	ns
Rise Time	t <sub>r</sub>			25	50	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			35	55	
Fall Time	t <sub>f</sub>			15	30	

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 24 V, I <sub>D</sub> = 6.0 A, R <sub>G</sub> = 2.5 Ω		20		ns
Rise Time	t <sub>r</sub>			80		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			25		
Fall Time	t <sub>f</sub>			15		

### DRAIN-SOURCE DIODE CHARACTERISTICS (Note 4)

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 6.0 A	T <sub>J</sub> = 25°C		0.80	1.1	V
			T <sub>J</sub> = 125°C		0.65		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>SD</sub> /d t = 100 A/μs, I <sub>S</sub> = 6.0 A			40	55	ns
Charge Time	t <sub>a</sub>				23		
Discharge Time	t <sub>b</sub>				17		
Reverse Recovery Charge	Q <sub>RR</sub>				0.05		

#### NOTES:

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

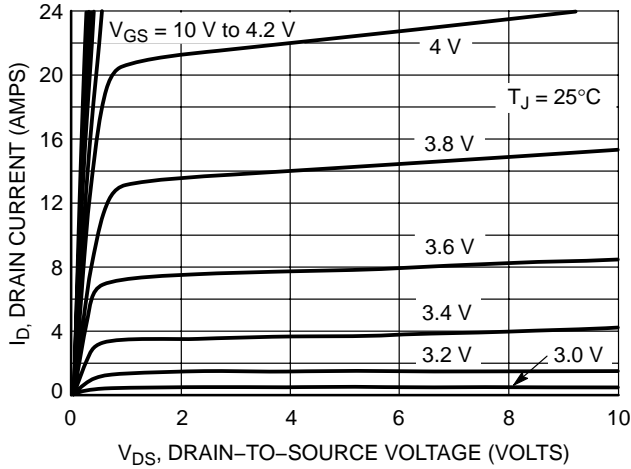


Figure 1. On-Region Characteristics

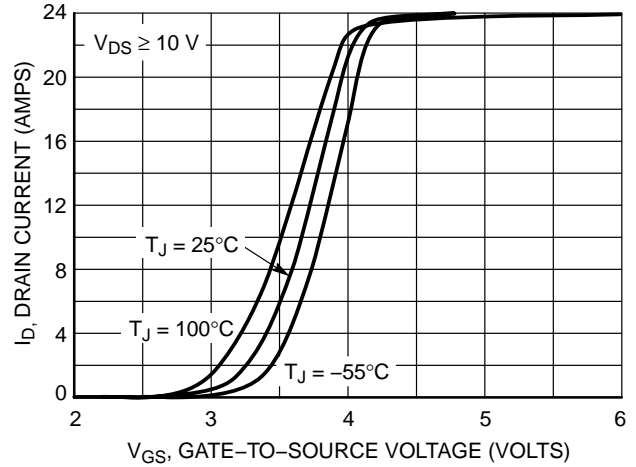


Figure 2. Transfer Characteristics

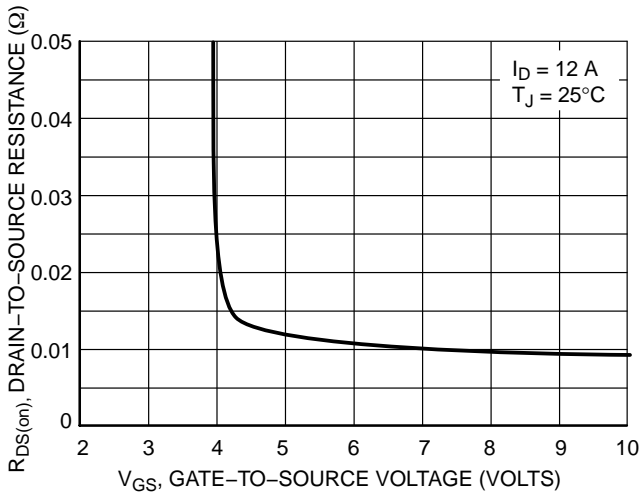


Figure 3. On-Resistance vs. Gate-to-Source Voltage

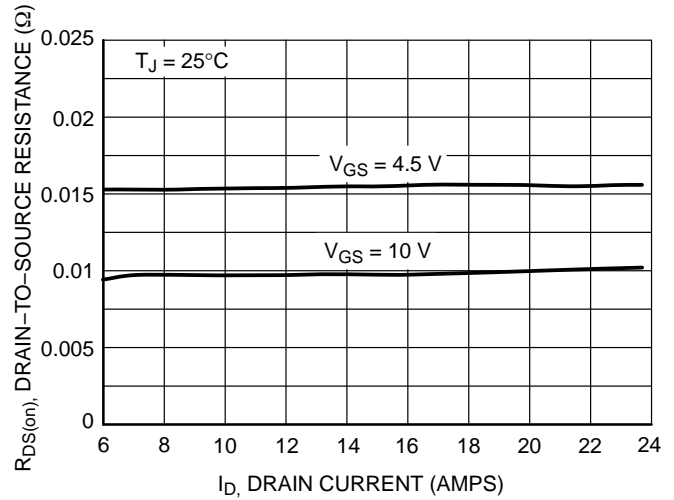


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

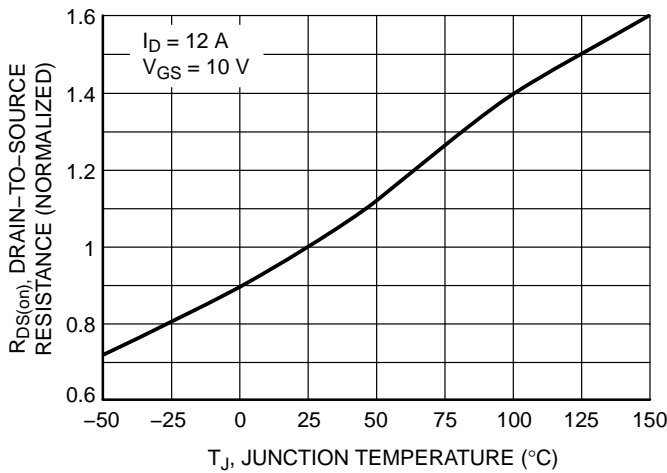


Figure 5. On-Resistance Variation with Temperature

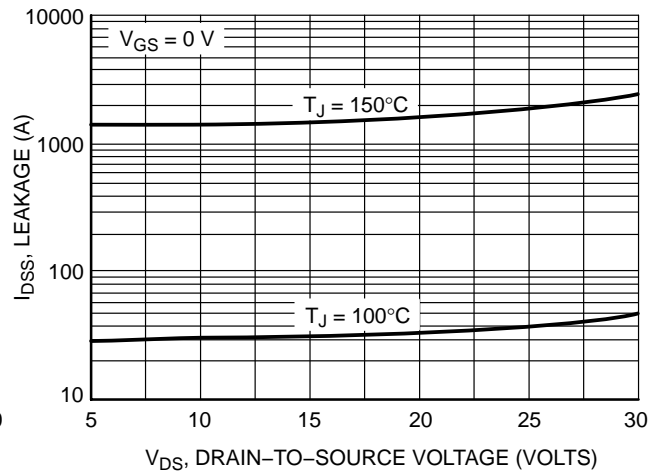
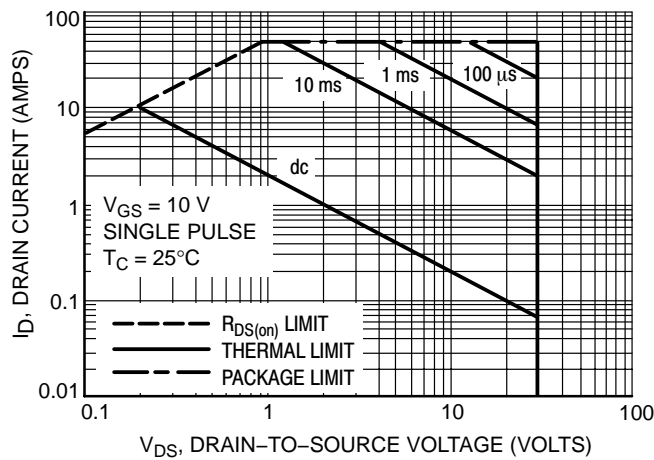
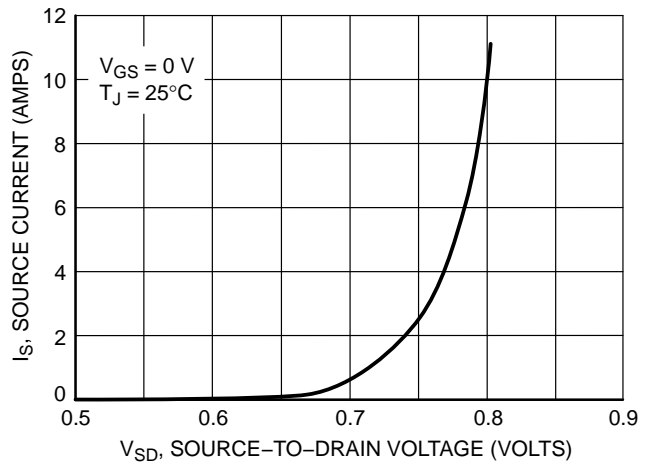
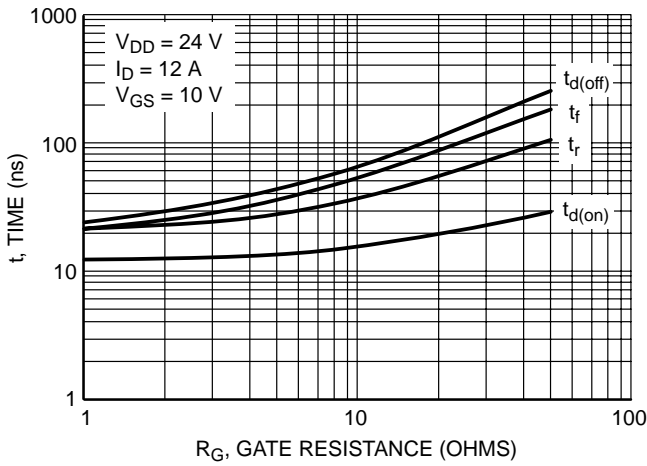
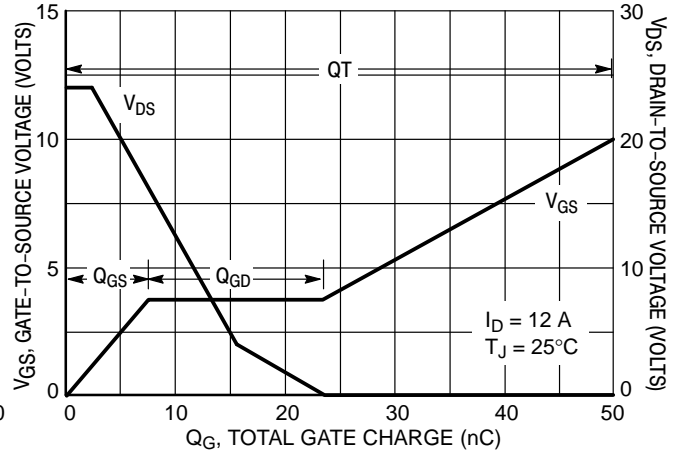
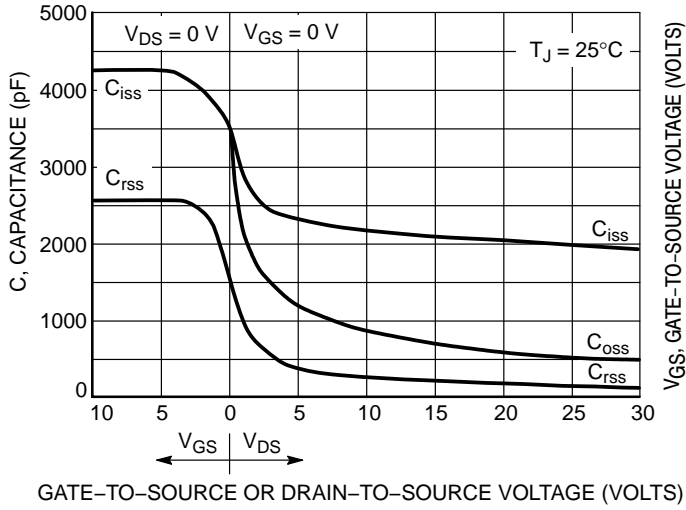


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



# NTMS4404N

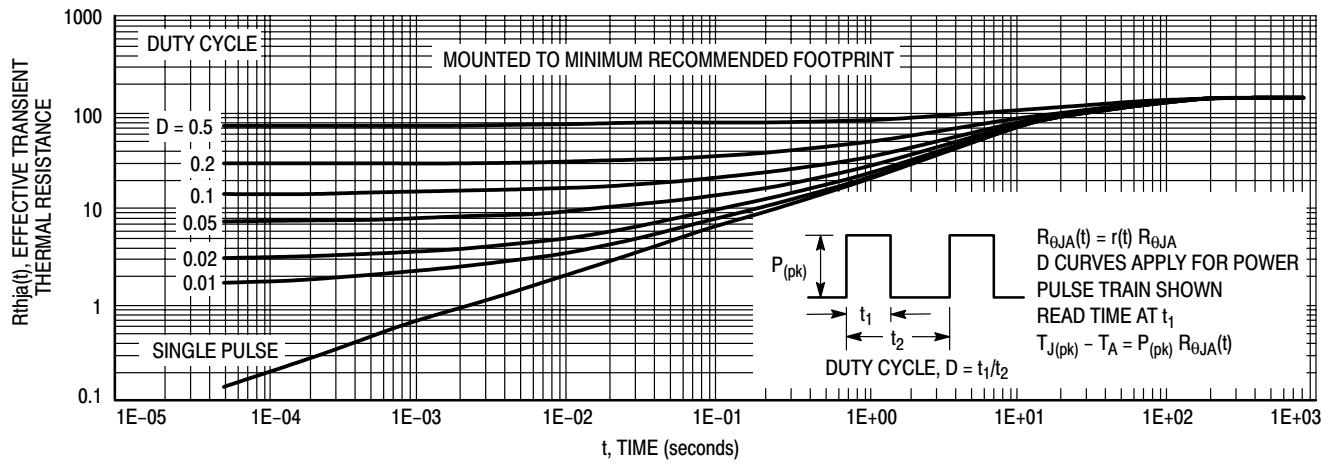
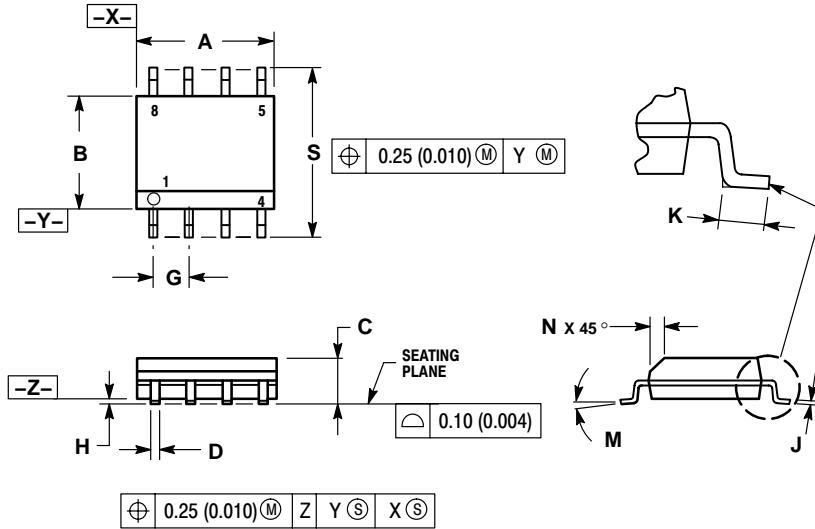


Figure 12. Thermal Response – Various Duty Cycles

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## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AA



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
E	1.27 BSC		0.050 BSC	
F	0.10	0.25	0.004	0.010
G	0.19	0.25	0.007	0.010
H	0.40	1.27	0.016	0.050
J	0°	8°	0°	8°
K	0.25	0.50	0.010	0.020
M	5.80	6.20	0.228	0.244

### STYLE 12:

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

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