NTMD3P03R2

Power MOSFET
-3.05 Amps, -30 Volts
Dual P−Channel SO−8

Features

- High Efficiency Components in a Dual SO−8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$
- Miniature SO−8 Surface Mount Package − Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for the SO−8 Package is Provided

Applications

- DC−DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery−Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−30	V
Gate−to−Source Voltage − Continuous	V_{GS}	±20	V
Thermal Resistance − Junction−to−Ambient (Note 1) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ 25°C Continuous Drain Current @ 70°C Pulsed Drain Current (Note 4)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	171 0.73 −2.34 −1.87 −8.0	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 2) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ 25°C Continuous Drain Current @ 70°C Pulsed Drain Current (Note 4)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	100 1.25 −3.05 −2.44 −12	°C/W W A A A
Thermal Resistance − Junction−to−Ambient (Note 3) Total Power Dissipation @ T_A = 25°C Continuous Drain Current @ 25°C Continuous Drain Current @ 70°C Pulsed Drain Current (Note 4)	$R_{\theta JA}$ P_D I_D I_D I_{DM}	62.5 2.0 −3.86 −3.1 −15	°C/W W A A A
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = −30 Vdc, V_{GS} = −4.5 Vdc, Peak I_L = −7.5 Apk, L = 5 mH, R_G = 25 Ω)	E_{AS}	140	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

1. Minimum FR−4 or G−10 PCB, t = Steady State.
2. Mounted onto a 2″ square FR−4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Mounted onto a 2″ square FR−4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

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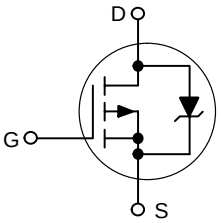
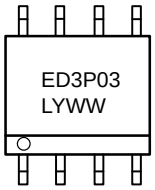
V_{DSS}	$R_{DS(ON)}$ TYP	I_D MAX
−30 V	85 mΩ @ −10 V	−3.05 A

P−Channel



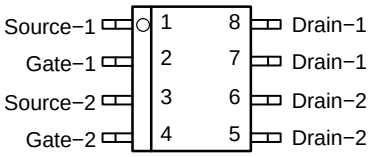
SO−8
CASE 751
STYLE 11

MARKING DIAGRAM



ED3P03 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTMD3P03R2	SO−8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = −250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 −30 −	 − −30	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = −24 Vdc, V_{GS} = 0 Vdc, T_J = 25°C) (V_{DS} = −24 Vdc, V_{GS} = 0 Vdc, T_J = 125°C) (V_{DS} = −30 Vdc, V_{GS} = 0 Vdc, T_J = 25°C)		I_{DSS}	 − − −	 − − −	 −1.0 −20 −2.0	μAdc
Gate−Body Leakage Current (V_{GS} = −20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	 −	 −	 −100	nAdc
Gate−Body Leakage Current (V_{GS} = +20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	 −	 −	 100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = −250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 −1.0 −	 −1.7 3.6	 −2.5 −	Vdc
Static Drain−to−Source On−State Resistance (V_{GS} = −10 Vdc, I_D = −3.05 Adc) (V_{GS} = −4.5 Vdc, I_D = −1.5 Adc)		$R_{DS(on)}$	 − −	 0.063 0.090	 0.085 0.125	Ω
Forward Transconductance (V_{DS} = −15 Vdc, I_D = −3.05 Adc)		g_{FS}	−	5.0	−	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = −24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	520	750	pF
Output Capacitance		C_{oss}	−	170	325	
Reverse Transfer Capacitance		C_{rss}	−	70	135	
SWITCHING CHARACTERISTICS (Notes 6 and 7)						
Turn−On Delay Time	(V_{DD} = −24 Vdc, I_D = −3.05 Adc, V_{GS} = −10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	12	22	ns
Rise Time		t_r	−	16	30	
Turn−Off Delay Time		$t_{d(off)}$	−	45	80	
Fall Time		t_f	−	45	80	
Turn−On Delay Time	(V_{DD} = −24 Vdc, I_D = −1.5 Adc, V_{GS} = −4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	−	16	−	ns
Rise Time		t_r	−	42	−	
Turn−Off Delay Time		$t_{d(off)}$	−	32	−	
Fall Time		t_f	−	35	−	
Total Gate Charge	(V_{DS} = −24 Vdc, V_{GS} = −10 Vdc, I_D = −3.05 Adc)	Q_{tot}	−	16	25	nC
Gate−Source Charge		Q_{gs}	−	2.0	−	
Gate−Drain Charge		Q_{gd}	−	4.5	−	
BODY−DRAIN DIODE RATINGS (Note 6)						
Diode Forward On−Voltage	(I_S = −3.05 Adc, V_{GS} = 0 V) (I_S = −3.05 Adc, V_{GS} = 0 V, T_J = 125°C)	V_{SD}	 −	 −0.96 −0.78	 −1.25 −	Vdc
Reverse Recovery Time	(I_S = −3.05 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	34	−	ns
		t_a	−	18	−	
		t_b	−	16	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.03	−	μC

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

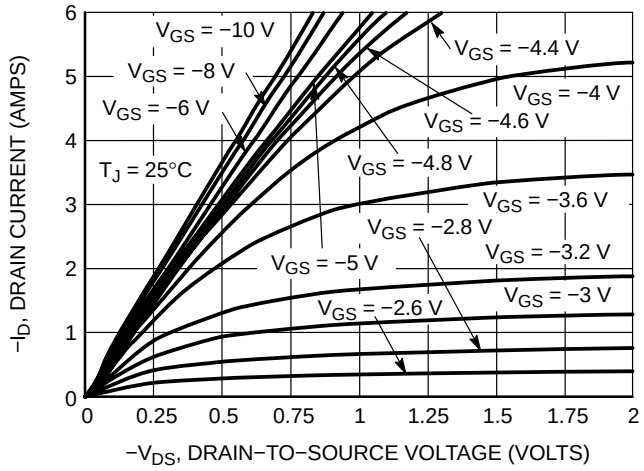


Figure 1. On−Region Characteristics

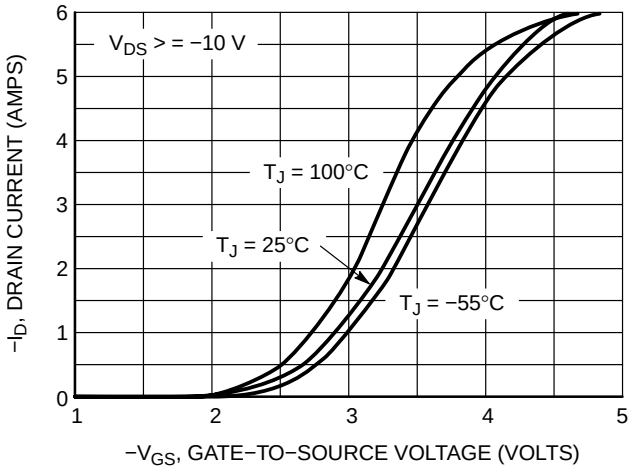


Figure 2. Transfer Characteristics

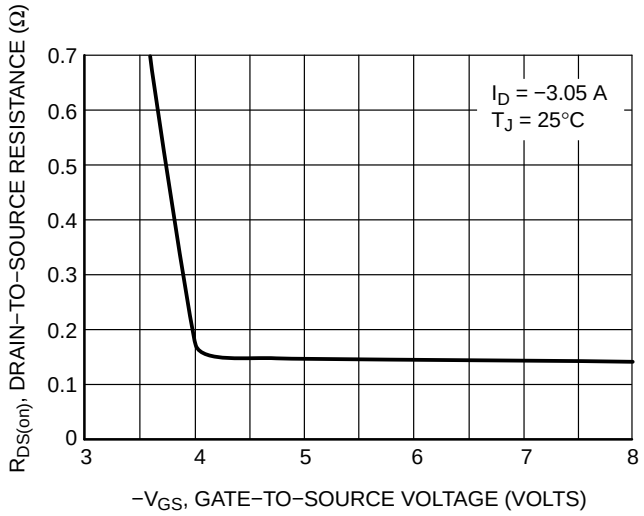


Figure 3. On−Resistance vs. Gate−to−Source Voltage

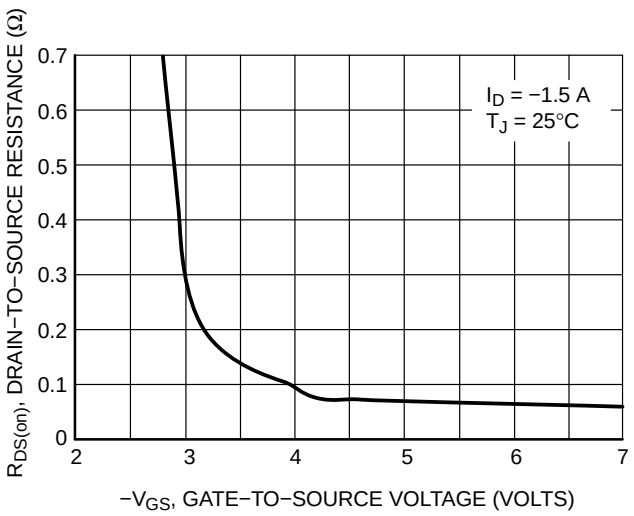


Figure 4. On−Resistance vs. Gate−to−Source Voltage

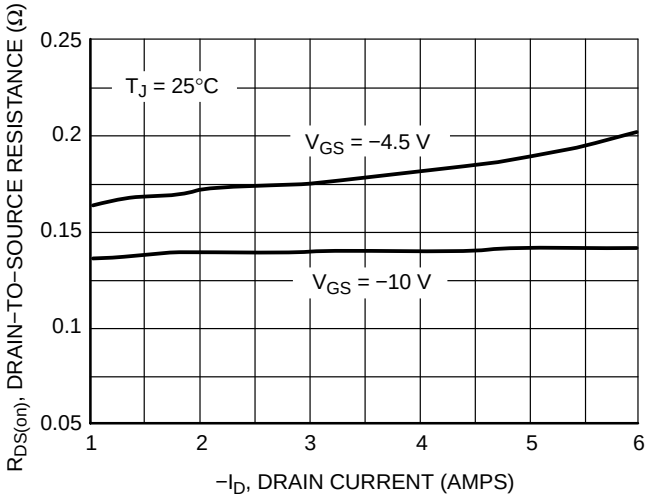


Figure 5. On−Resistance vs. Drain Current and Gate Voltage

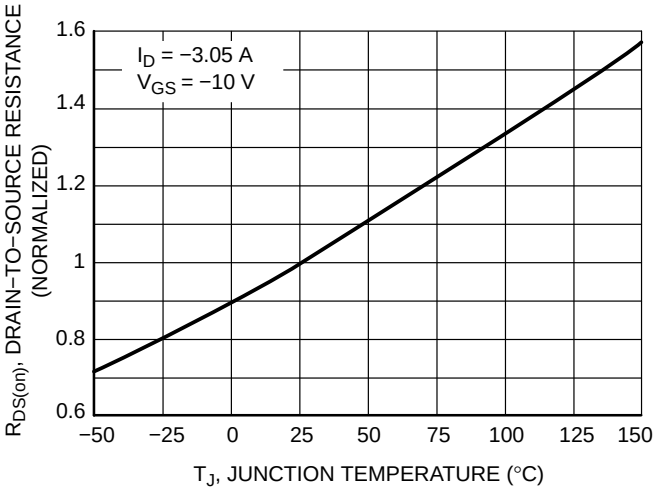


Figure 6. On Resistance Variation with Temperature

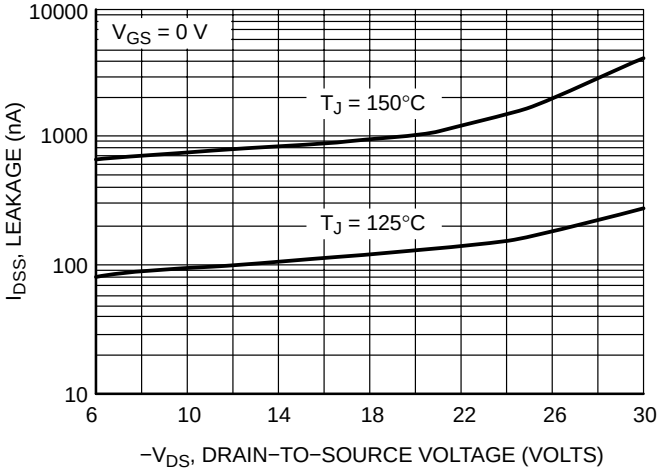


Figure 7. Drain−to−Source Leakage Current vs. Voltage

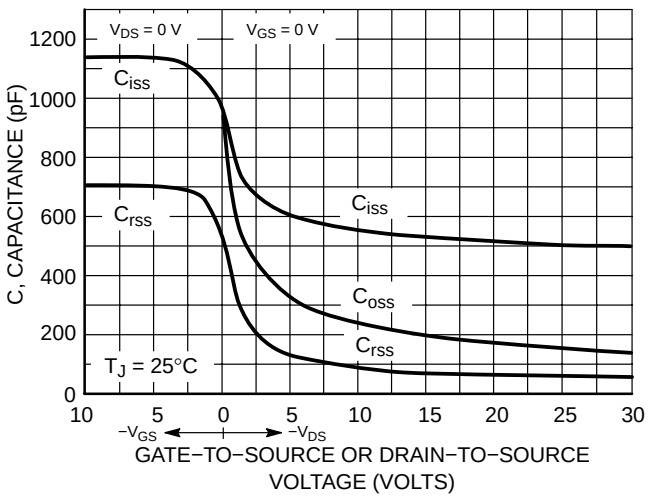


Figure 8. Capacitance Variation

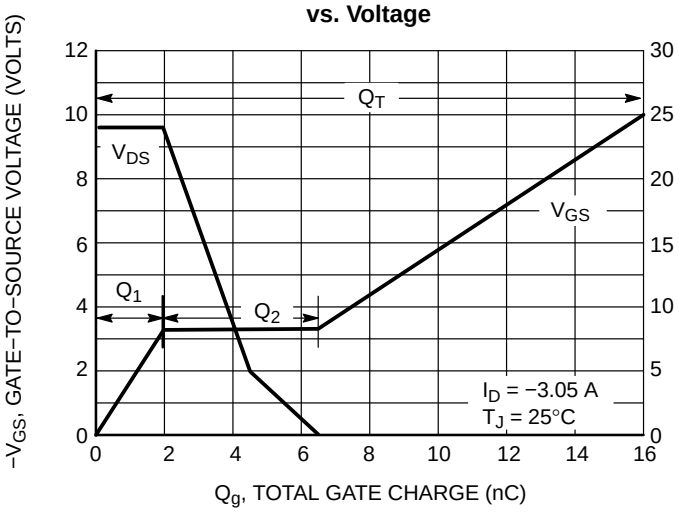


Figure 9. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

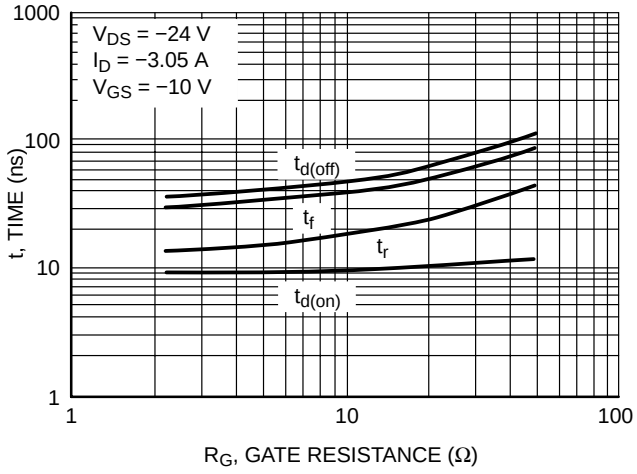


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

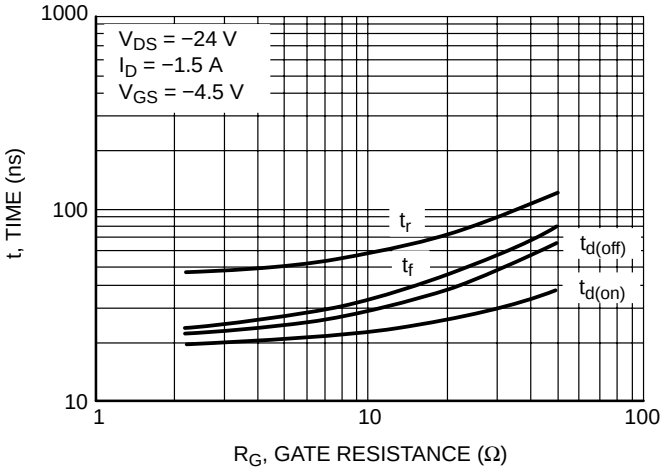


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

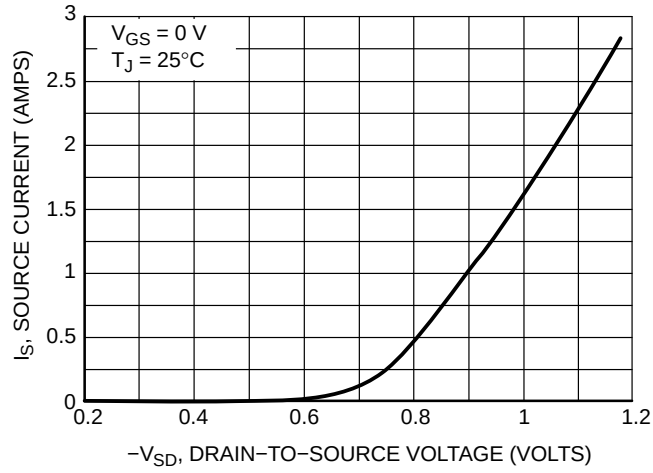


Figure 12. Diode Forward Voltage vs. Current

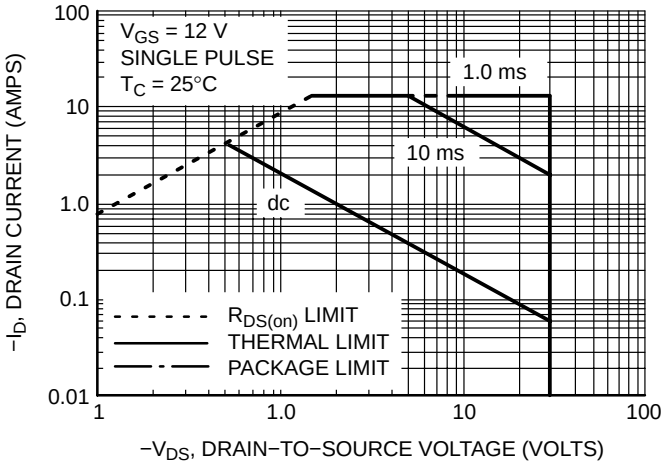


Figure 13. Maximum Rated Forward Biased Safe Operating Area

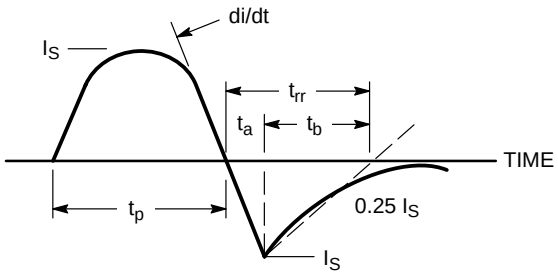


Figure 14. Diode Reverse Recovery Waveform

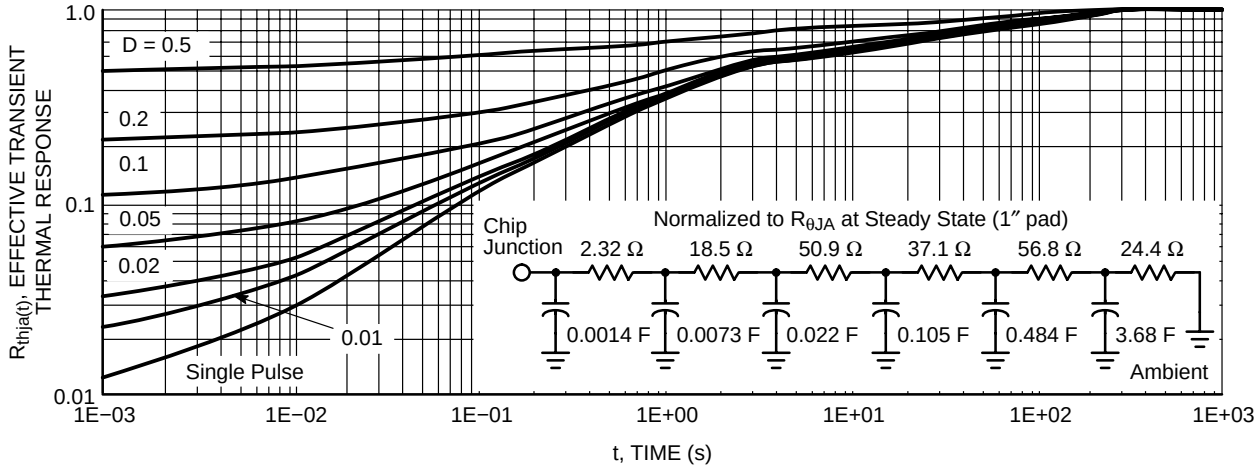
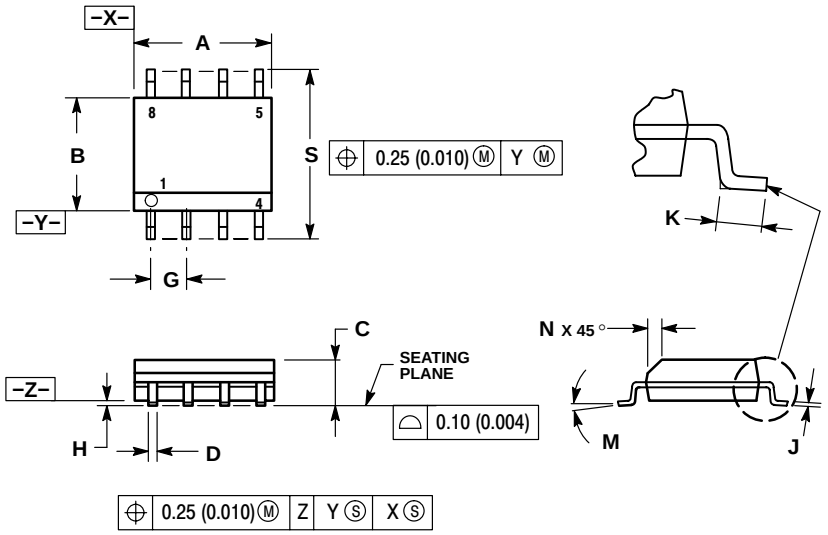


Figure 15. FET Thermal Response

PACKAGE DIMENSIONS

SO−8
CASE 751−07
ISSUE AB

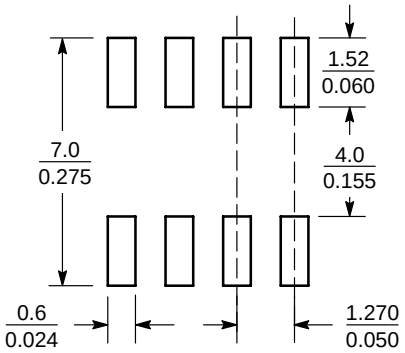


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Email: orderlit@onsemi.com

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