CS1112

Quad Power Output Driver

The CS1112 is a Power Output Driver. The IC incorporates four protected DMOS low–side drivers designed to drive inductive and resistive loads in an automotive environment. The outputs are controlled by an 8–bit serial peripheral interface (SPI) or its associated parallel input. Each output contains overcurrent protection, open load detection, and inductive flyback clamps. The device is overvoltage protected. Overcurrent and open load faults are reported over the SPI port, and at the STATUS lead.

I/O Control

SPI communication is initiated by asserting CSB low. Data at the SI lead is transferred on the rising edge of SCLK. The MSB is transferred first. The outputs become active at the rising edge of CSB. Diagnostic status bits are transferred out the SO lead at the falling edge of SCLK. The SO lead is high impedance while CSB is high. An open drain output, (STATUS) reports a fault (short to V_{PWR}, GND, or open load) has occurred at one or more of the outputs.

Protection

Each output independently detects shorts to V_{PWR} while the output is “on” and open load/short to ground while the output is “off”. The fault register will be set if a fault occurs at the output. The fault register will be reset if the fault condition is removed from the output. The fault data is latched when CSB is asserted low.

If an overcurrent condition or short circuit to V_{BATT} occurs, the output goes into a low duty cycle mode for the duration of the fault. The outputs are disabled during an overvoltage or undervoltage condition.

Features

- 4.0 MHz Serial Input Bus
- Parallel Input Control
- 1.0 Ω DMOS Drivers (typ)
- Power On Reset
- Internal Flyback Clamps
- Status Output
- Fault Protection
  - 46 V Peak Transient
  - Power Limiting
  - Undervoltage
  - Overvoltage
- Fault Reporting
  - Open Load
  - Short Circuit
- 8 Internally Fused Leads

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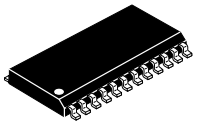
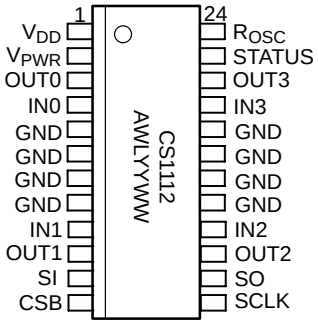


SO–24L
DW SUFFIX
CASE 751E

PIN CONNECTIONS AND MARKING DIAGRAM

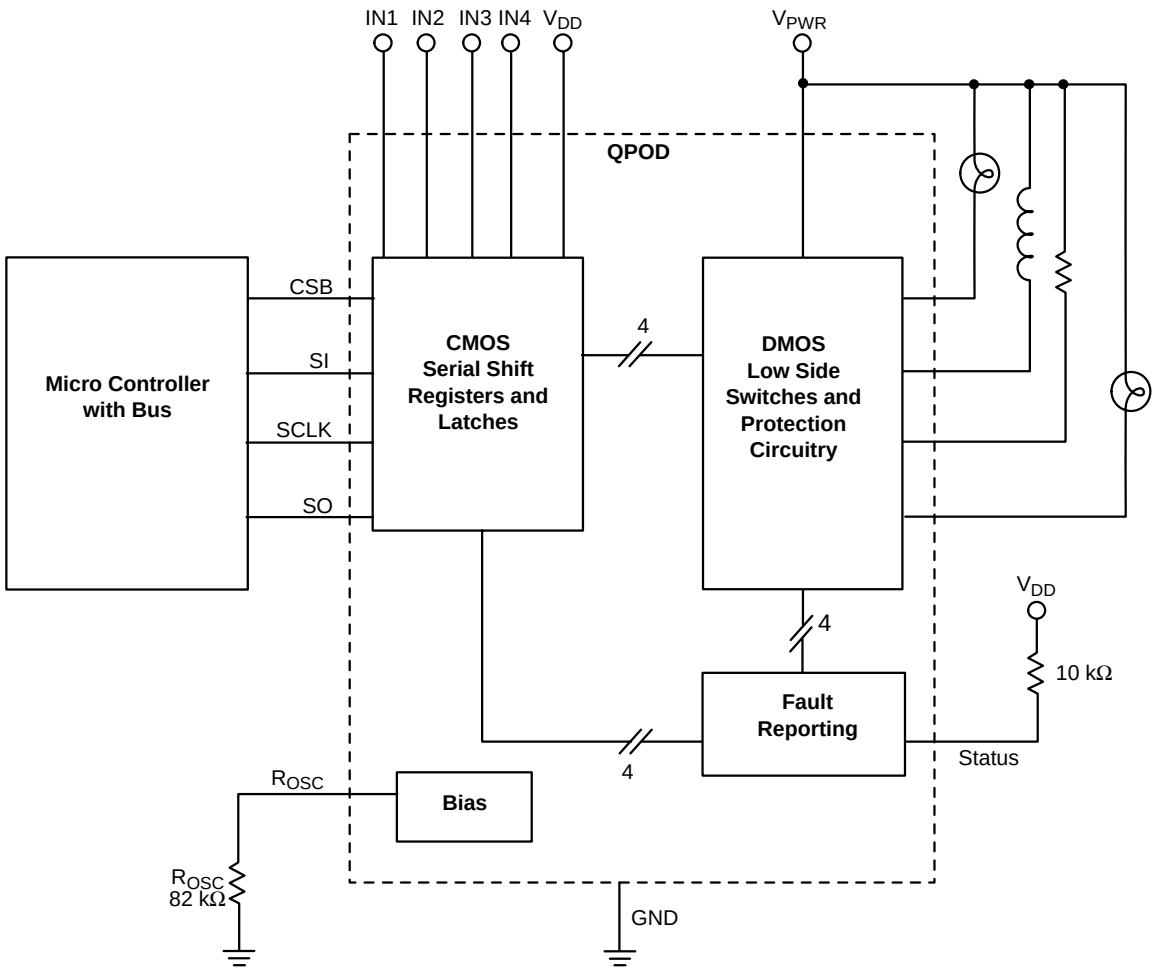


A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
CS1112YDWF24	SO–24L	31 Units/Rail
CS1112YDWFR24	SO–24L	1000 Tape & Reel

APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
DC Supply (V_{PWR})	–0.3 to 30	V
Output DC Voltage (Out 0, 1, 2, 3)	46	V
V_{DD} Supply Voltage	–0.3 to +7.0	V
Peak Transient (1.0 ms rise time, 300 ms period, 32 V Load Dump @ 14 V V_{PWR})	46	V
Digital Input Voltage	–0.3 to V_{DD} + 0.3	V
Single Pulse Avalanche Energy (I = 450 mA)(Out 0, 1, 2, 3)	50	mJ
Operating Junction Temperature, T_J	–40 to 150	°C
ESD Capability (Human Body Model)	1.5	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1.)	230 peak	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (9.0 V < V_{PWR} < 17 V, 4.5 V < V_{DD} < 5.5 V, –40°C < T_J < 125°C, 5.5 V < V_{PWR} < 25 V, (Outputs Functional); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Supply Voltages and Currents					
V_{DD} Power On Reset Threshold	Outputs Latched Off By Event	2.5	3.0	3.5	V
V_{DD} Power On Reset Hysteresis	–	–	200	–	mV
V_{PWR} Undervoltage	Outputs Latched Off By Event	4.0	4.5	5.0	V
V_{PWR} Overvoltage Lockout	Outputs Latched Off By Event	30	35	45	V
Digital Supply Current, $I_{V(DD)}$	All Outputs On (@ 350 mA)	–	–	5.0	mA
Analog Supply Current, $I_{V(PWR)}$	All Outputs On (@ 350 mA)	–	–	5.0	mA
Sleep Current, $I_{V(PWR)}$	V_{DD} ≤ 0.5 V	–	–	10	μA
Digital Inputs and Outputs					
V_{IN} High	SI, SCLK, CSB, IN0, IN1, IN2, IN3	70	–	–	%V_{DD}
V_{IN} Low	SI, SCLK, CSB, IN0, IN1, IN2, IN3	–	–	30	%V_{DD}
V_{IN} Hysteresis	–	–	230	–	mV
Input Pulldown Current	SI, IN0, IN1, IN2, IN3, V_{IN} = 30% V_{DD}	–	–	25	μA
Input Pullup Current	CSB, V_{IN} = 70% V_{DD}	–	–	–25	μA
Status Low	I_{STATUS} = 0.5 mA	–	0.1	0.5	V
Fault Detection/Timing					
Overcurrent Sense Time, t_{SS}	Overcurrent Sense Time, R_{OSC} = 82 kΩ	25	62.5	100	μs
Overcurrent Shutdown Time	Overcurrent Shutdown Time, R_{OSC} = 82 kΩ	1.60	3.94	6.3	ms
Fault Duty Cycle	After the first fault cycle, Note 1.	1.4	1.56	1.7	%
Open Load Trip Point	IN = Low	40	50	60	%V_{DD}
Open Load Sense Time	Open Load Sense Time, R_{OSC} = 82 kΩ	12.5	–	100	μs
Power Outputs					
V_{DRAIN} Clamp	I_D = 20 mA, t_{CLAMP} = 100 μs	48	52	64	V
Drain Leakage Current	V_{DRAIN} = 17 V	–	–	25	μA
Drain Leakage Current	V_{DRAIN} = 46 V	–	–	400	μA
$R_{DS(ON)}$	V_{PWR} = 13 V, I_D = 0.5 A	–	1.0	2.0	Ω
Current Limit	Note 2.	3.0	4.5	6.0	A
Reverse Diode Drop	Reverse Diode Drop I = 350 mA	–	–	1.4	V
Fall Time Delay, t_{phl}	V_{PWR} = 13 V, R_{LOAD} = 33 Ω, Note 3. (see Figure 2)	–	–	10	μs
Rise Time Delay, t_{plh}	V_{PWR} = 13 V, R_{LOAD} = 33 Ω, Note 3. (see Figure 2)	–	–	15	μs
Rise Time, t_r	V_{PWR} = 13 V, R_{LOAD} = 33 Ω	0.4	–	10	μs
Fall Time, t_f	V_{PWR} = 13 V, R_{LOAD} = 33 Ω	0.4	–	10	μs

1. Guaranteed by design.
2. A duty cycle mode will initiate at a minimum of 1.0 A and before the current limit.
3. Output turn on delay and turn off delay from rising edge of CSB to the output reaching 50% of V_{PWR}.

ELECTRICAL CHARACTERISTICS (continued) (9.0 V < V_{PWR} < 17 V, 4.5 V < V_{DD} < 5.5 V, –40°C < T_J < 125°C, 5.5 V < V_{PWR} < 25 V, (Outputs Functional); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Serial Peripheral Interface	V_{PWR} = 14 V				
SCLK Clock Period	C_O = 200 pF	250	–	–	ns
MAX Input Capacitance	SI, SCLK, Note 1.	–	–	12	pF
V_{OUT} High	SO, I_{OH} = 1.0 mA	V_{DD} – 1.0	–	–	V
V_{OUT} Low	SO, I_{OL} = 1.0 mA	–	–	0.5	V
SCLK High Time	F_{SCLK} = 4.0 MHz, SCLK = 2.0 V to 2.0 V (see Figure 1)	125	–	–	ns
SCLK Low Time	F_{SCLK} = 4.0 MHz, SCLK = 0.8 V to 0.8 V (see Figure 1)	125	–	–	ns
SI Setup Time	SI = 0.8 V/2.0 V to SCLK = 2.0 V at 4.0 MHz; Note 1. (see Figure 1)	25	–	–	ns
SI Hold Time	SCLK = 2.0 V to SI = 0.8 V/2.0 V at 4.0 MHz; Note 1. (see Figure 1)	25	–	–	ns
SO Rise Time	C_{LD} = 200 pF (0.1 V_{DD} to 0.9 V_{DD}); Note 1.	–	25	50	ns
SO Fall Time	C_{LD} = 200 pF (0.9 V_{DD} to 0.1 V_{DD}); Note 1.	–	–	50	ns
CSB Setup Time	CSB = 0.8 V to SCLK = 2.0 V (see Figure 1) Note 1.	60	–	–	ns
CSB Hold Time	SCLK = 0.8 V to CSB = 2.0 V (see Figure 1) Note 1.	75	–	–	ns
SO Delay Time	SCLK = 0.8 V to SO Data Valid, V_{DD} = 5.0 V C_{LD} = 200 pF at 4.0 MHz (see Figure 1); Note 1.	–	65	125	ns
Xfer Delay Time	CSB rising edge to next falling edge. Note 1.	1.0	–	–	µs

1. Guaranteed by design.

PACKAGE PIN DESCRIPTION

PACKAGE PIN # 24 Lead SOIC	PIN SYMBOL	FUNCTION
1	V_{DD}	Input voltage to bias logic and control circuitry.
2	V_{PWR}	Input voltage to bias gate drive circuitry.
3	OUT0	Open drain output one.
4	IN0	Parallel input one.
5, 6, 7, 8 17, 18, 19, 20	GND	Ground Reference.
9	IN1	Parallel input two.
10	OUT1	Open drain output two.
11	SI	SPI serial input.
12	CSB	SPI active low chip select.
13	SCLK	SPI clock input.
14	SO	SPI serial output.

PACKAGE PIN DESCRIPTION (continued)

PACKAGE PIN # 24 Lead SOIC	PIN SYMBOL	FUNCTION
15	OUT2	Open drain output three.
16	IN2	Parallel input three.
21	IN3	Parallel input four.
22	OUT3	Open drain output four.
23	STATUS	Open drain output, which is asserted when an open load or overcurrent condition occurs at any of the outputs.
24	R_{OSC}	82 kΩ resistor tied to ground to set up accurate internal current sources.

CIRCUIT DESCRIPTION

Typical Operation

Control of the CS1112 can be done using the Serial Peripheral Interface (SPI) port using the Data Input information in Table 1, or the outputs can be controlled via the parallel inputs (IN0, IN1, IN2, IN3). IN0 controls OUT0, IN1 controls OUT1, IN2 controls OUT2, and IN3 controls OUT3. Turning the output drivers on is an OR function with the SPI input and the parallel inputs.

Note: To prevent damage to the IC or the output load, V_{DD} must be above the Power on Reset threshold (3.5 V) before IN0, IN1, IN2, or IN3 are asserted high (< 70% V_{DD}).

TIMING DIAGRAM

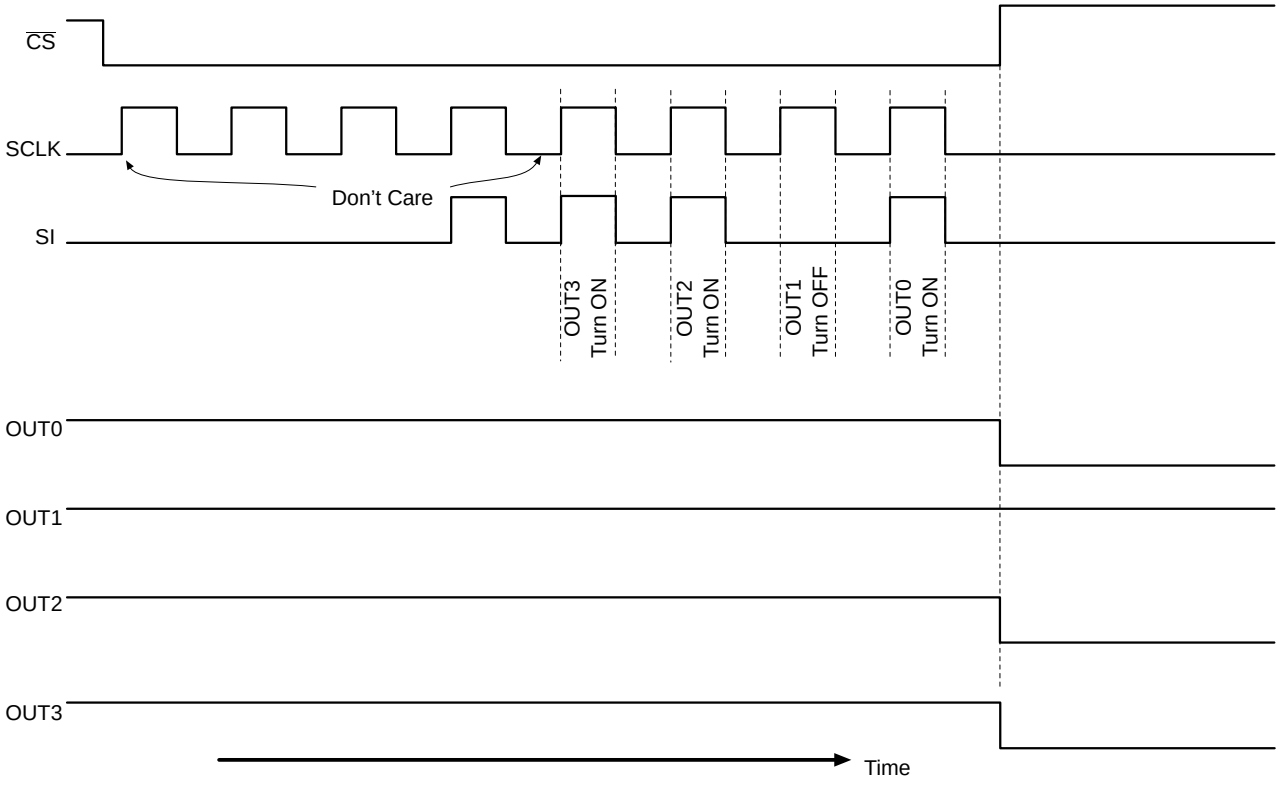


Table 1. SPI Inputs

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	OUT3	OUT2	OUT1	OUT0
MSB							LSB

X = Don't Care; MSB is Transferred first.

SERIAL PERIPHERAL INTERFACE TIMING REQUIREMENTS

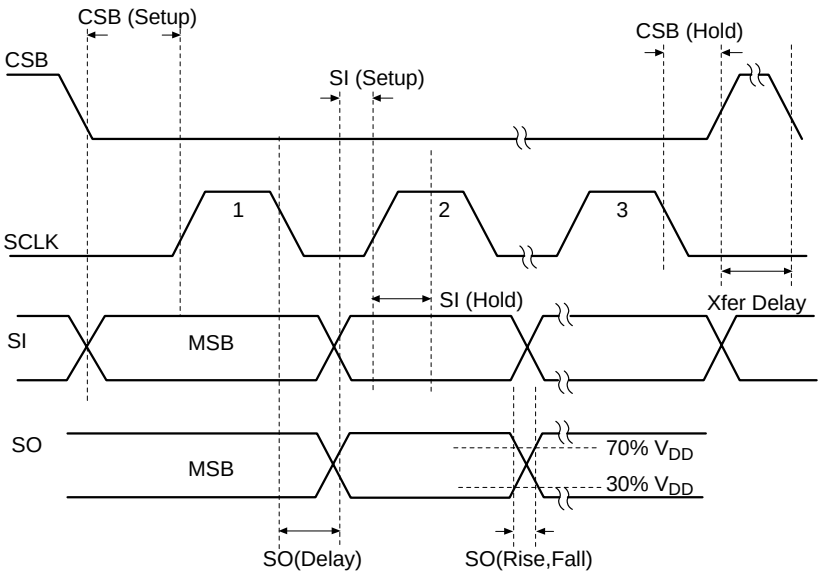


Figure 1.

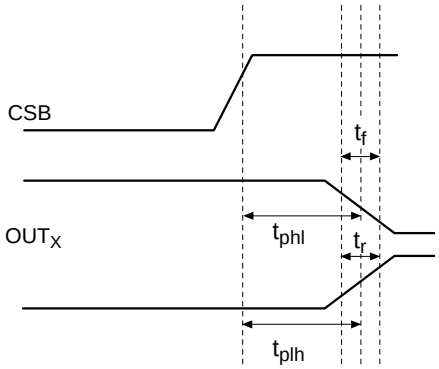
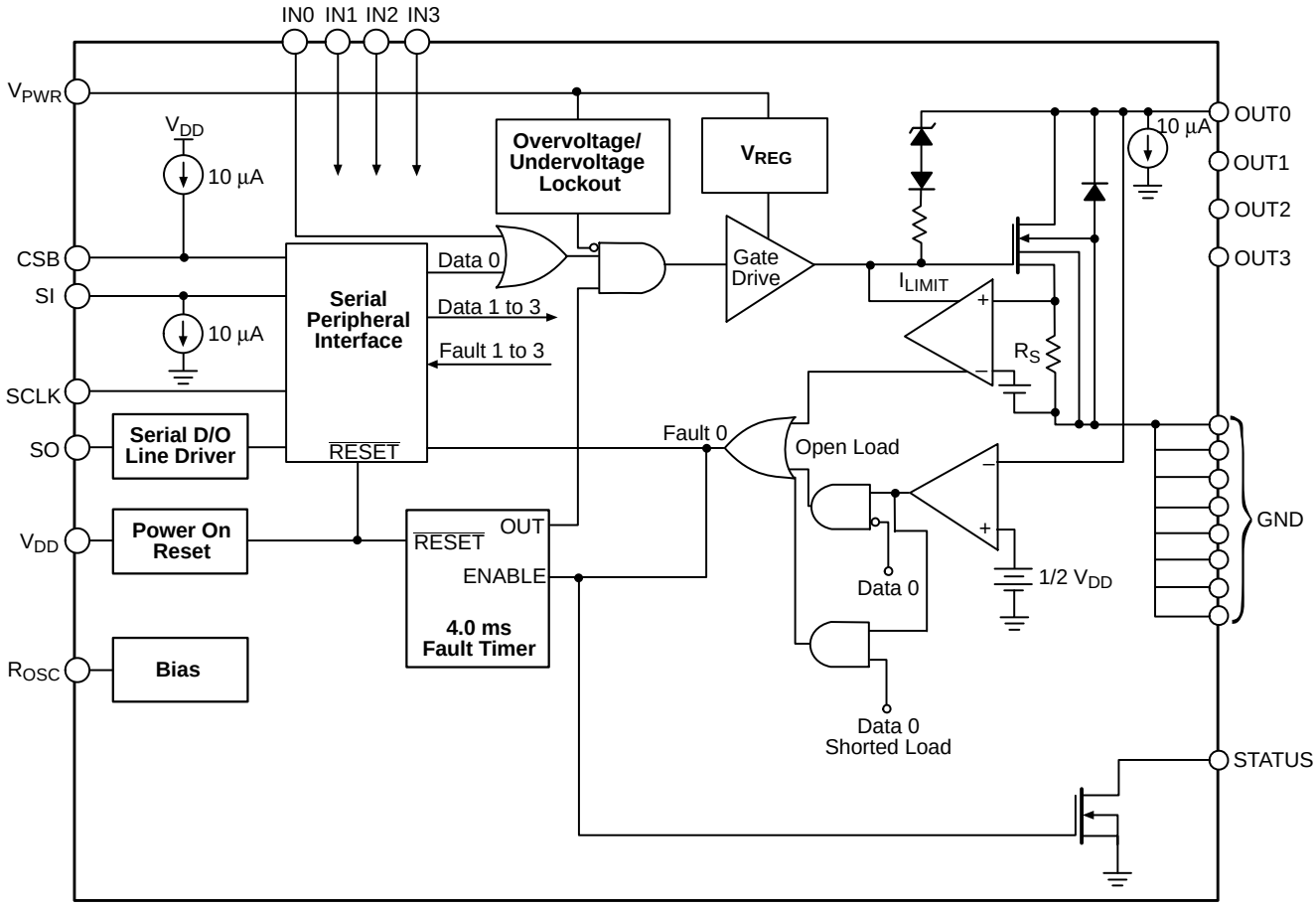


Figure 2.

BLOCK DIAGRAM



APPLICATION INFORMATION

CIRCUIT DESCRIPTION

The CS1112 was developed for use in very noisy and very harsh environments such as seen in an automobile system. The device has four low–side switches all controlled through an 8–bit Serial Peripheral Interface (SPI) port. Control of the outputs is also OR'd with parallel inputs. This is a critical feature enhancement over similar devices because of the ease in which the parallel inputs can be used to control the outputs in a Pulse Width Modulation (PWM) mode. Creating a PWM mode using just the serial port input is not a practical application.

This part uses ON Semiconductor's POWERSENSE™ process technology. POWERSENSE combines the robustness of Bipolar with the dense logic capability of CMOS, and the power capabilities of DMOS.

Power consumption is kept to a minimum using POWERSENSE in comparison to a bipolar technology. A bipolar process requires DC bias currents to power–up the integrated circuit. This is needed in many applications requiring analog circuitry, but is not needed here. Digital POWERSENSE logic dissipates power only when switching because that is when transient gate charging current flows. POWERSENSE logic requires little space, and is a good economical solution. The DMOS side of the process provides a robust user interface to the outside world on each of the outputs. Peak transient capability of each output is rated at a maximum of 46 V (typical of an automotive load dump transient).

The CS1112 uses quasi–vertical DMOS transistors resulting in an output resistance ($R_{DS(ON)}$) at each output of less than 1.0 Ω @ 13 V and 500 mA @ 25°C.

The part can be put in a sleep mode where the part draws less than 2.0 μA of bias current from V_{PWR}. The part enters this sleep mode when $V_{DD} \leq 0.5$ V. Maximum quiescent current for the device is 5.0 mA maximum for any combination of output drivers enabled.

Fault reporting is controlled by the CS1112. Overcurrent and short to V_{BATT} are detected when the output is on. Open load and short to ground are detected when the output is off. Faults are reported out of the serial output (SO) pin as a new 8–bit word is being fed into the serial input (SI) pin.

Figure 3 highlights the SPI interface between the microprocessor and the CS1112. The SPI control inputs and all other logic inputs are compatible with 5.0 V CMOS logic levels.

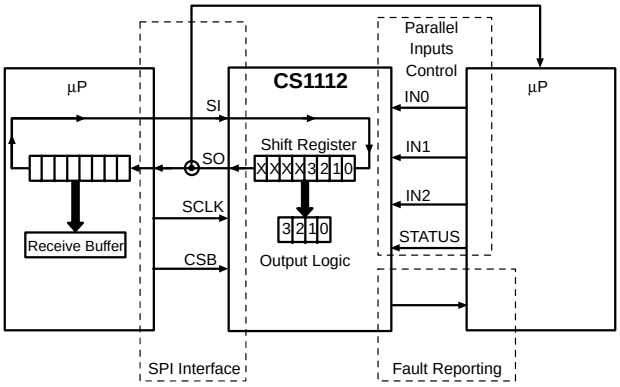


Figure 3.

The four communication lines which define the SPI interface are the SI, SO, CSB, and SCLK. The parallel inputs, which control the outputs can also connect to the same microprocessor, a separate microprocessor, or any other sensor or electrical device which meets the voltage requirements of the CS1112 ($V_{IN(max)} = V_{DD} + 0.3$ V).

SPI communication is as follows (2 scenarios):

1. **8–Bit Normal Operation**
   CSB pin is brought low activating the SPI port. Faults detected since the last CSB low to high transition are latched into the serial register when CSB goes low. 8 command bits are clocked into the SI pin. The four fault bits are clocked out of the SO pin. CSB pin is brought high translating the final 4 bits to the outputs turning them on or off. Faults are then detected and saved in the fault register when CSB goes low.
2. **16–Bit Operation For Command Verify**
   CSB pin is brought low activating the SPI port. 16 bits are clocked into the SI pin (the last 4 are the 4 control pins for the four outputs). CSB pin is brought high translating the last 4 bits to the outputs turning them on or off.
   CSB pin is brought low activating the SPI port. 16 new bits are clocked into the SI pin. As the new bits are being clocked in, the first 8 bits being clocked out of the SO pin are the fault bits, followed by the first 8 bits which were clocked in (the verification bits). The verification bits should replicate the command bits.

Serial clock frequencies up to 4.0 MHz can be used by the CS1112.

Internal pull–up circuitry is provided on the Chip Select Bar (CSB) pin. Internal active pulldowns are provided on the parallel input pins (IN0, IN1, IN2, IN3, and SI pin).

A product highlight of this part is its ability to be daisy–chained with other parts which follow the SPI protocol as defined in Figure 1. Figure 4 displays this aspect. The serial output of each device is fed into the serial input of the next device. All data bits are clocked into their respective registers, while the CSB pin is low. The drivers are switched to the resulting command when the CSB pin is brought back high.

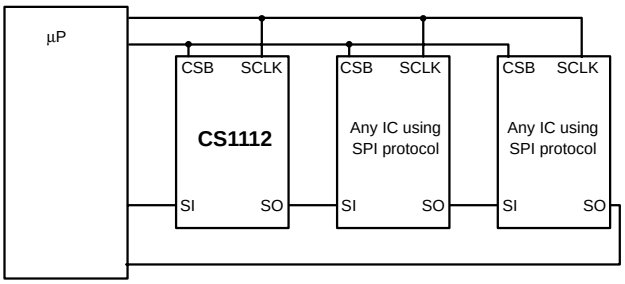


Figure 4.

Multiple SPI port devices can also be connected in a parallel fashion (Figure 5) instead of the daisy–chained connection previously shown. The microprocessor controls the CS1112 in a multiplex fashion allowing the serial data input to be input to the device when the device is activated through the CSB pin. This creates a system whose number of outputs is a multiple of 4. Figure 5 displays a 12 output setup.

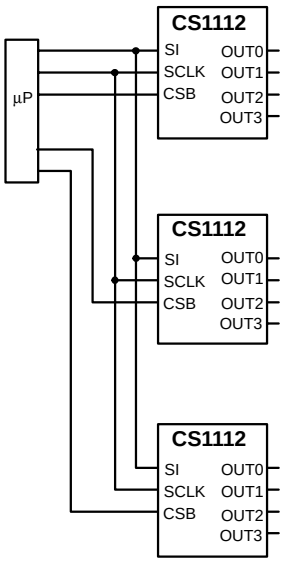


Figure 5.

Figure 6 displays the device controlling 4 outputs with the use of its SPI port. Figure 7 displays the device controlling 1 output with the SPI port, and 3 outputs being controlled with the parallel inputs allowing them to run in a PWM mode.

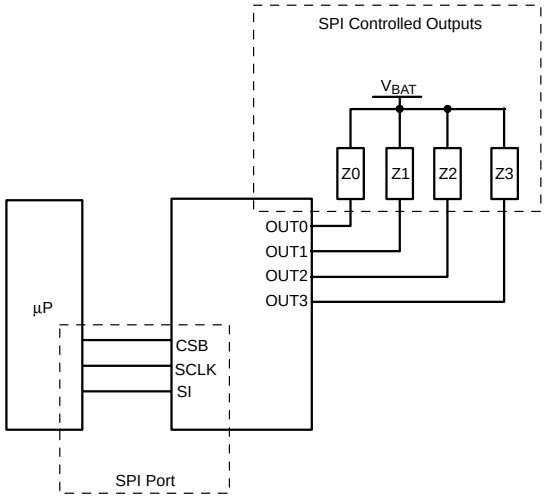


Figure 6.

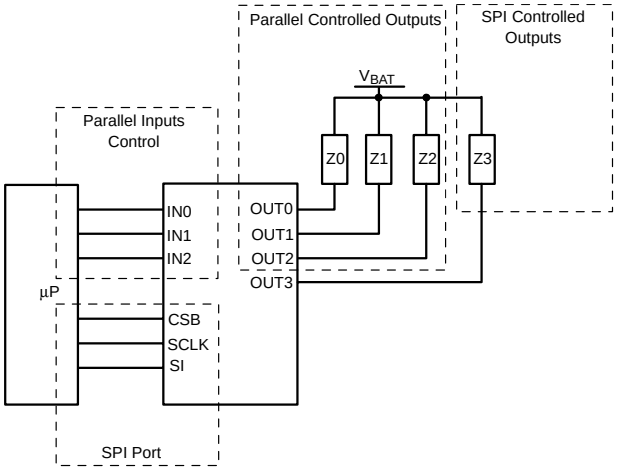


Figure 7.

The CS1112 provides a very efficient way of controlling 4 output drivers by minimizing the number of I/O pins through use of the SPI port, and still provides the flexibility of pulse width modulating the output drivers where needed. The use of the SPI also allows the integrated circuit to communicate directly with the microprocessor.

While designed for an automotive environment, the CS1112 can be used in other applications in the computer market, industrial market, telecommunications market, or any other instance where numerous drivers are needed. All parts are 100% tested and guaranteed to meet all parameters specified in the electrical characteristics. These specifications cover the entire voltage range for V_{PWR} (9.0 V to 17 V), and V_{DD} (4.5 V to 5.5 V).

FAULT MODE OPERATION

The CS1112 provides protection for a multitude of system faults and conditions. These include Overvoltage, Current Limit, Open Circuit, Output Short to Power, Output Short to Ground, and Flyback Clamp.

Overvoltage

The IC is constantly monitoring the voltage on the V_{PWR} pin. If the voltage on this pin exceeds the Overvoltage Shutdown Threshold (typically 35 V), all outputs immediately turn off. The programmed outputs (via serial or parallel input) turn back on once the voltage is brought back down below this level.

Current Limit/Short to V_{BATT}

When the output current exceeds the Overcurrent (4.5 A typical) for the Short Circuit/Overcurrent Sense Time (typically 62.5 μs) as it would do during an output short to V_{BATT}, its fault status bit will be latched to a logic one. The fault status bit remains latched until the rising edge of CSB. The output will go into a low duty cycle mode (typically 1.56%) as long as the overcurrent condition exists, and the channel is on. This protects the integrated circuit from damaging itself due to its thermal limits.

Open Circuit/Short to Ground

Open circuit conditions are detected while the outputs are off. A fault bit is set when the Open Load “Off” Detection Voltage (typically $0.5 \times V_{DD}$) is present for the Open Load “Off” Sense Time (typically 62.5 μs) as it would do during an output short to ground.

Flyback Clamp

While the flyback clamp is not a fault mode, it is a protection feature of the CS1112. When driving inductive loads, it is normal to observe high voltage spikes on the output pin due to the stored energy in the windings when the device is turned off. On–chip clamps on the outputs limit the voltage amplitude on the pin to prevent damage to the device. Each output has an Output Clamp which limits the output voltage to 52 V (typical when measured at 20 mA for 100 μs).

PIN FUNCTION DESCRIPTION

SI

The SI (Serial Input) receives serial 8–bit or 16–bit words sent most significant bit first. Data is clocked in on the rising edge of SCLK. An internal active pull–down is connected to this input. CMOS logic levels are required on this pin.

SO

The SO (Serial Output) can be connected to the serial data input pin of the microprocessor, or it can be daisy–chained to the serial input (SI) of another SPI compatible device. This pin is tri–stated unless a low CSB pin selects the device. The signal on this pin is clocked from the falling edge of the SCLK pin. The serial output data provides fault information for each output and returns most significant bit (bit 7) first. Bits 0 through 3 are output fault bits for outputs 0 through 3, respectively. In 8–bit SPI mode, bits 0–3, under normal conditions return all zeros representing no faults. A 1 indicates a fault. The output from this pin conforms to CMOS logic levels.

R_{OSC}

An 82 kΩ resistor tied to ground sets up an accurate internal current source.

CSB

The CSB (Chip Select Bar) is the select pin when the microprocessor wants to communicate with the CS1112. A low on this pin enables the SPI communication with the device and enables the SO pin. After the digital word is clocked into the IC, a transition from low to high on the CSB pin translates the last 4 bits of information turning the outputs on or off. An internal active pull–up is connected to this input. CMOS logic levels are required on this pin.

SCLK

The SCLK (Serial Clock) clocks the internal shift registers. This pin controls the data being shifted into the SI pin, and data being shifted out of the SO pin. CMOS logic levels are required on this pin.

IN0, IN1, IN2, IN3

These pins control their corresponding numbered output. These are the parallel input pins which may be used to PWM the outputs. They have 230 mV of hysteresis. These inputs are OR’d with their corresponding input bit in the serial control byte. An internal active pull–down is connected to these pins. CMOS logic levels are required on these pins.

OUT0, OUT1, OUT2, OUT3

These pins are the output low–side driver pins. They all have typically 1.0 Ω $R_{DS(ON)}$ at V_{PWR} = 13 V. Current limit on these pins has a minimum specification of 3.0 A. A low duty cycle mode (1.5% typ.) will initiate at a minimum of 1A and before the current limit.

V_{PWR}

14 V Battery voltage input. 5.0 mA (max) is needed.

V_{DD}

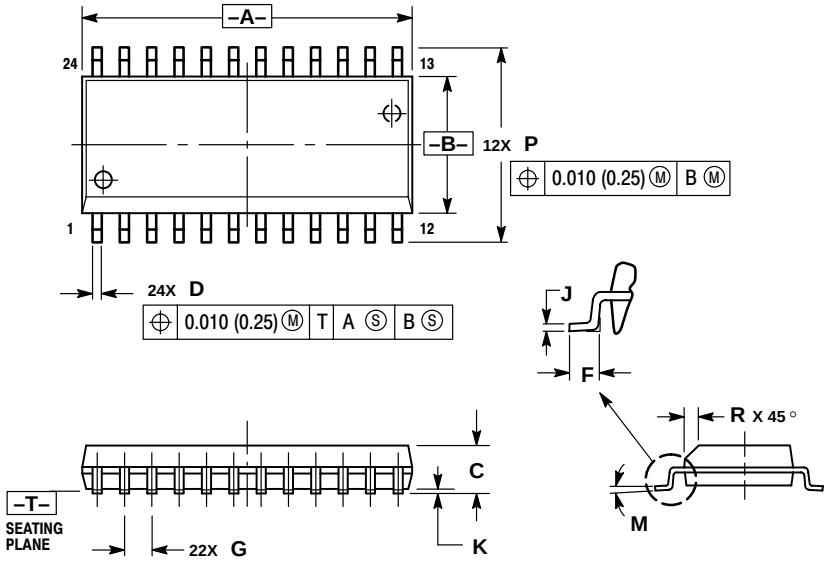
5.0 V Supply input. 5.0 mA (max) is needed.

STATUS

Open drain output. This pin goes low when an open load or overcurrent condition occurs on any of the outputs. This provides immediate notification to the controller that a fault is present. The controller can subsequently query the device (serially) to determine its origin.

PACKAGE DIMENSIONS

SO–24L
DW SUFFIX
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PACKAGE THERMAL DATA

Parameter		SO–24L	Unit
$R_{\Theta JC}$	Typical	9	°C/W
$R_{\Theta JA}$	Typical	55	°C/W

Notes

POWERSENSE is a trademark of Semiconductor Components Industries, LLC (SCILLC).

PUBLICATION ORDERING INFORMATION

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