This version: Aug. 1998

OKI Semiconductor

ML7000-01/02/03
ML7001-01/02/03

Single Rail CODEC

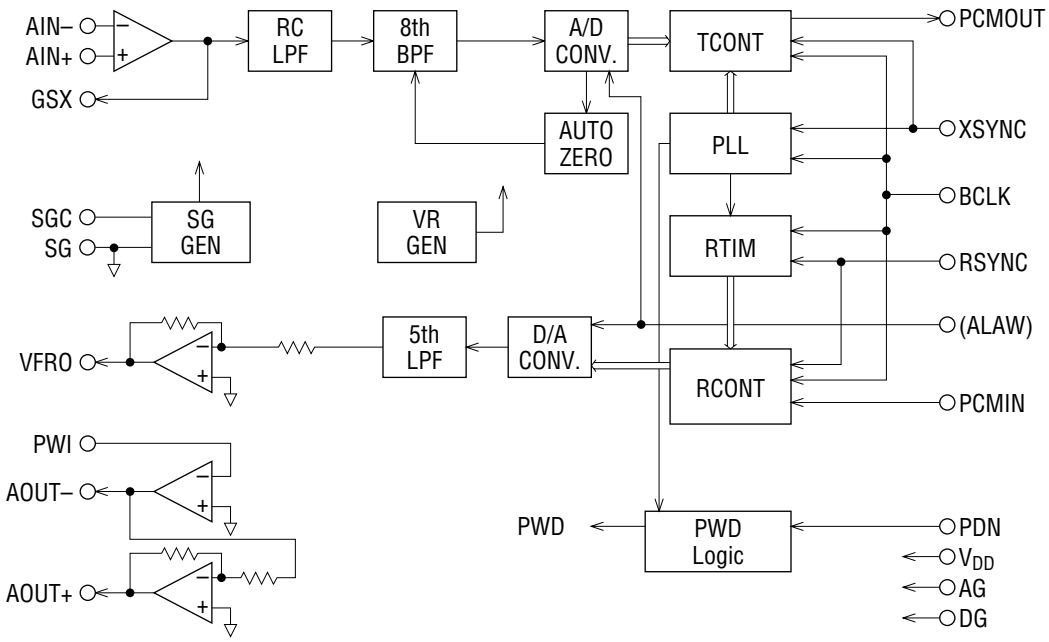
GENERAL DESCRIPTION

The ML7000/ML7001 are single-channel CMOS CODEC LSI devices for voice signals ranging from 300 to 3400 Hz with filters for A/D and D/A conversion.
Designed especially for a single-power supply and low-power applications, the devices are optimized for ISDN terminals, digital wireless systems, and digital PBXs.
The devices use the same transmission clocks as those used in the MSM7507.
With the differential analog signal outputs which can drive 60 Ω load, the devices can directly drive a handset receiver.

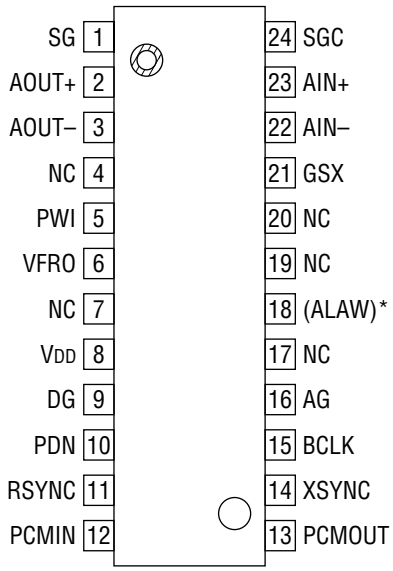
FEATURES

- Single power supply: +5 V (ML7000-xx)
  +3 V (ML7001-xx)
- Low power consumption
  Operating mode: 25 mW Typ. V_{DD} = 5.0 V (ML7000-xx)
  20 mW Typ. V_{DD} = 3.0 V (ML7001-xx)
  Power-down mode: 0.05 mW Typ. V_{DD} = 5.0 V (ML7000-xx)
  0.03 mW Typ. V_{DD} = 3.0 V (ML7001-xx)
- Conforms to ITU-T Companding law
  ML7000-01/ML7001-01: μ/A-law pin selectable
  ML7000-02/ML7001-02: μ-law
  ML7000-03/ML7001-03: A-law
- Transmission characteristics conform to ITU-T G.714
- Short frame sync timing operation
- Built-in PLL eliminates a master clock
- Serial data rate: 64/96/128/192/200/256/384/512/
  768/1024/1536/1544/2048 kHz
- Adjustable transmit gain
- Adjustable receive gain
- Built-in reference voltage supply
- Package options:
  24-pin plastic SOP (SOP24-P-430-1.27-K) (Product name: ML7000-01MA/ML7001-01MA)
  (Product name: ML7000-02MA/ML7001-02MA)
  (Product name: ML7000-03MA/ML7001-03MA)
  20-pin plastic SSOP (SSOP20-P-250-0.95-K) (Product name: ML7000-01MB/ML7001-01MB)
  (Product name: ML7000-02MB/ML7001-02MB)
  (Product name: ML7000-03MB/ML7001-03MB)

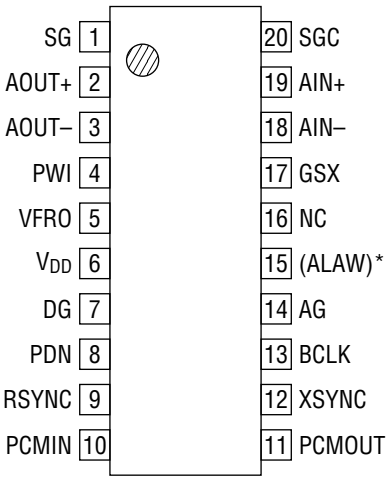
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



24-Pin Plastic SOP



20-Pin Plastic SSOP

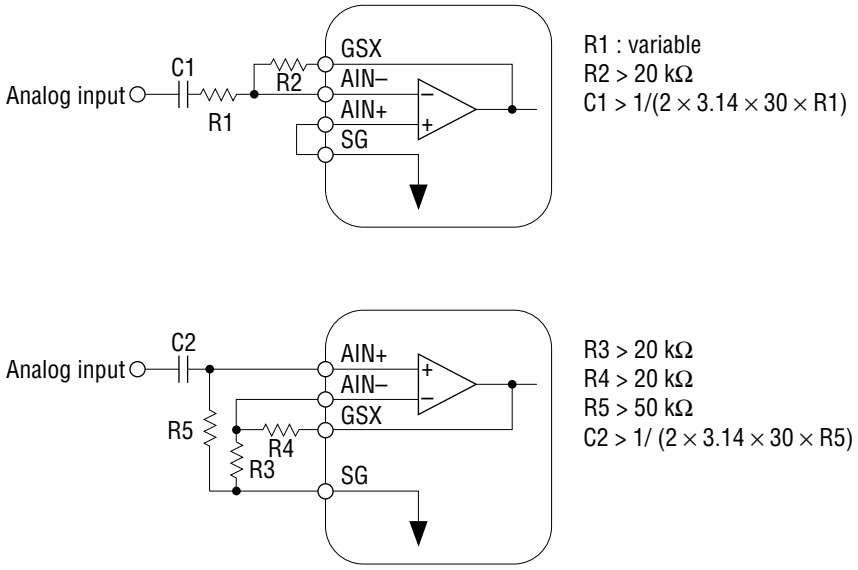
* The ALAW pin is only supported by the ML7000-01MA/ML7000-01MB/ML7001-01MA/ML7001-01MB.

NC : No connect pin

PIN FUNCTIONAL DESCRIPTION

AIN+, AIN–, GSX

Transmit analog input and transmit level adjustment.
AIN+ is a non-inverting input to the op-amp; AIN– is an inverting input to the op-amp; GSX is connected to the output of the op-amp.
The level adjustment should be performed using any of the methods shown below. During power-saving and power-down modes, the GSX output is at AG voltage.



AG

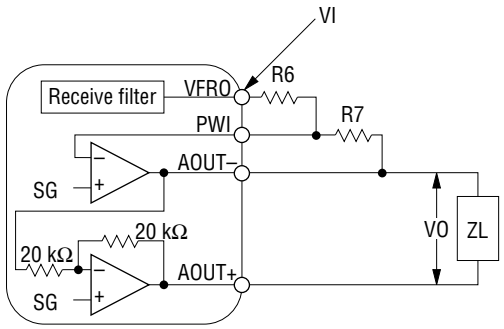
Analog ground.

VFRO

Receive filter output.
The output signal has an amplitude of 2.4 V_{PP} for ML7000-xx and 2.0 V_{PP} for ML7001-xx above and below the signal ground voltage (SG) when the digital signal of +3 dBm0 is input to PCMIN and can drive a load of 20 kΩ or more.
For driving a load of less than 20 kΩ, connect a resistor of 20 kΩ or more between the pins VFRO and PWI.
During power-saving or power-down mode, the VFRO output is at an SG level.
When adjusting the receive signal on the basis of frequency characteristics, refer to the Frequency Characteristics Adjustment Circuit.

PWI, AOUT+, AOUT–

PWI is connected to the inverting input of the receive driver.
The receive driver output is connected to the AOUT– pin. Therefore, the receive level can be adjusted with the pins VFRO, PWI, and AOUT–. During power-saving or power down-mode, the outputs of AOUT+ and AOUT– are in a high impedance state. The output of AOUT+ is inverted with respect to the output of AOUT–. Since these outputs provide differential drive of an impedance of 1.2 kΩ, they can directly be connected to a handset using a piezoelectric earphone or a line transformer. Refer to the application example.



R6 > 20 kΩ
ZL > 1.2 kΩ

Gain = VO/VI = 2 × R7/R6 ≤ 2

V_{DD}

Power supply for +5 V (ML7000-xx) or +3 V (ML7001-xx)

PCMIN

PCM data input.
A serial PCM data input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLK signal.
The data rate of PCM is equal to the frequency of the BCLK signal.
PCM signal is shifted in at the falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.
The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

BCLK

Shift clock signal input for the PCMIN and PCMOUT signals.
The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, or 2048 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.
Eight required bits are selected from serial PCM signals on the PCMIN pin by the receive synchronizing signal.
Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK. The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the receive section.
However, if the frequency characteristic of an applied system is not specified exactly, this device can operate in the range of 6 to 9 kHz, but the electrical characteristics in this specification are not guaranteed.

XSYNC

Transmit synchronizing signal input.
The PCM output signal from the PCMOUT pin is output in synchronization with this signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section. This synchronizing signal must be synchronized in phase with BCLK.
The frequency should be 8 kHz ±50 ppm to guarantee the AC characteristics which are mainly the frequency characteristics of the transmit section. However, if the frequency characteristic of an applied system is not specified exactly, this device operates in the range of 6 to 9 kHz, but the electrical characteristics in this specification are not guaranteed.
Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

DG

Ground for the digital signal circuits.
This ground is separate from the analog signal ground AG. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground AG.

PDN

Power down control signal.
A logic "0" level drives both transmit and receive circuits to a power down state.

PCMOUT

PCM signal output.
Synchronizing with the rising edge of the BCLK signal, the PCM output signal is output from MSD in a sequential order.
MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.
This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down mode.
A pull-up resistor must be connected to this pin because its output is configured as an open drain.
This device is compatible with the ITU-T recommendation on coding law and output coding format.
The ML7000-03 (A-law) and ML7001-03 (A-law) output the character signal, inverting the even bits.

Input/Output Level	PCMIN/PCMOUT	
	ML7000-02 (μ-law) ML7001-02 (μ-law)	ML7000-03 (A-law) ML7001-03 (A-law)
+Full scale	MSD LSD 1 0 0 0 0 0 0 0	MSD LSD 1 0 1 0 1 0 1 0
+0	1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1
–0	0 1 1 1 1 1 1 1	0 1 0 1 0 1 0 1
–Full scale	0 0 0 0 0 0 0 0	0 0 1 0 1 0 1 0

SG

Signal ground voltage output.
The output voltage is 1/2 of the power supply voltage.
The output drive current capability is ±300 µA for ML7000-xx and ±200 µA for ML7001-xx.
This pin provides the SG level for CODEC peripherals.
This output voltage level is undefined during power-saving or power-down mode.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor.
Connect a 0.1 µF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

ALAW

Control signal input of the companding law selection.
Only the ML7000-01MA/ML7000-01MB/ML7001-01MA/ML7001-01MB have this pin. The CODEC will operate in the µ-law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the µ-law if the pin is left open, since the pin is internally pulled down.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +7	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	4.75	5.00	5.25	V
			2.70	3.00	3.30	
Operating Temperature	Ta	—	–30	+25	+85	°C
Analog Input Voltage	V_{AIN}	Connect AIN– and GSX	—	—	2.4	V_{PP}
			—	—	1.2	
High Level Input Voltage	V_{IH}	XSYNC, RSYNC, BCLK, PCMIN, PDN, ALAW	2.2	—	V_{DD}	V
			0.45×V_{DD}	—	V_{DD}	
Low Level Input Voltage	V_{IL}		0	—	0.8	V
			0	—	0.16×V_{DD}	
Clock Frequency	F_C	BCLK	64, 96, 128, 192, 200, 256, 384, 512, 768, 1024, 1536, 1544, 2048			kHz
Sync Pulse Frequency	F_S	XSYNC, RSYNC (–40 to +75 °C)	6.0	8.0	9.0	kHz
			6.0	8.0	10.0	
Clock Duty Ratio	D_C	BCLK	40	50	60	%
Digital Input Rise Time	t_{lr}	XSYNC, RSYNC, BCLK, PCMIN, PDN	—	—	50	ns
Digital Input Fall Time	t_{lf}		—	—	50	ns
Transmit Sync Pulse Setting Time	t_{CX}	BCLK→XSYNC, See Fig. 1	50	—	—	ns
	t_{XC}	XSYNC→BCLK, See Fig. 1	50	—	—	ns
XSYNC Setup Time	t_{XS}	—	50	—	—	ns
XSYNC Hold Time	t_{XH}	—	50	—	—	ns
Receive Sync Pulse Setting Time	t_{CR}	BCLK→RSYNC, See Fig. 1	50	—	—	ns
	t_{RC}	RSYNC→BCLK, See Fig. 1	50	—	—	ns
RSYNC Setup Time	t_{RS}	—	50	—	—	ns
RSYNC Hold Time	t_{RH}	—	50	—	—	ns
PCMIN Setup Time	t_{DS}	—	50	—	—	ns
PCMIN Hold Time	t_{DH}	—	50	—	—	ns
Digital Output Load	R_{DL}	Pull-up resistor	0.5	—	—	kΩ
	C_{DL}	—	—	—	100	pF
Analog Input Allowable DC Offset	V_{off}	Transmit gain stage, Gain = 0 dB	–10	—	+10	mV
		Transmit gain stage, Gain = +20 dB	–100	—	+100	mV
Allowable Jitter Width	—	XSYNC, RSYNC, BCLK	—	—	1000	ns

Values above the dotted line are for ML7000-xx; those below, for ML7001-xx.

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(ML7001-xx: V_{DD} = 2.7 V to 3.3 V, Ta = –30 to +85°C)
(ML7000-xx: V_{DD} = +5.0 V ±5%, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode	V_{DD} = 5.0 V	—	5.0	12.0	mA
		No signal	V_{DD} = 3.0 V	—	6.5	10.0	
	I_{DD2}	Power-saving mode, PDN = 1, XSYNC → OFF		—	1.5	4.0	mA
				—	2.0	8.0	
	I_{DD3}	Power-down mode, PDN = 0, BCLK OFF		—	0.01	0.05	mA
High Level Input Voltage	V_{IH}	—		2.2	—	V_{DD}	V
				0.45×V_{DD}	—	V_{DD}	
Low Level Input Voltage	V_{IL}	—		0.0	—	0.8	V
				0.0	—	0.16×V_{DD}	
High Level Input Leakage Current	I_{IH}	—		—	—	2.0	µA
High Level Input Leakage Current	I_{IH2}	ALAW		—	—	30.0	µA
Low Level Input Leakage Current	I_{IL}	—		—	—	0.5	µA
Digital Output Low Voltage	V_{OL}	Pull-up resistor = 500 Ω		0.0	0.2	0.4	V
Digital Output Leakage Current	I_O	—		—	—	10	µA
Input Capacitance	C_{IN}	—		—	5	—	pF

Values above the dotted line are for ML7000-xx; those below, for ML7001-xx.

Transmit Analog Interface Characteristics

(ML7001-xx: V_{DD} = 2.7 V to 3.3 V, Ta = –30 to +85°C)
(ML7000-xx: V_{DD} = +5.0 V ±5%, Ta = –30 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN+, AIN–		10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX with respect to SG		20	—	—	kΩ
Output Load Capacitance	C_{LGX}			—	—	30	pF
Output Amplitude	V_{OGX}			–1.2	—	+1.2	V0p
				–0.7	—	+0.7	
Offset Voltage	V_{OSGX}		Gain = 1	–20	—	+20	mV

Values above the dotted line are for ML7000-xx; those below, for ML7001-xx.

Receive Analog Interface Characteristics

(ML7001-xx: V_{DD} = 2.7 V to 3.3 V, Ta = –30 to +85°C)
(ML7000-xx: V_{DD} = +5.0 V ±5%, Ta = –30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INPW}	PWI	10	—	—	MΩ
Output Load Resistance	R_{LVF}	VFRO with respect to SG	20	—	—	kΩ
	R_{LAO}	AOUT+, AOUT– (each) with respect to SG	0.6	—	—	kΩ
Output Load Capacitance	C_{LVF}	VFRO	—	—	30	pF
	C_{LAO}	AOUT+, AOUT–	—	—	50	pF
Output Amplitude	V_{OVF}	VFRO, R_L = 20 kΩ with respect to SG	–1.2	—	+1.2	V0p
			–1.0	—	+1.0	
	V_{OAO}	AOUT+, AOUT–, R_L = 0.6 kΩ with respect to SG	–1.3	—	+1.3	
			–1.0	—	+1.0	
Offset Voltage	V_{OSVF}	VFRO with respect to SG	–100	—	+100	mV
	V_{OSAO}	AOUT+, AOUT–, Gain = 1 with respect to SG	–100	—	+100	mV

Values above the dotted line are for ML7000-xx; those below, for ML7001-xx.

AC Characteristics

(ML7001-xx: F_S = 8 kHz, V_{DD} = 2.7 V to 3.3 V, Ta = –30 to +85°C)
(ML7000-xx: F_S = 8 kHz, V_{DD} = +5.0 V ±5%, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Transmit Frequency Response	Loss T1	60	0		20	26	—	dB
	Loss T2	300			–0.15	+0.07	+0.2	
	Loss T3	1020			Reference			
	Loss T4	2020			–0.15	–0.04	+0.2	
	Loss T5	3000			–0.15	+0.07	+0.2	
	Loss T6	3400			0	0.4	0.8	
Receive Frequency Response	Loss R1	300	0		–0.15	–0.03	+0.2	dB
	Loss R2	1020			Reference			
	Loss R3	2020			–0.15	0.00	+0.2	
	Loss R4	3000			–0.15	+0.05	+0.2	
	Loss R5	3400			0	0.54	0.8	
Transmit Signal to Distortion Ratio	SD T1	1020	3	*1	35	43	—	dB
	SD T2		0		35	41	—	
	SD T3		–30		35.0	38.0	—	
					34.0	38.0	—	
	SD T4		–40		26.0	31.0	—	
					26.0	30.0	—	
	SD T5		–45		24.0	25.0	—	
					—	25.0	—	
Receive Signal to Distortion Ratio	SD R1	1020	3	*1	36	43	—	dB
	SD R2		0		36	41	—	
	SD R3		–30		36.0	40.0	—	
					35.0	40.0	—	
	SD R4		–40		25.0	32.0	—	
					26.0	32.0	—	
	SD R5		–45		25.0	27.0	—	
					—	27.0	—	
Transmit Gain Tracking	GT T1	1020	3		–0.3	+0.01	+0.3	dB
	GT T2		–10		Reference			
	GT T3		–40		–0.3	–0.05	+0.3	
	GT T4		–50		–0.6	–0.05	+0.6	
	GT T5		–55		–1.2	–0.08	+1.2	
Receive Gain Tracking	GT R1	1020	3		–0.3	–0.06	+0.3	dB
	GT R2		–10		Reference			
	GT R3		–40		–0.3	+0.08	+0.3	
	GT R4		–50		–0.6	+0.12	+0.6	
	GT R5		–55		–1.2	+0.15	+1.2	

*1 Psophometric filter is used.

Values above the dotted line are for ML7000-xx; those below, for ML7001-xx.

AC Characteristics (Continued)

(ML7001-xx: F_S = 8 kHz, V_{DD} = 2.7 V to 3.3 V, Ta = –30 to +85°C)
(ML7000-xx: F_S = 8 kHz, V_{DD} = +5.0 V ±5%, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Idle Channel Noise	Nidle T	—	—	AIN = SG	—	–73.0	–66.0	dBm0p
				*1 *2	—	–69.5	–65.0	
	Nidle R	—	—	*1 *2	—	–78.0	–71.0	
					—	–75.0	–65.0	
Absolute Level (Initial Difference)	AV T	1020	0	V_{DD} = 5.0 V, Ta = 25°C	0.58	0.6007	0.622	Vrms
				V_{DD} = 3.0 V, Ta = 25°C	0.338	0.35	0.362	
	AV R			*3	0.58	0.6007	0.622	
					0.483	0.5	0.518	
Absolute Level (Deviation of Temperature and Power)	AV Tt	V_{DD} = 5 V ±5%, Ta = –30 to 85°C *3			–0.2	—	0.2	dB
	AV Rt	V_{DD} = 2.7 to 3.3 V, Ta = –30 to 85°C *3			–0.2	—	0.2	
Absolute Delay	Td	1020	0	A to A BCLK = 64 kHz	—	—	0.6	ms
Transmit Group Delay	t_{GD} T1	500	0	*4	—	0.19	0.75	ms
	t_{GD} T2	600			—	0.11	0.35	
	t_{GD} T3	1000			—	0.02	0.125	
	t_{GD} T4	2600			—	0.05	0.125	
	t_{GD} T5	2800			—	0.07	0.75	
Receive Group Delay	t_{GD} R1	500	0	*4	—	0.00	0.75	ms
	t_{GD} R2	600			—	0.00	0.35	
	t_{GD} R3	1000			—	0.00	0.125	
	t_{GD} R4	2600			—	0.09	0.125	
	t_{GD} R5	2800			—	0.12	0.75	
Crosstalk Attenuation	CR T	1020	0	TRANS → RECV	—	–85	–75	dB
	CR R			RECV → TRANS	—	–76	–70	

*1 Psophometric filter is used.
*2 Input "0" code to PCMIN.
*3 AVR is defined at VFRO output.
*4 With respect to minimum value of the group delay distortion.

Values above the dotted line are for ML7000-xx; those below, for ML7001-xx.

AC Characteristics (Continued)

(ML7001-xx: F_S = 8 kHz, V_{DD} = 2.7 V to 3.3 V, Ta = –30 to +85°C)
(ML7000-xx: F_S = 8 kHz, V_{DD} = +5.0 V ±5%, Ta = –30 to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 kHz to 72 kHz	0	0 to 4000 Hz	30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz	—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fd = 320	–4	2fa – fb	—	–52	–35	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{PP}	Measured inband *5	—	30	—	dB
	PSR R							
Digital Output Delay Time	t_{XD1}	C_L = 100 pF + 1 LSTTL			20	—	200	ns
	t_{XD2}	Pull-up resistor = 500 Ω			20	—	200	

*5 Measured under idle channel noise.

TIMING DIAGRAM

PCM Data Input/Output Timing

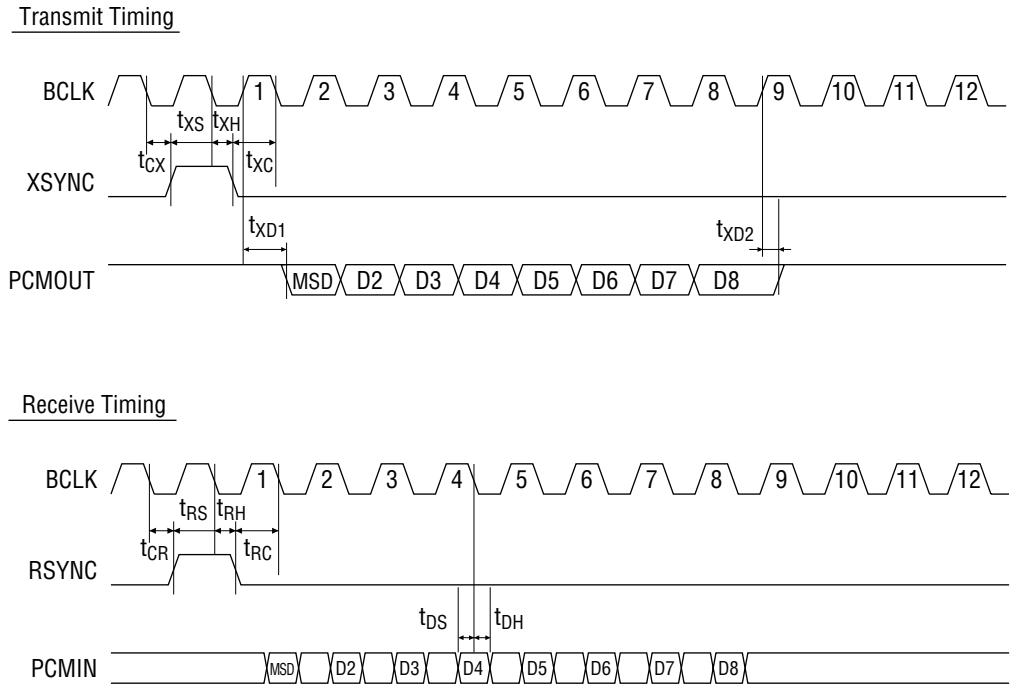
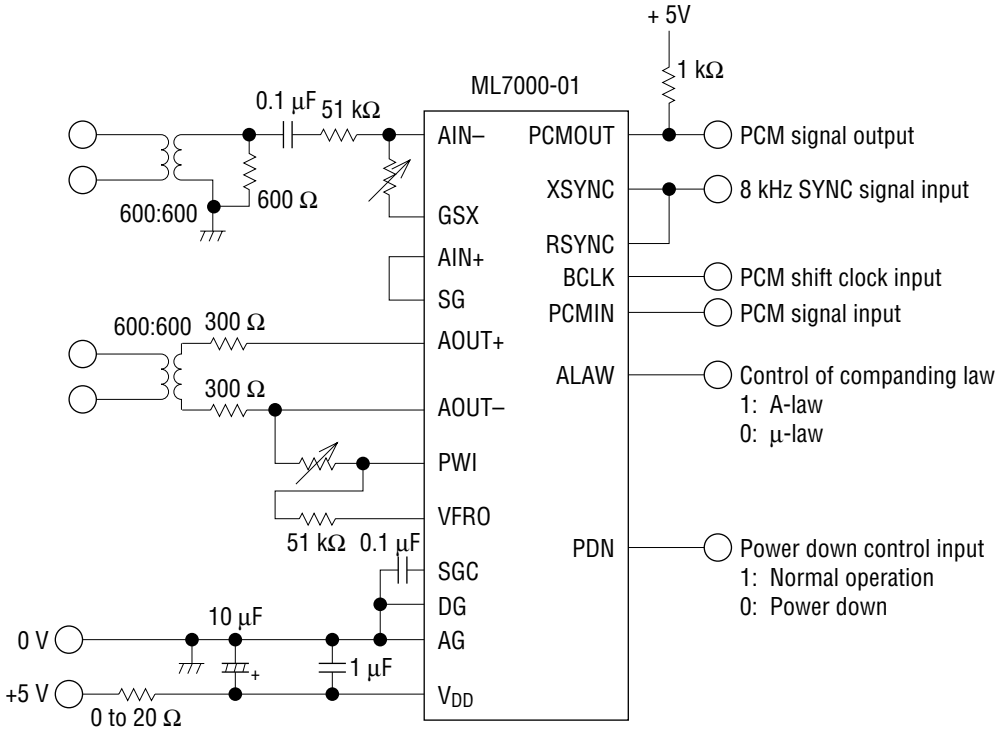
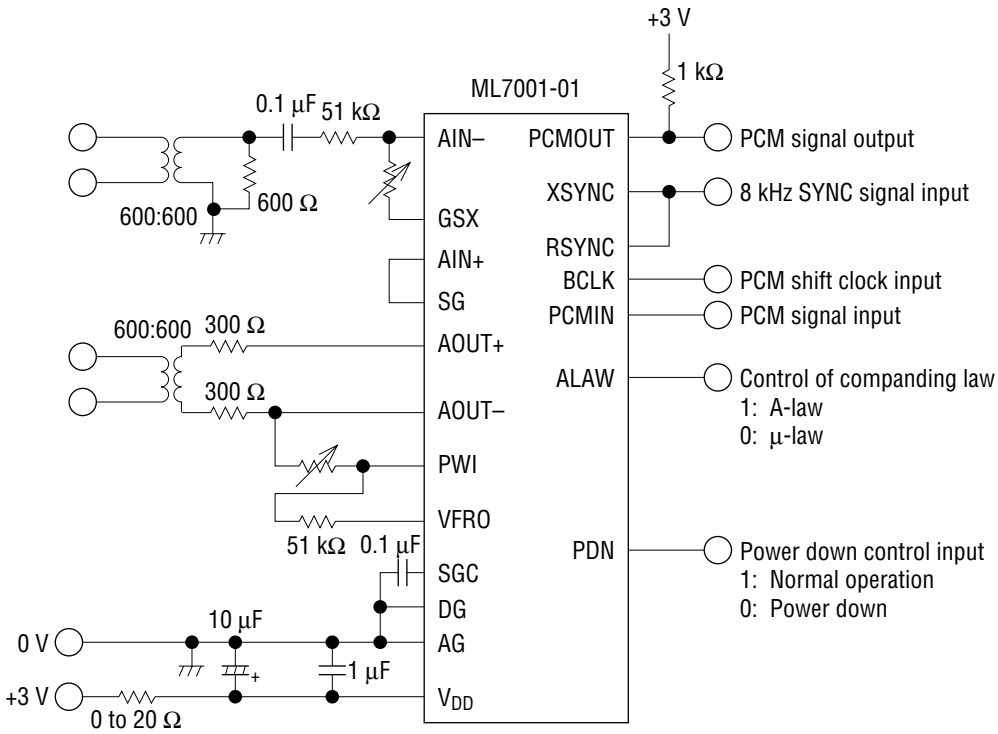


Figure 1 Basic Timing

APPLICATION CIRCUIT





NOTES ON USE

- To ensure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.

- Connect the AG pin and the DG pin as closely as possible. Connect to the system ground with low impedance.

- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If the use of IC socket is unavoidable, use the short lead type socket.

- When mounted on a frame, use electromagnetic shielding if any electromagnetic wave sources such as power supply transformers surrounds the device.

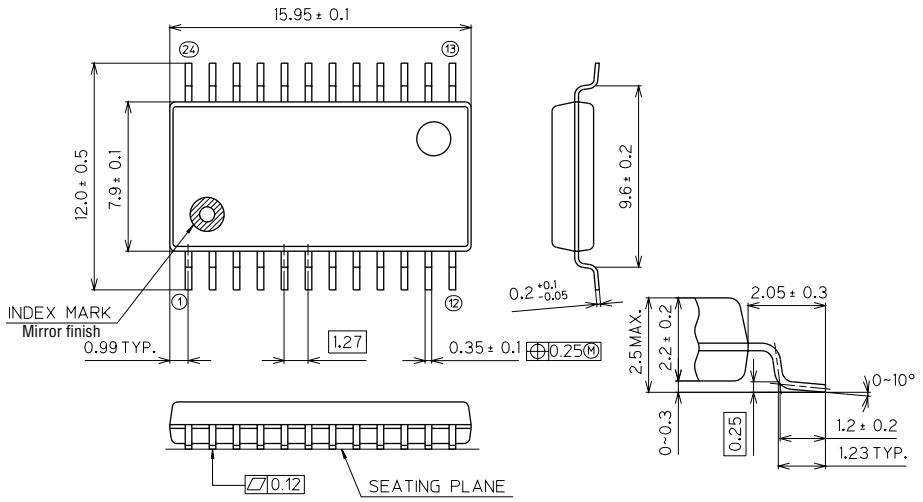
- Keep the voltage on the V_{DD} pin not lower than –0.3 V even instantaneously to avoid latch-up that may otherwise occur when power is turned on.

- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

PACKAGE DIMENSIONS

(Unit : mm)

SOP24-P-430-1.27-K



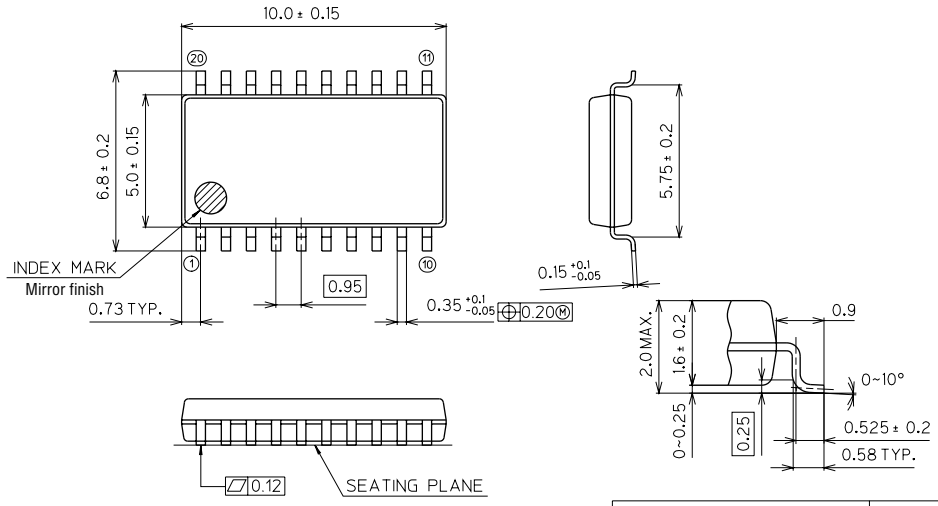
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.58 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

SSOP20-P-250-0.95-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.18 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).