Numonyx™ StrataFlash® Cellular Memory (M18)

Datasheet

Product Features

- High-Performance Read, Program and Erase
  - 96 ns initial read access
  - 108 MHz with zero wait-state synchronous burst reads: 7 ns clock-to-data output
  - 133 MHz with zero wait-state synchronous burst reads: 5.5 ns clock-to-data output
  - 8-, 16-, and continuous-word synchronous-burst Reads
  - Programmable WAIT configuration
  - Customer-configurable output driver impedance
  - Buffered Programming: 2.0 µs/Word (typ), 512-Mbit 65 nm; Block Erase: 0.9 s per block (typ)
  - 20 µs (typ) program/erase suspend
- Architecture
  - 16-bit wide data bus
  - Multi-Level Cell Technology
  - Symmetrically-Blocked Array Architecture
  - 256-Kbyte Erase Blocks
  - 1-Gbit device: Eight 128-Mbit partitions
  - 512-Mbit device: Eight 64-Mbit partitions
  - 256-Mbit device: Eight 32-Mbit partitions.
  - 128-Mbit device: Eight 16-Mbit partitions.
  - Read-While-Program and Read-While-Erase
  - Status Register for partition/device status
  - Blank Check feature
- Quality and Reliability
  - Expanded temperature: –30 °C to +85 °C
  - Minimum 100,000 erase cycles per block
  - ETOX™ X Process Technology (65 nm)
  - ETOX™ IX Process Technology (90 nm)
- Power
  - Core voltage: 1.7 V - 2.0 V
  - I/O voltage: 1.7 V - 2.0 V
  - Standby current: 60 µA (typ) for 512-Mbit, 65 nm
  - Deep Power-Down mode: 2 µA (typ)
  - Automatic Power Savings mode
  - 16-word synchronous-burst read current: 23 mA (typ) @ 108 MHz; 24 mA (typ) @ 133 MHz
- Software
  - Numonyx™ Flash Data Integrator (Numonyx™ FDI) optimized
  - Basic Command Set and Extended Command Set compatible
  - Common Flash Interface
- Security
  - OTP Registers: 64 unique pre-programmed bits 2112 user-programmable bits
  - Absolute write protection with V_{PP} = GND
  - Power-transition erase/program lockout
  - Individual zero-latency block locking
  - Individual block lock-down
- Density and Packaging
  - Density: 128-, 256-, and 512-Mbit, and 1-Gbit
  - Address-data multiplexed and non-multiplexed interfaces
  - x16D (105-ball) Flash SCSP
  - x16C (107-ball) Flash SCSP
  - 0.8 mm pitch lead-free solder-ball

Order Number: 309823-11
April 2008

Contents

Revision History

Date	Revision	Description
14-April-06	001	Initial Release
28-April-06	002	Updated the template (naming and branding). On the cover page, changed BEFP from 1.6 µs/byte (typ) to 3.2 µs/Word (typ).
20-June-06	003	Correced the BEFP on the cover page to read 3.2 µs/Word and synchronized the BEFP on the cover with that in Section 7.4, "Program and Erase Characteristics" on page 68. Added Figure 1, "Mechanical Specifications: x16D (105-ball) package (8x10x1.0 mm)" on page 14 and Figure 5, "Mechanical Specifications: x16 Split Bus (165-ball) package (10x11x1.2 mm)" on page 18. Added the following line item part numbers: —PF48F6000M0Y0BE —PF38F6070M0Y0BE —PF38F6070M0Y0VE —PF48F6000M0Y1BE
October 2006	004	Removed information on the 90 nm Extended Flash Array (EFA) feature that is no longer supported.
November 2006	005	Revised to include 65 nm, 1-Gbit device information. Moved sections for Device ID, Additional Information, and Order Information to Functional Description chapter. Created a separate M18 Developer's Manual to include the following information: —Bus Interface —Flash Operations —Device Command Codes —Flow Charts —Common Flash Interface —Next State Table Removed line item PF5566MMY0C0 (512+512 M18 + 128 + 128 PSRAM) and its accompanying package (8x11x1.4, x16C 107 ball). Added the following line items: —PF48F6000M0Y0BE, 65 nm —PF38F6070M0Y0BE, 65 nm —PF38F4060M0Y0B0 —PF58F0031M0Y1BE, 65 nm —PF38F6070M0Y0C0, 65 nm —PF38F4060M0Y0C0 —PF38F4060M0Y1C0 —PF38F6070M0Y0VE, 65 nm Added the following packages to support new line items: —8x10x1.0, x16D 105 ball —11x15x1.2, x16D 105 ball —11x11x1.2, x16C 107 ball —8x10x1.2, x16C 107 ball —10x11x1.2, x16SB 165 ball
November 2006	006	Updated line item information.
February 2007	007	Added the following line items and package as applicable: PF48F4000M0Y0CE, 8x10x1.0 x16C
June 2007	008	Merged the Developer Manual and Datasheet content into a single document.
March 2008	009	Updated the Performance specifications for 133MHz Capulet 1G improvements.
March 2007	008	Updated timing diagrams in AC Characteristics section.

Date	Revision	Description
July 2007	009	Added note stating the value of RCR8 in timing diagrams in Section 7.2.1, "Read Timing Waveforms" on page 52. Resized several timing diagrams in AC Characteristics section. Updated timing diagrams Figure 31, "Async Read to Write (Non-Mux)" on page 62, Figure 36, "Async Read to Write (AD-Mux)" on page 66 and Figure 37, "Write to Async Read (AD-Mux)" on page 66
March 2008	010	Updated Program performance specs with Capulet improved performance values.
April 2008	11	Applied Numonyx branding.

1.0 Introduction

Numonyx™ StrataFlash® Cellular Memory is the sixth generation Numonyx™ StrataFlash® memory with multi-level cell (MLC) technology. It provides high-performance, low-power synchronous-burst read mode and asynchronous read mode at 1.8 V. It features flexible, multi-partition read-while-program and read-while-erase capability, enabling background programming or erasing in one partition simultaneously with code execution or data reads in another partition. The eight partitions allow flexibility for system designers to choose the size of the code and data segments. The Numonyx™ StrataFlash® Cellular Memory is manufactured using Intel* 65 nm ETOX* X and 90 nm ETOX* IX process technology and is available in industry-standard chip-scale packaging.

1.1 Document Purpose

This document describes the specifications of the Numonyx™ StrataFlash® Cellular Memory device.

1.2 Nomenclature

Table 1: Definition of Terms

Term	Definition
1.8 V	Refers to VCC and VCCQ voltage range of 1.7 V to 2.0 V
Block	A group of bits that erase with one erase command
Main Array	A group of 256-KB blocks used for storing code or data
Partition	A group of blocks that share common program and erase circuitry and command status register
Programming Region	An aligned 1-KB section within the main array
Segment	A 32-byte section within the programming region
Byte	8 bits
Word	2 bytes = 16 bits
Kb	1024 bits
KB	1024 bytes
KW	1024 words
Mb	1,048,576 bits
MB	1,048,576 bytes

1.3 Acronyms

Table 2: List of Acronyms

Acronym	Meaning
APS	Automatic Power Savings
CFI	Common Flash Interface
DU	Don't Use
ECR	Enhanced Configuration Register (Flash)

Table 2: List of Acronyms

Acronym	Meaning
ETOX	EPROM Tunnel Oxide
FDI	Numonyx™ Flash Data Integrator
RCR	Read Configuration Register (Flash)
RFU	Reserved for Future Use
SCSP	Stacked Chip Scale Package

1.4 Conventions

Table 3: Datasheet Conventions

Convention	Meaning
Group Membership Brackets	Square brackets are used to designate group membership or to define a group of signals with a similar function, such as A[21:1].
VCC vs. V_{CC}	When referring to a signal or package-connection name, the notation used is VCC. When referring to a voltage level, the notation used is subscripted such as V_{CC}.
Device	This term is used interchangeably throughout this document to denote either a particular die, or all die in the package.
F[3:1]-CE#, F[2:1]-OE#	This is the method used to refer to more than one chip-enable or output enable. When each is referred to individually, the reference is F1-CE# and F1-OE# (for die #1), and F2-CE# and F2-OE# (for die #2).
F-VCC P-VCC, S-VCC	When referencing flash memory signals, the notation used is F-VCC or F-$V_{CC,}$ respectively. When the reference is to PSRAM signals or timings, the notation is prefixed with "P-" (for example, P-VCC, P-V_{CC}). When referencing SRAM signals or timings, the notation is prefixed with "S-" (for example, S-VCC or S-V_{CC}). P-VCC and S-VCC are RFU for stacked combinations that do not include PSRAM or SRAM.
R-OE#, R-LB#, R-UB#, R-WE#	Used to identify RAM OE#, LB#, UB#, WE# signals, and are usually shared between two or more RAM die. R-OE#, R-LB#, R-UB# and R-WE# are RFU for stacked combinations that do not include PSRAM or SRAM.
00FFh	Denotes 16-bit hexadecimal numbers
00FF 00FFh	Denotes 32-bit hexadecimal numbers

2.0 Functional Description

2.1 Product Overview

The Numonyx™ StrataFlash® Cellular Memory (M18) device provides high read and write performance at low voltage on a 16-bit data bus.

The flash memory device has a multi-partition architecture with read-while-program and read-while-erase capability.

The device supports synchronous burst reads up to 108 MHz using ADV# and CLK address-latching on some litho/density combinations and up to 133 MHz using CLK address-latching only on some litho/density combinations. It is listed below in the following table.

Table 4: M18 Product Litho / Density / Frequency Combinations

Litho (nm)	Density (Mbit)	Supports frequency up to (MHz)	Sync read address-latching
90	256	133	CLK-latching
	512	108	ADV#- and CLK-latching
65	128	133	CLK-latching
	256	133	CLK-latching
	512	133	CLK-latching
	1024	108	ADV#- and CLK-latching
	1024	133	CLK-latching

In continuous-burst mode, a data Read can traverse partition boundaries.

Upon initial power-up or return from reset, the device defaults to asynchronous array-read mode. Synchronous burst-mode reads are enabled by programming the Read Configuration Register. In synchronous burst mode, output data is synchronized with a user-supplied clock signal. A WAIT signal provides easy CPU-to-flash memory synchronization.

Designed for low-voltage applications, the device supports read operations with V_{CC} at 1.8 V, and erase and program operations with V_{PP} at 1.8 V or 9.0 V. VCC and VPP can be tied together for a simple, ultra-low power design. In addition to voltage flexibility, a dedicated VPP connection provides complete data protection when V_{PP} is less than V_{PPLK}.

A Status Register provides status and error conditions of erase and program operations.

One-Time-Programmable (OTP) registers allow unique flash device identification that can be used to increase flash content security. Also, the individual block-lock feature provides zero-latency block locking and unlocking to protect against unwanted program or erase of the array.

The flash memory device offers three power savings features:

- Automatic Power Savings (APS) mode: The device automatically enters APS following a read-cycle completion.
- Standby mode: Standby is initiated when the system deselects the device by deasserting CE#.

- Deep Power-Down (DPD) mode: DPD provides the lowest power consumption and is enabled by programming in the Enhanced Configuration Register. DPD is initiatied by asserting the DPD pin.

2.2 Configuration and Memory Map

The Numonyx™ StrataFlash® Cellular Memory device features a symmetrical block architecture. The flash device main array is divided as follows:

- The main array of the 128-Mbit device is divided into eight 16-Mbit partitions. Each parition is divided into eight 256-KByte blocks: 8 x 8 = 64 blocks in the main array of a 128-Mbit device.
- The main array of the 256-Mbit device is divided into eight 32-Mbit partitions. Each parition is divided into sixteen 256-KByte blocks: 8 x 16 = 128 blocks in the main array of a 256-Mbit device.
- The main array of the 512-Mbit device is divided into eight 64-Mbit partitions. Each parition is divided into thirty-two 256-KByte blocks: 8 x 32 = 256 blocks in the main array of a 256-Mbit device.
- The main array of the 1-Gbit device is divided into eight 128-Mbit partitions. Each parition is divided into sixty-four 256-KByte blocks: 8 x 64 = 512 blocks in the main array of a 1-Gbit device.

Each block is divided into as many as two-hundred-fifty-six 1-KByte programming regions. Each region is divided into as many as thirty-two 32-Byte segments.

Table 5: Main Array Memory Map (Sheet 1 of 2)

Partition	Mbit	128-Mbit Device		Mbit	256-Mbit Device		Mbit	512-Mbit Device		Mbit	1-Gbit Device	
		Blk #	Address Range		Blk #	Address Range		Blk #	Address Range		Blk #	Address Range
7	16	63	07E0000-07FFFFF	32	127	0FE0000-0FFFFFF	64	255	1FE0000-1FFFFFF	128	511	3FE0000-3FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		56	0700000-071FFFF		112	0E00000-0E1FFFF		224	1C00000-1C1FFFF		448	3800000-381FFFF
6	16	55	06E0000-06FFFFF	32	111	0DE0000-0DFFFFF	64	223	1BE0000-1BFFFFF	128	447	37E0000-37FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		48	0600000-061FFFF		96	0C00000-0C1FFFF		192	1800000-181FFFF		384	3000000-301FFFF
5	16	47	05E0000-05FFFFF	32	95	0BE0000-0BFFFFF	64	191	17E0000-17FFFFF	128	383	2FE0000-2FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		40	0500000-051FFFF		80	0A00000-0A1FFFF		160	1400000-141FFFF		320	2800000-281FFFF
4	16	39	04E0000-04FFFFF	32	79	09E0000-09FFFFF	64	159	13E0000-13FFFFF	128	319	27E0000-27FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		32	0400000-041FFFF		64	0800000-081FFFF		128	1000000-101FFFF		256	2000000-201FFFF

Table 5: Main Array Memory Map (Sheet 2 of 2)

Partition	Mbit	128-Mbit Device		Mbit	256-Mbit Device		Mbit	512-Mbit Device		Mbit	1-Gbit Device	
		Blk #	Address Range		Blk #	Address Range		Blk #	Address Range		Blk #	Address Range
3	16	31	03E0000-03FFFFF	32	63	07E0000-07FFFFF	64	127	0FE0000-0FFFFFF	128	255	1FE0000-1FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		24	0300000-031FFFF		48	0600000-061FFFF		96	0C00000-0C1FFFF		192	1800000-181FFFF
2	16	23	02E0000-02FFFFF	32	47	05E0000-05FFFFF	64	95	0BE0000-0BFFFFF	128	191	17E0000-17FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		16	0200000-021FFFF		32	0400000-041FFFF		64	0800000-081FFFF		128	1000000-101FFFF
1	16	15	01E0000-01FFFFF	32	31	03E0000-03FFFFF	64	63	07E0000-07FFFFF	128	127	0FE0000-0FFFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		8	0100000-011FFFF		16	0200000-021FFFF		32	0400000-041FFFF		64	0800000-081FFFF
0	16	7	00E0000-00FFFFF	32	15	01E0000-01FFFFF	64	31	03E0000-03FFFFF	128	63	07E0000-07FFFFF
		⋮	⋮		⋮	⋮		⋮	⋮		⋮	⋮
		0	0000000-001FFFF		0	0000000-001FFFF		0	0000000-001FFFF		0	0000000-001FFFF

2.3 Device ID

Table 6: Device ID codes

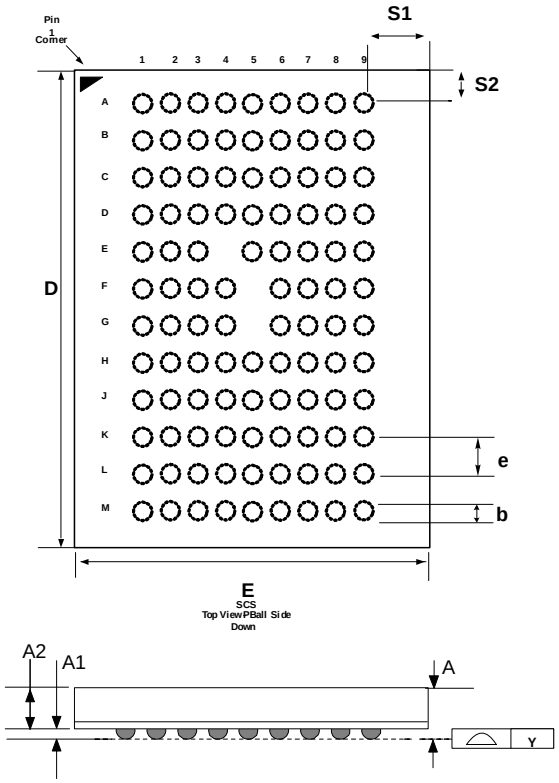
Density	Litho (nm)	Product	Device Identifier Code (Hex)
128 Mbit	65	Non-Mux	8900
		AD-Mux	8903
256 Mbit	65, 90	Non-Mux	8901
		AD-Mux	8904
512 Mbit	65, 90	Non-Mux	887E
		AD-Mux	8881
1024 Mbit	65	Non-Mux	88B0
		AD-Mux	88B1

Note: To order parts listed above and to obtain a datasheet for the M18 SCSP parts, please contact your local Numonyx sales office.

3.0 Package Information

The following figures show the ballout package information for the device:

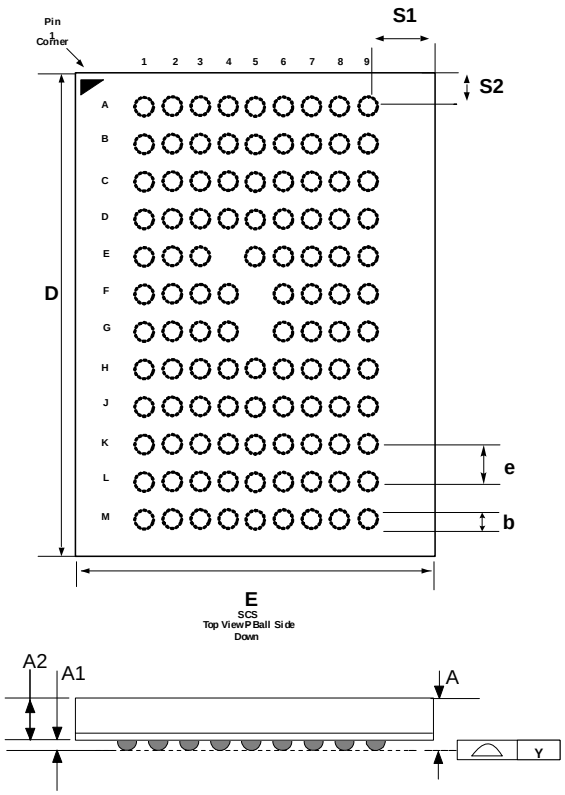
Figure 1: Mechanical Specifications: x16D (105-ball) package (8x10x1.0 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.0				0.0394
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.660				0.0260	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

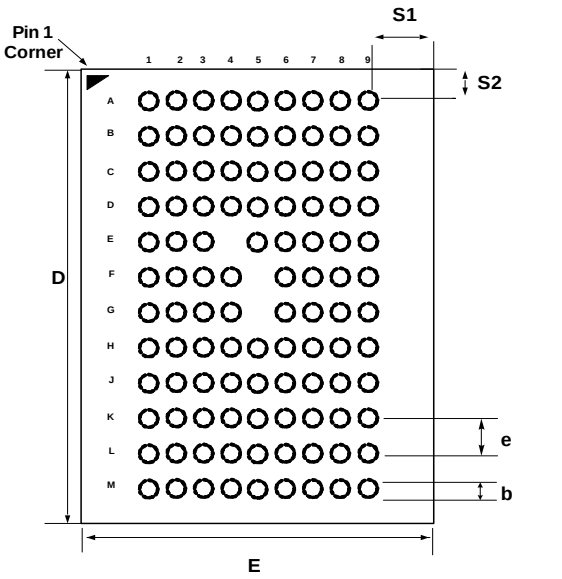
Figure 2: Mechanical Specifications: x16D (105-ball) package (8x10x1.4 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.4				0.0551
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		1.070				0.0421	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

Figure 3: Mechanical Specifications: x16D (105-ball) package (9x11x1.2 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	8.90	9.00	9.10		0.3504	0.3543	0.3583
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		105				105	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.200	1.300	1.400		0.0472	0.0512	0.0551
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 4: Mechanical Specifications: x16D (105 balls) Package (11x15x1.2 mm)

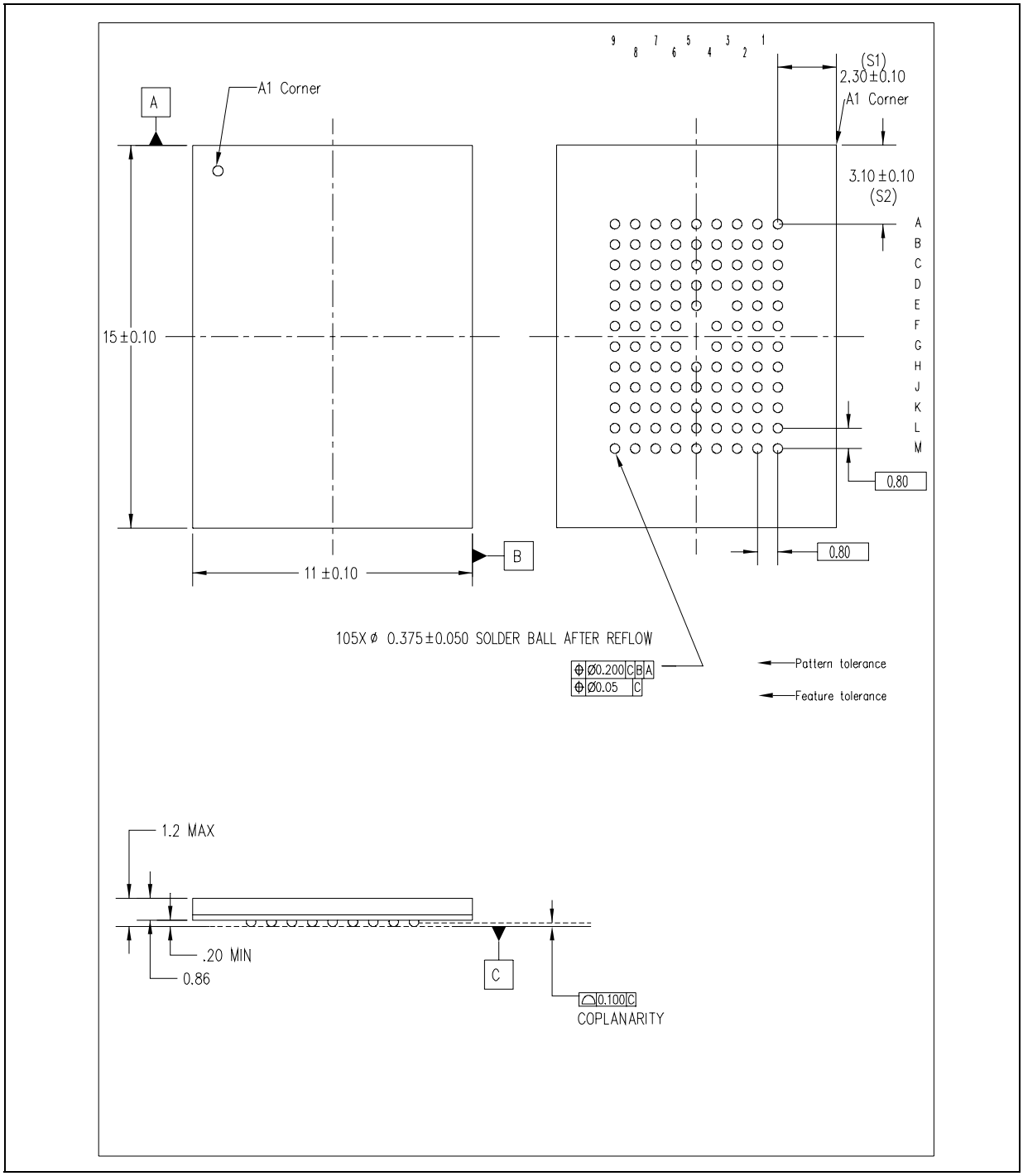
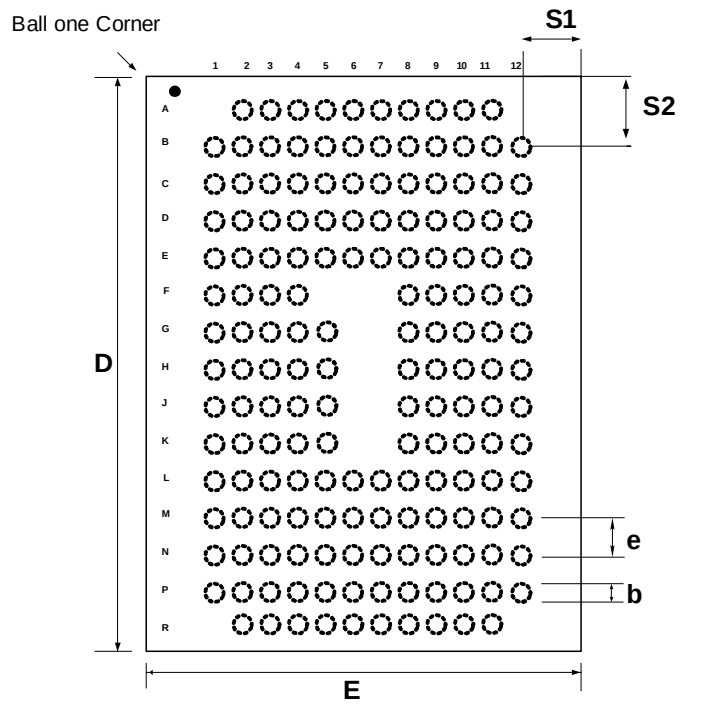
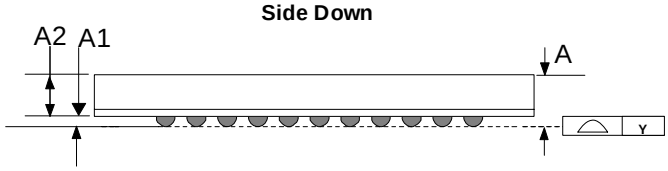


Figure 5: Mechanical Specifications: x16 Split Bus (165-ball) package (10x11x1.2 mm)



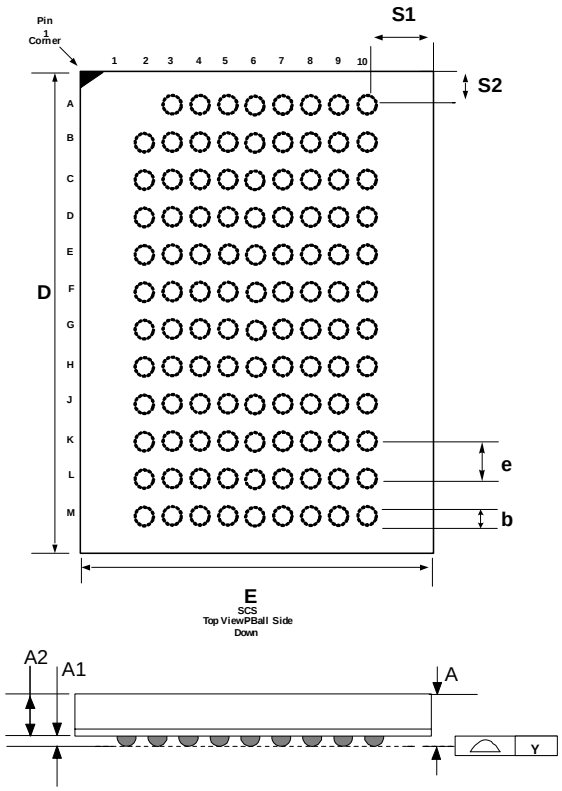
Top View - Ball Side Down



Note: Drawing not to scale.

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	9.90	10.00	10.10		0.3898	0.3937	0.3976
Pitch	e		0.650				0.0256	
Ball (Lead) Count	N		165				165	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	1.325	1.425	1.525		0.0522	0.0561	0.0600
Corner to Ball Distance Along D	S2	1.500	1.600	1.700		0.0591	0.0630	0.0669

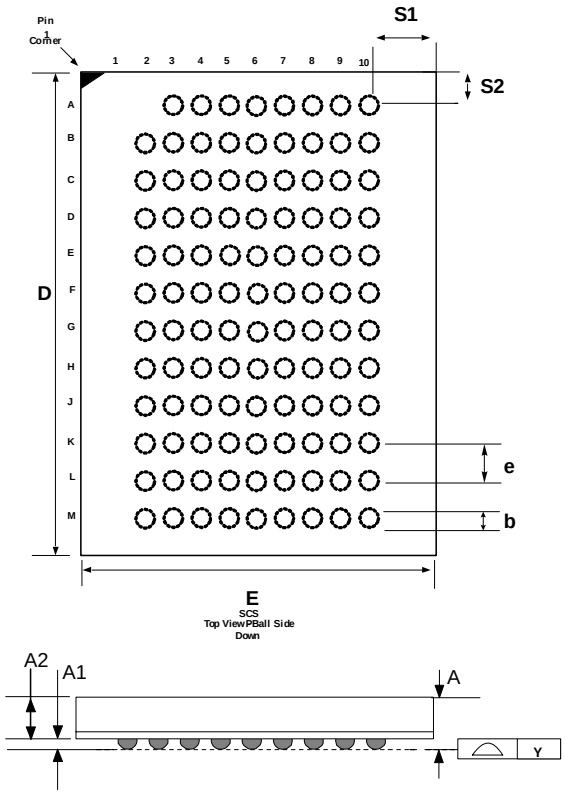
Figure 6: Mechanical Specifications: x16C (107-ball) package (8x10x1.0 mm)



Note: Drawing not to scale.

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.0				0.0394
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.660				0.0260	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

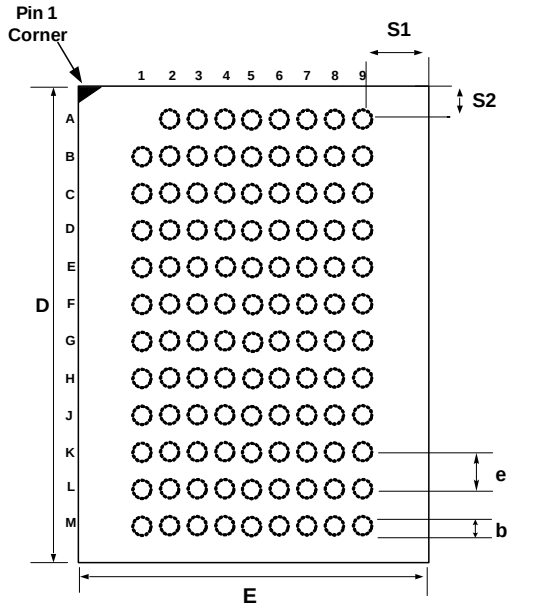
Figure 7: Mechanical Specifications: x16C (107-ball) package (8x10x1.2 mm)



Note: Drawing not to scale

Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.90	10.00	10.10		0.3898	0.3937	0.3976
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

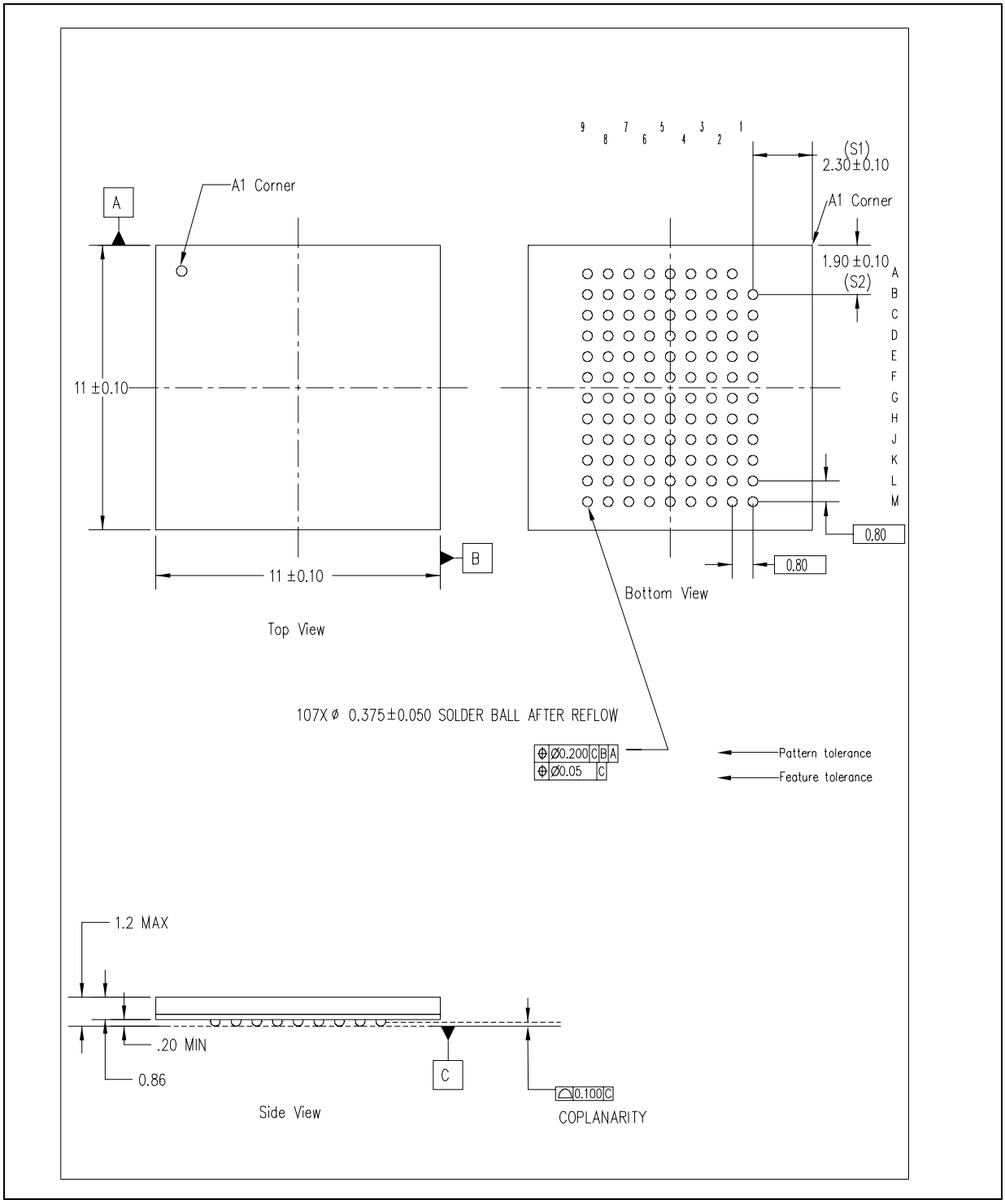
Figure 8: Mechanical Specifications: x16C (107-ball) package (8x11x1.2 mm)



Note: Drawing not to scale.

		Millimeters				Inches		
Dimensions	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A			1.2				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	10.90	11.00	11.10		0.4291	0.4331	0.4370
Package Body Width	E	7.90	8.00	8.10		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		107				107	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball Distance Along E	S1	0.700	0.800	0.900		0.0276	0.0315	0.0354
Corner to Ball Distance Along D	S2	1.000	1.100	1.200		0.0394	0.0433	0.0472

Figure 9: Mechanical Specifications: x16C (107-ball) package (11x11x1.2 mm)



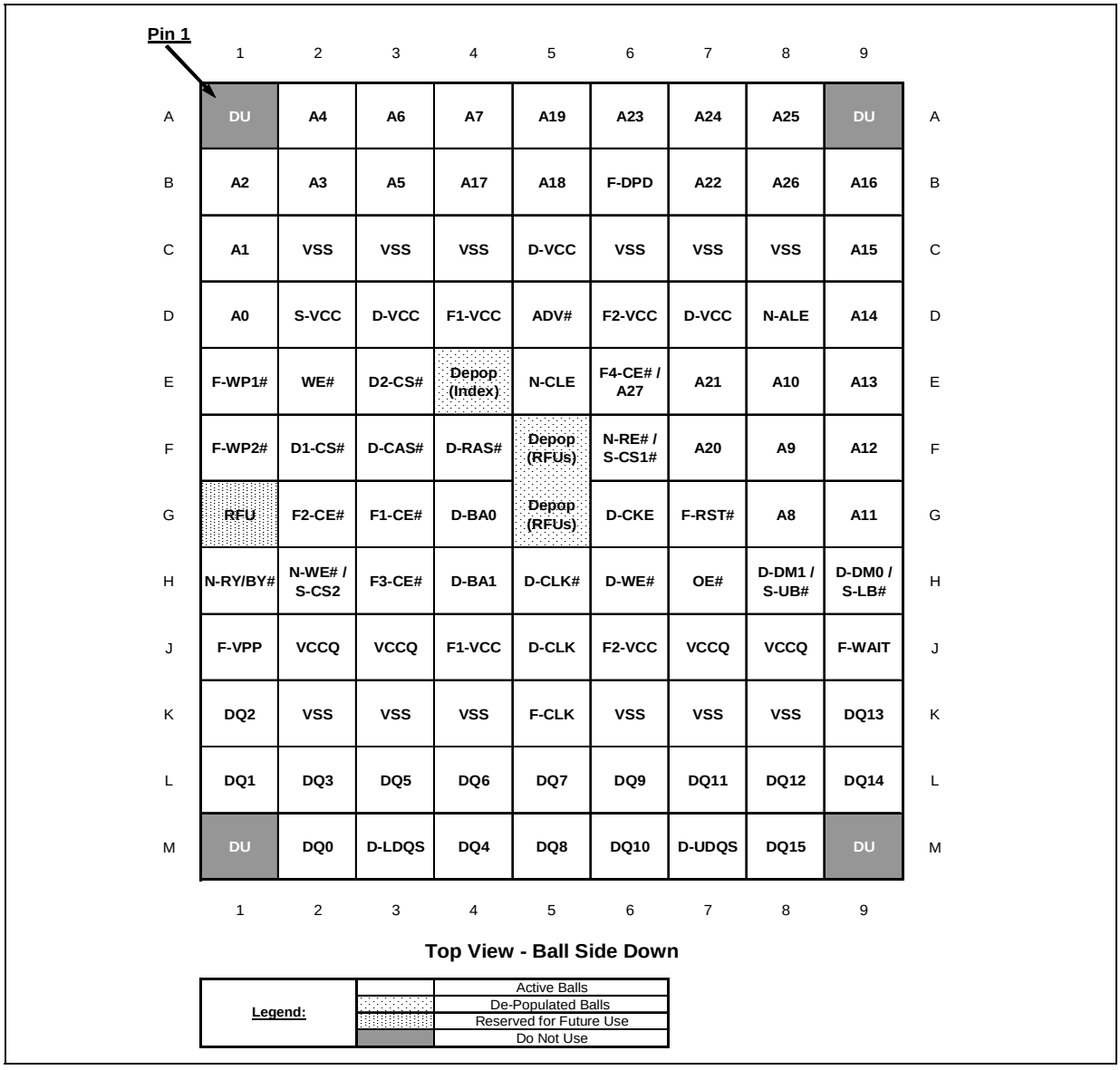
4.0 Ballouts and Signal Descriptions

This section provides ballout and signal description information for x16D (105-ball), x16C (107-ball), and x16 Split Bus (165-ball) packages, Non-Mux, AD-Mux, AA/D Mux interfaces.

4.1 Ballouts, x16D

4.1.1 x16D (105-Ball) Ballout, Non-Mux

Figure 10: x16D (105-Ball) Electrical Ballout, Non-Mux



4.1.2 x16D (105-Ball) Ballout, AD-Mux

Figure 11: x16D (105-Ball) Electrical Ballout, AD-Mux

Pin 1

	1	2	3	4	5	6	7	8	9	
A	DU	A4	A6	A7	A19	A23	A24	A25	DU	A
B	A2	A3	A5	A17	A18	F-DPD	A22	A26	A16	B
C	A1	VSS	VSS	VSS	D-VCC	VSS	VSS	VSS	A15	C
D	A0	S-VCC	D-VCC	F1-VCC	ADV#	F2-VCC	D-VCC	N-ALE	A14	D
E	F-WP1#	WE#	D2-CS#	Depop (Index)	N-CLE	F4-CE# / A27	A21	A10	A13	E
F	F-WP2#	D1-CS#	D-CAS#	D-RAS#	Depop (RFUs)	N-RE# / S-CS1#	A20	A9	A12	F
G	RFU	F2-CE#	F1-CE#	D-BA0	Depop (RFUs)	D-CKE	F-RST#	A8	A11	G
H	N-RY/BY#	N-WE# / S-CS2	F3-CE#	D-BA1	D-CLK#	D-WE#	OE#	D-DM1 / R-UB#	D-DM0 / R-LB#	H
J	F-VPP	VCCQ	VCCQ	F1-VCC	D-CLK	F2-VCC	VCCQ	VCCQ	F-WAIT	J
K	AD2	VSS	VSS	VSS	F-CLK	VSS	VSS	VSS	AD13	K
L	AD1	AD3	AD5	AD6	AD7	AD9	AD11	AD12	AD14	L
M	DU	AD0	D-LDQS	AD4	AD8	AD10	D-UDQS	AD15	DU	M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:		Active Balls
		De-Populated Balls
		Reserved for Future Use
		Do Not Use

4.1.3 x16D Mux (105-Ball) Ballout, AA/D Mux

Figure 12: x16D (105-Ball) Electrical Ballout, AA/D Mux

Pin 1

	1	2	3	4	5	6	7	8	9	
A	DU	A4	A6	A7	RFU	RFU	RFU	RFU	DU	A
B	A2	A3	A5	RFU	RFU	F-DPD	RFU	F-ADV2#	RFU	B
C	A1	VSS	VSS	VSS	D-VCC	VSS	VSS	VSS	A15	C
D	A0	S-VCC	D-VCC	F-VCC	F-ADV#	F-VCC	D-VCC	N-ALE	A14	D
E	F-WP1#	WE#	D2-CS#	Depop (Index)	N-CLE	F4-CE#	RFU	A10	A13	E
F	F-WP2#	D1-CS#	D-CAS#	D-RAS#	Depop (RFU)	S-CS1 / N-RE#	RFU	A9	A12	F
G	RFU	F2-CE#	F1-CE#	D-BA0	Depop (RFU)	D-CKE	F-RST#	A8	A11	G
H	N-RY/BY#	S-CS2 / N-WE#	F3-CE#	D-BA1	D-CLK#	D-WE#	OE#	D-DM1 / S-UB#	D-DM0 / S-LB#	H
J	F-VPP	VCCQ	VCCQ	F-VCC	D-CLK	F-VCC	VCCQ	VCCQ	F-WAIT	J
K	AD2	VSS	VSS	VSS	F-CLK	VSS	VSS	VSS	AD13	K
L	AD1	AD3	AD5	AD6	AD7	AD9	AD11	AD12	AD14	L
M	DU	AD0	D-LDQS	AD4	AD8	AD10	D-UDQS	AD15	DU	M
	1	2	3	4	5	6	7	8	9	

Top View - Ball Side Down

Legend:	
	Active Balls
	De-Populated Balls
	Reserved for Future Use
	Do Not Use

4.2 Signal Descriptions, x16D

Table 7: Signal Descriptions, x16D Non-Mux/AD-Mux; x16D AA/D-Mux (Sheet 1 of 4)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX: 0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 • A[12:0] are the row and A[9:0] are the column addresses for 512-Mbit LPSDRAM. • A[12:0] are the row and A[8:0] are the column addresses for 256-Mbit LPSDRAM. • A[11:0] are the row and A[8:0] are the column addresses for 128-Mbit LPSDRAM. Unused address inputs should be treated as RFU.	1
DQ[15:0]	Input/ Output	**DATA INPUT/OUTPUTS:** Global device signals. DQ[15:0] are used to input commands and write-data during Write cycles, and to output read-data during Read cycles. During NAND accesses, DQ[7:0] are used to input commands, address-data, and write-data, and to output read-data. Data signals are High-Z when the device is deselected or its output is disabled.	
F-ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV# or continuously flows through while F-ADV# is low.	
Address and Data Signals, AD-Mux			
A[MAX:16]	Input	**ADDRESS:** Global device signals. Shared address inputs for all Flash and SRAM memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs should be treated as RFU.	1
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** AD-Mux flash and SRAM lower address and data signals; LPSDRAM data signals. During AD-Mux flash and SRAM Write cycles, AD[15:0] are used to input the lower address followed by commands or write-data. During AD-Mux flash Read cycles, AD[15:0] are used to input the lower address followed by read-data output. During LPSDRAM accesses, AD[15:0] are used to input commands and write-data during Write cycles or to output read-data during Read cycles. During NAND accesses, AD[7:0] are used to input commands, address, or write-data, and to output read-data. AD[15:0] are High-Z when the flash or SRAM is deselected or its output is disabled.	
A[15:0]	Input	RFU, except for DRAM.	

Table 7: Signal Descriptions, x16D Non-Mux/AD-Mux; x16D AA/D-Mux (Sheet 2 of 4)

Symbol	Type	Signal Descriptions	Notes
F-ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV#.	
A[MAX: 0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27 • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 • A[12:0] are the row and A[9:0] are the column addresses for 512-Mbit LPSDRAM. • A[12:0] are the row and A[8:0] are the column addresses for 256-Mbit LPSDRAM. • A[11:0] are the row and A[8:0] are the column addresses for 128-Mbit LPSDRAM. Unused address inputs should be treated as RFU.	1
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** AAD-Mux flash address and data; LPSDRAM data. During AAD-Mux flash Write cycles, AD[15:0] are used to input the upper address, lower address, and commands or write-data. During AAD-Mux flash Read cycles, AD[15:0] are used to input the upper address and lower address, and output read-data. During LPSDRAM accesses, AD[15:0] are used to input commands and write-data during Write cycles or to output read-data during Read cycles. During NAND accesses, AD[7:0] are used to input commands, address-data, or write-data, and to output read-data. AD[15:0] are High-Z when the device is deselected or its output is disabled.	
F-ADV# F-ADV2#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During a synchronous flash Read operation, the address is latched on the F-ADV# rising edge or the first F-CLK edge after F-ADV# low in devices that support up to 104 MHz, and on the last rising F-CLK edge after F-ADV# low in devices that support upto 133 MHz. During a synchronous flash Read operation, the address is latched on the rising edge of F-ADV# or the first active F-CLK edge whichever occurs first. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV#. During AAD-Mux flash accesses, the upper address is latched on the valid edge of F-CLK while F-ADV2# is low; the lower address is latched on the valid edge of F-CLK while F-ADV# is low. The upper address is always latched first, followed by the lower address.	
Control Signals			
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU. • For NOR/NAND stacked device, F1-CE# selects NOR die #1, F2-CE# selects NOR die #2 while F4-CE# selects NAND die #1 and NAND die #2 using virtual chip-select scheme, F3-CE# selects NAND die #3 if present.	1
F-CLK	Input	**FLASH CLOCK:** Flash-specific signal; rising active-edge input. F-CLK synchronizes the flash with the system clock during synchronous operations.	
D-CLK	Input	**LPSDRAM CLOCK:** LPSDRAM-specific signal; rising active-edge input. D-CLK synchronizes the LPSDRAM and DDR LPSDRAM with the system clock.	2
D-CLK#	Input	**DDR LPSDRAM CLOCK:** DDR LPSDRAM-specific signal; falling active-edge input. D-CLK# synchronizes the DDR LPSDRAM with the system clock.	2

Table 7: Signal Descriptions, x16D Non-Mux/AD-Mux; x16D AA/D-Mux (Sheet 3 of 4)

Symbol	Type	Signal Descriptions	Notes
OE#	Input	**OUTPUT ENABLE:** Flash- and SRAM-specific signal; low-true input. When low, OE# enables the output drivers of the selected flash or SRAM die. When high, OE# disables the output drivers of the selected flash or SRAM die and places the output drivers in High-Z.	
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
F-WAIT	Output	**FLASH WAIT:** Flash -specific signal; configurable-true output. When asserted, F-WAIT indicates invalid output data. F-WAIT is driven whenever F-CE# and OE# are low. F-WAIT is High-Z whenever F-CE# or OE# is high.	
WE#	Input	**WRITE ENABLE:** Flash- and SRAM-specific signal; low-true input. When low, WE# enables Write operations for the enabled flash or SRAM die.	
D-WE#	Input	**LPSDRAM WRITE ENABLE:** LPSDRAM-specific signal; low-true input. D-WE#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-RAS#, define the LPSDRAM command or operation. D-WE# is sampled on the rising edge of D-CLK.	2
F-WP[2:1]#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is common to all other flash dies, if present. Otherwise it is RFU. • For NOR/NAND stacked device, F-WP1# selects all NOR dies; F-WP2# selects all NAND dies.	
F-DPD	Input	**FLASH DEEP POWER-DOWN:** Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter and exit Deep Power-Down mode.	
N-CLE	Input	**NAND COMMAND LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of N-WE#.	2
N-ALE	Input	**NAND ADDRESS LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of N-WE#.	2
N-RE#	Input	**NAND READ ENABLE:** NAND-specific signal; low-true input. When low, N-RE# enables the output drivers of the selected NAND die. When high, N-RE# disables the output drivers of the selected NAND die and places the output drivers in High-Z.	2, 4
N-RY/BY#	Output	**NAND READY/BUSY:** NAND-specific signal; low-true output. When low, N-RY/BY# indicates the NAND is busy performing a read, program, or erase operation. When high, N-RY/BY# indicates the NAND device is ready.	2
N-WE#	Input	**NAND WRITE ENABLE:** NAND-specific signal; low-true input. When low, N-WE# enables Write operations for the enabled NAND die.	2, 5
D-CKE	Input	**LPSDRAM CLOCK ENABLE:** LPSDRAM-specific signal; high-true input. When high, D-CKE indicates that the next D-CLK edge is valid. When low, D-CKE indicates that the next D-CLK edge is invalid and the selected LPSDRAM die is suspended.	2
D-BA[1:0]	Input	**LPSDRAM BANK SELECT:** LPSDRAM-specific input signals. D-BA[1:0] selects one of four banks in the LPSDRAM die.	2
D-RAS#	Input	**LPSDRAM ROW ADDRESS STROBE:** LPSDRAM-specific signal; low-true input. D-RAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-RAS# is sampled on the rising edge of D-CLK.	2
D-CAS#	Input	**LPSDRAM COLUMN ADDRESS STROBE:** LPSDRAM-specific signal; low-true input. D-CAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-RAS#, and D-WE#, define the LPSDRAM command or operation. D-CAS# is sampled on the rising edge of D-CLK.	2
D[2:1]-CS#	Input	**LPSDRAM CHIP SELECT:** LPSDRAM-specific signal; low-true input. When low, D-CS# selects the associated LPSDRAM memory die and starts the command input cycle. When D-CS# is high, commands are ignored but operations continue. • D-CS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-RAS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-CS# is sampled on the rising edge of D-CLK. • D[2:1]-CS# are dedicated to LPSDRAM die #2 and die #1, respectively, if present. Otherwise, any unused LPSDRAM chip selects should be treated as RFU.	2

Table 7: Signal Descriptions, x16D Non-Mux/AD-Mux; x16D AA/D-Mux (Sheet 4 of 4)

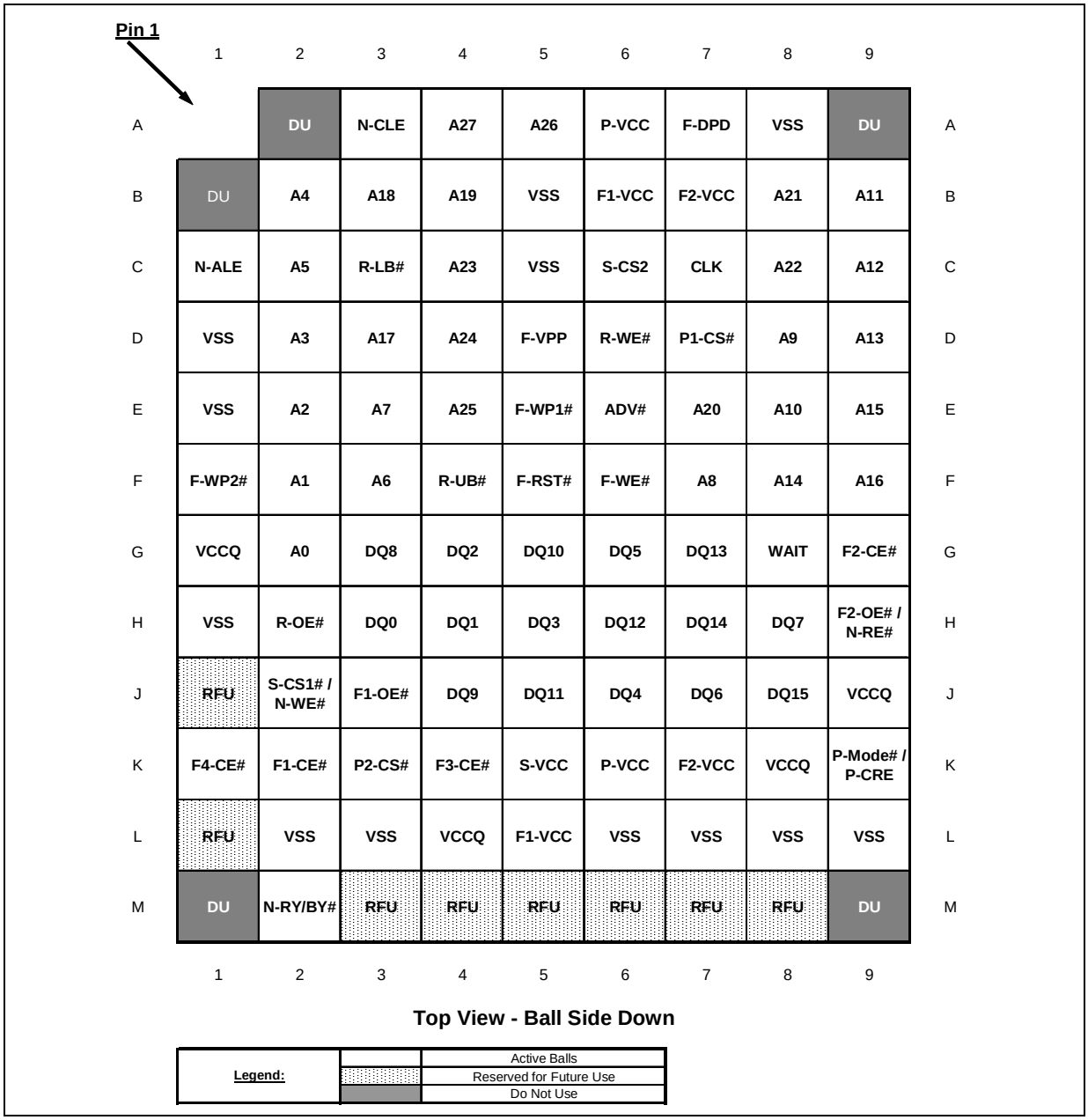
Symbol	Type	Signal Descriptions	Notes
D-DM[1:0]	Input	**LPSDRAM DATA MASK:** LPSDRAM-specific signal; high-true input. When high, D-DM[1:0] controls masking of input data during writes and output data during reads. • D-DM1 corresponds to the data on DQ[15:8]. • D-DM0 corresponds to the data on DQ[7:0].	2, 3
D-UDQS D-LDQS	Input/ Output	**LPSDRAM UPPER/LOWER DATA STROBE:** DDR LPSDRAM-specific input/output signals. D-UDQS and D-LDQS provide as output the read-data strobes, and as input the write-data strobes. • D-UDQS corresponds to the data on DQ[15:8]. • D-LDQS corresponds to the data on DQ[7:0].	2
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both are asserted, S-CS1# and S-CS2 select the SRAM die. When either is deasserted, the SRAM die is deselected and its power is reduced to standby levels.	2, 4, 5
S-UB# S-LB#	Input	**SRAM UPPER/LOWER BYTE ENABLES:** SRAM-specific signals; low-true inputs. When low, S-UB# enables DQ[15:8] and S-LB# enables DQ[7:0] during SRAM Read and Write cycles. When high, S-UB# masks DQ[15:8] and S-LB# masks DQ[7:0].	2, 3
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	
F1-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F1-VCC supplies the core power to the NOR flash die.	
F2-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F2-VCC supplies the core power to either 1) the NOR flash die in stack packages with multiple NOR flash dies, or 2) NAND flash die in stack packages with NOR-NAND flash dies.	6
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	
D-VCC	Power	**LPSDRAM CORE POWER SUPPLY:** LPSDRAM specific. D-VCC supplies the core power to the LPSDRAM die.	2
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die.	2
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** Ball should not be connected to any power supplies, signals, or other balls. Ball can be left floating.	
RFU	—	**RESERVED FOR FUTURE USE:** Reserved by Numonyx for future device functionality/enhancement. Ball must be left floating.	

Notes:
1. F4-CE# and A27 share the same package ball at location E6. Only one signal function is available, depending on the stacked device combination.
2. Only available on stacked device combinations with NAND, SRAM, and/or LPSDRAM die; otherwise, treated as RFU.
3. D-DM[1:0] and S-UB#/S-LB# share the same package balls at locations H8 and H9, respectively. Only one signal function for each ball location is available, depending on the stacked device combination.
4. S-CS1# and N-RE# share the same package ball at location F6. Only one signal function is available, depending on the stacked device combination.
5. S-CS2 and N-WE# share the same package ball at location H2. Only one signal function is available, depending on the stacked device combination.
6. In stack packages with only one NOR flash die, this signal can be left floating.

4.3 Ballouts, x16C

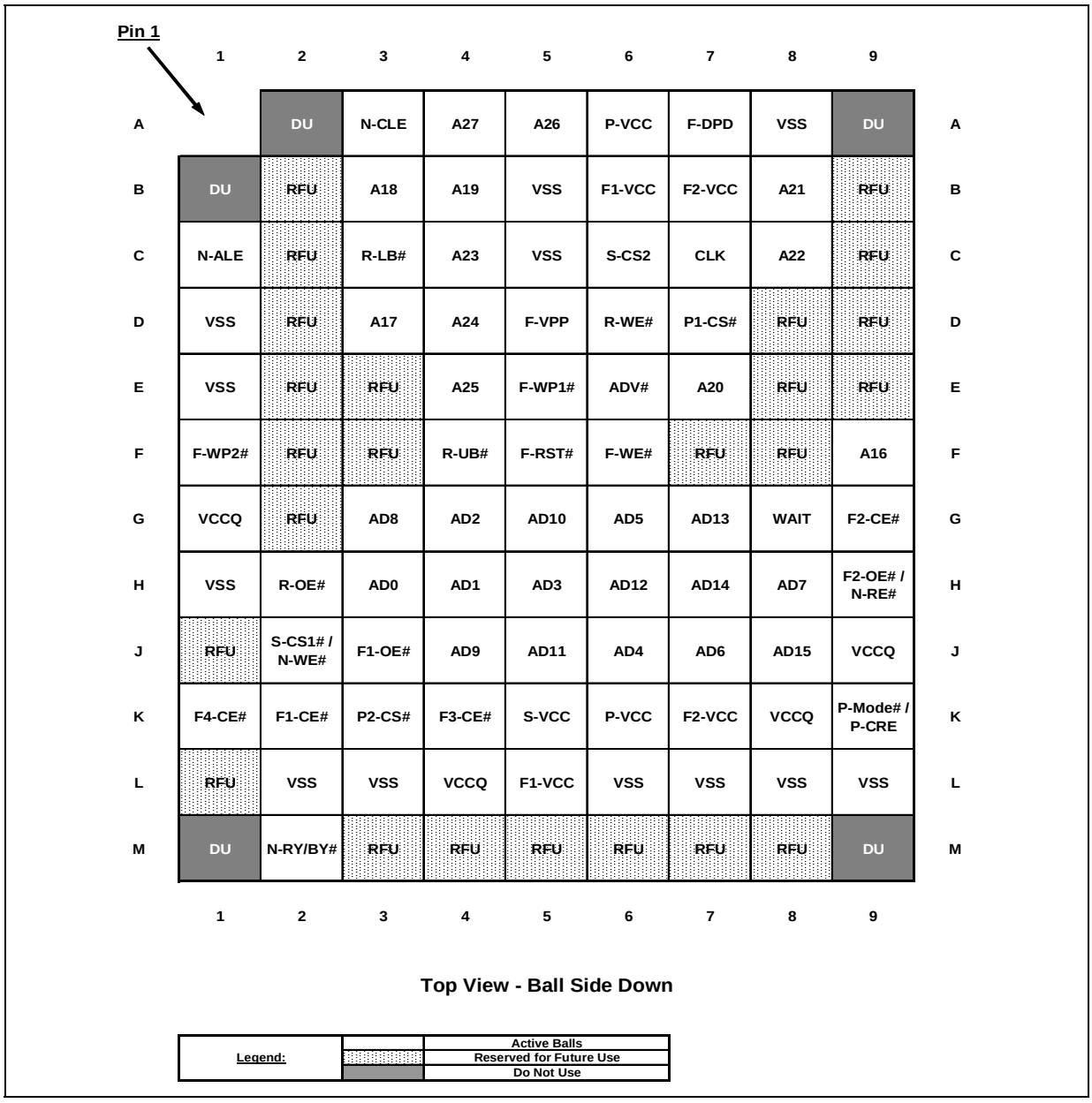
4.3.1 x16C (107-Ball) Ballout, Non-Mux

Figure 13: x16C (107-Ball) Electrical Ballout, Non-Mux



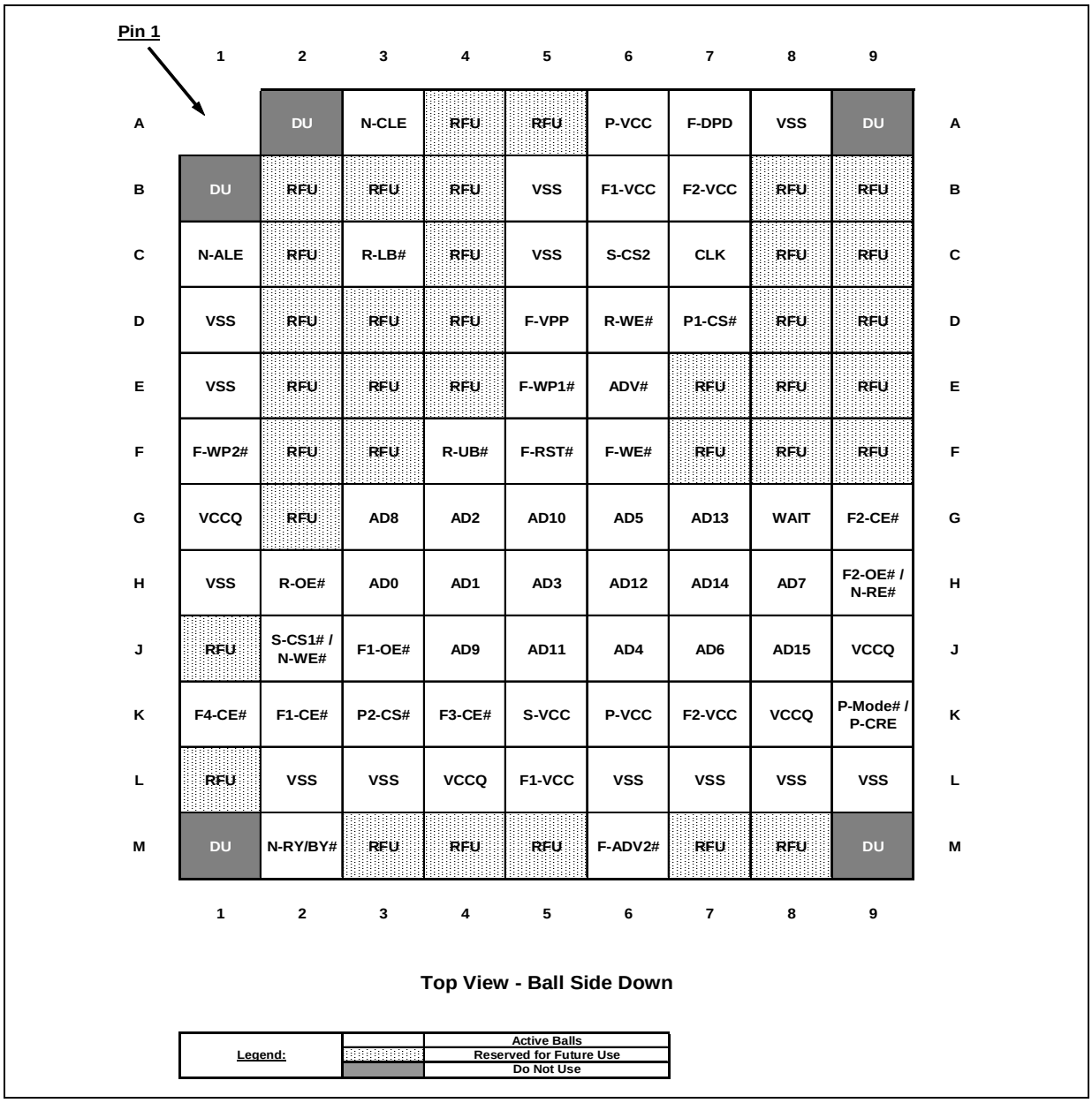
4.3.2 x16C (107-Ball) Ballout, AD-Mux

Figure 14: x16C (107-Ball) Electrical Ballout, AD-Mux



4.3.3 x16C (107-Ball) Ballout, AA/D-Mux

Figure 15: x16C (107-Ball) Electrical Ballout, AA/D-Mux



4.4 Signal Descriptions x16C

Table 8: Signal Descriptions for x16C / x16C AD-Mux / x16C AA/D-Mux Ballout (Sheet 1 of 3)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
A[MAX:0]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27• 128-Mbit: AMAX = A22 • 2-Gbit: AMAX = A26• 64-Mbit: AMAX = A21 • 1-Gbit: AMAX = A25• 32-Mbit: AMAX = A20 • 512-Mbit: AMAX = A24• 16-Mbit: AMAX = A19 • 256-Mbit: AMAX = A23• 8-Mbit: AMAX = A18 Unused address inputs should be treated as RFU.	
DQ[15:0]	Input / Output	**DATA INPUT/OUTPUTS:** Global device signals. Inputs data and commands during Write cycles, outputs data during Read cycles. Data signals are High-Z when the device is deselected or its output is disabled.	
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of ADV# or continuously flows through while ADV# is low.	
Address and Data Signals, AD-Mux			
A[MAX:16]	Input	**ADDRESS:** Global device signals. Shared address inputs for all memory die during Read and Write operations. • 4-Gbit: AMAX = A27• 128-Mbit: AMAX = A22 • 2-Gbit: AMAX = A26• 64-Mbit: AMAX = A21 • 1-Gbit: AMAX = A25• 32-Mbit: AMAX = A20 • 512-Mbit: AMAX = A24• 16-Mbit: AMAX = A19 • 256-Mbit: AMAX = A23• 8-Mbit: AMAX = A18 Unused address inputs should be treated as RFU.	
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** Global device signals. During AD-Mux Write cycles, AD[15:0] are used to input the lower address followed by commands or data. During AD-Mux Read cycles, AD[15:0] are used to input the lower address followed by read-data output. During NAND accesses, AD[7:0] is used to input commands, address-data, or write-data, and output read-data. AD[15:0] are High-Z when the device is deselected or its output is disabled.	
ADV#	Input	**ADDRESS VALID:** Flash- and Synchronous PSRAM-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of ADV#.	
Address and Data Signals, AAD-Mux			
AD[15:0]	Input / Output	**ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS:** Global device signals. During AAD-Mux flash Write cycles, AD[15:0] are used to input the upper address, lower address, and commands or data. During AAD-Mux flash Read cycles, AD[15:0] are used to input the upper address and lower address, and output read-data. During NAND accesses, AD[7:0] is used to input commands, address-data, or write-data, and output read-data. AD[15:0] are High-Z when the device is deselected or its output is disabled.	

Table 8: Signal Descriptions for x16C / x16C AD-Mux / x16C AA/D-Mux Ballout (Sheet 2 of 3)

Symbol	Type	Signal Descriptions	Notes
F-ADV2# ADV#	Input	**FLASH ADDRESS VALID:** Flash-specific signal; low-true input. During AAD-Mux flash accesses, the upper address is latched on the valid edge of CLK while F-ADV2# is low; the lower address is latched on the valid edge of CLK while ADV# is low. The upper address is always latched first, followed by the lower address.	
Control Signals			
F[4:1]-CE#	Input	**FLASH CHIP ENABLE:** Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, any unused flash chip enable should be treated as RFU. • For NOR/NAND stacked device, F1-CE# selects NOR die #1, F2-CE# selects NOR die #2 while F4-CE# selects NAND die #1 and NAND die #2 using virtual chip-select scheme, F3-CE# selects NAND die #3 if present.	
CLK	Input	**CLOCK:** Flash- and Synchronous PSRAM-specific input signal. CLK synchronizes the flash and/or synchronous PSRAM with the system clock during synchronous operations.	
F[2:1]-OE#	Input	**FLASH OUTPUT ENABLE:** Flash-specific signal; low-true input. When low, F-OE# enables the output drivers of the selected flash die. When high, F-OE# disables the output drivers of the selected flash die and places the output drivers in High-Z. • For NOR only stacked device, F[2:1]-OE# are common to all NOR dies in the device. • For NOR/NAND stacked device, F1-OE# enables all NOR dies, F2-OE# selects all NAND dies if present.	2
R-OE#	Input	**RAM OUTPUT ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-OE# enables the output drivers of the selected memory die. When high, R-OE# disables the output drivers of the selected memory die and places the output drivers in High-Z.	1
F-RST#	Input	**FLASH RESET:** Flash-specific signal; low-true input. When low, F-RST# resets internal operations and inhibits writes. When high, F-RST# enables normal operation.	
WAIT	Output	**WAIT:** Flash -and Synchronous PSRAM-specific signal; configurable true-level output. When asserted, WAIT indicates invalid output data. When deasserted, WAIT indicates valid output data. • WAIT is driven whenever the flash or the synchronous PSRAM is selected and its output enable is low. • WAIT is High-Z whenever flash or the synchronous PSRAM is deselected, or its output enable is high.	
F-WE#	Input	**FLASH WRITE ENABLE:** Flash-specific signal; low-true input. When low, F-WE# enables Write operations for the enabled flash die. Address and data are latched on the rising edge of F-WE#.	
R-WE#	Input	**RAM WRITE ENABLE:** PSRAM- and SRAM-specific signal; low-true input. When low, R-WE# enables Write operations for the selected memory die. Data is latched on the rising edge of R-WE#.	1
F-WP[2:1]#	Input	**FLASH WRITE PROTECT:** Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is common to all other flash dies, if present. Otherwise it is RFU. • For NOR/NAND stacked device, F-WP1# selects all NOR dies, while F-WP2# selects all NAND dies.	
F-DPD	Input	**FLASH DEEP POWER-DOWN:** Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter and exit Deep Power-Down mode.	
N-CLE	Input	**NAND COMMAND LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of N-WE#.	1

Table 8: Signal Descriptions for x16C / x16C AD-Mux / x16C AA/D-Mux Ballout (Sheet 3 of 3)

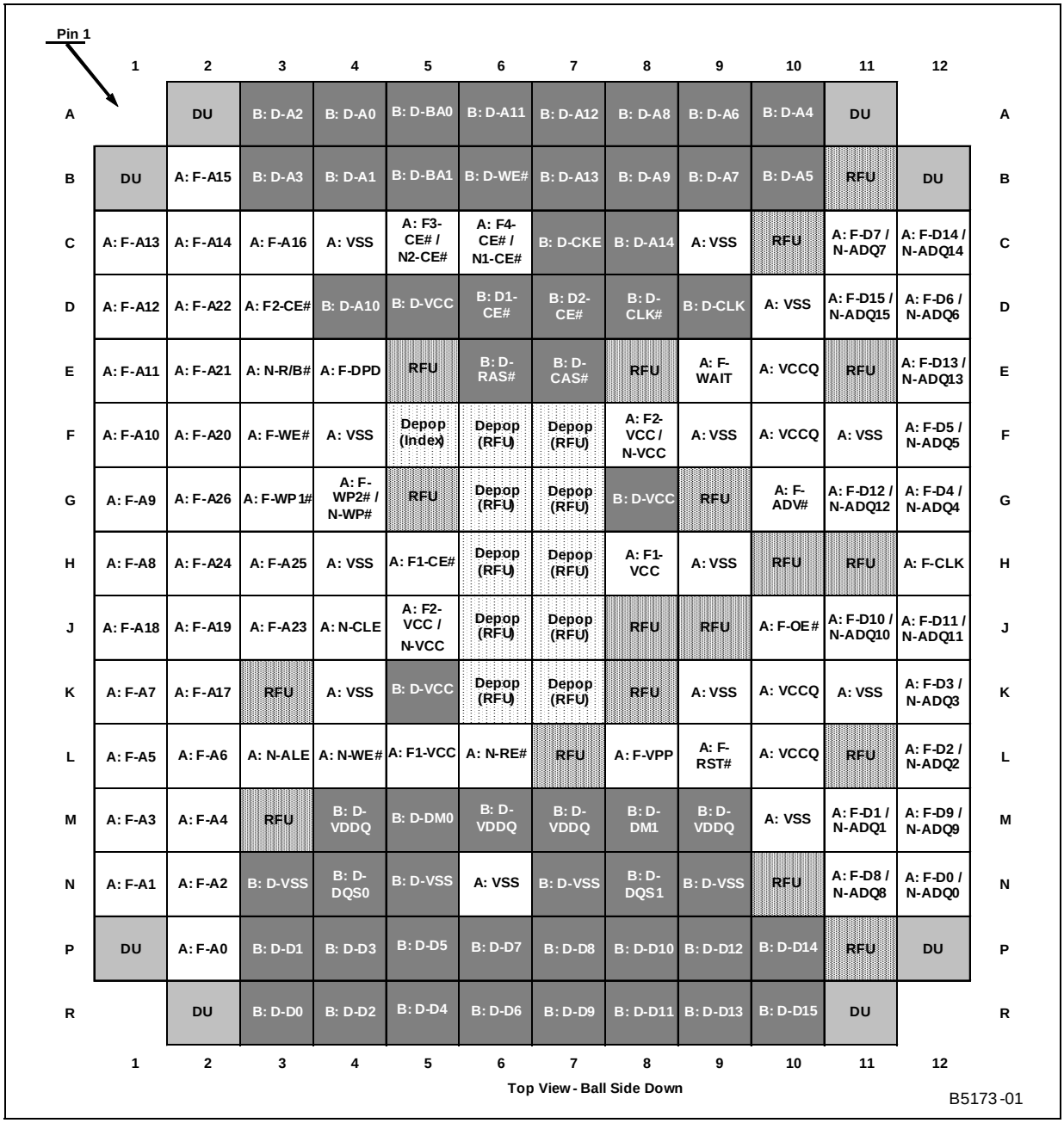
Symbol	Type	Signal Descriptions	Notes
N-ALE	Input	**NAND ADDRESS LATCH ENABLE:** NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of N-WE#.	1
N-RE#	Input	**NAND READ ENABLE:** NAND-specific signal; low-true input. When low, N-RE# enables the output drivers of the selected NAND die. When high, N-RE# disables the output drivers of the selected NAND die and places the output drivers in High-Z.	1, 2
N-RY/BY#	Output	**NAND READY/BUSY:** NAND-specific signal; low-true output. When low, N-RY/BY# indicates the NAND is busy performing a Read, Program, or Erase operation. When high, N-RY/BY# indicates the NAND device is ready.	1
N-WE#	Input	**NAND WRITE ENABLE:** NAND-specific signal; low-true input. When low, N-WE# enables Write operations for the enabled NAND die.	1, 4
P-CRE	Input	**PSRAM CONTROL REGISTER ENABLE:** Synchronous PSRAM-specific signal; high-true input. When high, P-CRE enables access to the Refresh Control Register (P-RCR) or Bus Control Register (P-BCR). When low, P-CRE enables normal Read or Write operations.	1, 3
P-MODE#	Input	**PSRAM MODE#:** Asynchronous only PSRAM-specific signal; low-true input. When low, P-MODE# enables access to the configuration register, and to enter or exit Low-Power mode. When high, P-MODE# enables normal Read or Write operations.	1, 3
P[2:1]-CS#	Input	**PSRAM CHIP SELECT:** PSRAM-specific signal; low-true input. When low, P-CS# selects the associated PSRAM memory die. When high, P-CS# deselects the associated PSRAM die. PSRAM die power is reduced to standby levels, and its data and WAIT outputs are placed in a High-Z state. • P1-CS# is dedicated to PSRAM die #1. • P2-CS# IS dedicated to PSRAM die #2. Otherwise, any unused PSRAM chip select should be treated as RFU.	1
S-CS1# S-CS2	Input	**SRAM CHIP SELECTS:** SRAM-specific signals; S-CS1# low-true input, S-CS2 high-true input. When both S-CS1# and S-CS2 are asserted, the SRAM die is selected. When either S-CS1# or S-CS2 is deasserted, the SRAM die is deselected.	1, 4
R-UB# R-LB#	Input	**RAM UPPER/LOWER BYTE ENABLES:** PSRAM- and SRAM-specific signals; low-true inputs. When low, R-UB# enables DQ[15:8] and R-LB# enables DQ[7:0] during PSRAM or SRAM Read and Write cycles. When high, R-UB# masks DQ[15:8] and R-LB# masks DQ[7:0].	1
Power Signals			
F-VPP	Power	**FLASH PROGRAM/ERASE VOLTAGE:** Flash specific. F-VPP supplies program or erase power to the flash die.	
F[2:1]-VCC	Power	**FLASH CORE POWER SUPPLY:** Flash specific. F[2:1]-VCC supplies the core power to the flash die. For NOR/NAND stacked device, F1-VCC is dedicated for all NOR dies, F2-VCC is dedicated for all NAND dies.	5
VCCQ	Power	**I/O POWER SUPPLY:** Global device I/O power. VCCQ supplies the device input/output driver voltage.	
P-VCC	Power	**PSRAM CORE POWER SUPPLY:** PSRAM specific. P-VCC supplies the core power to the PSRAM die.	1
S-VCC	Power	**SRAM POWER SUPPLY:** SRAM specific. S-VCC supplies the core power to the SRAM die.	1
VSS	Ground	**DEVICE GROUND:** Global ground reference for all signals and power supplies. Connect all VSS balls to system ground. Do not float any VSS connections.	
DU	—	**DO NOT USE:** Ball should not be connected to any power supplies, signals, or other balls. Ball can be left floating.	
RFU	—	**RESERVED for FUTURE USE:** Reserved by Numonyx for future device functionality and enhancement. Ball must be left floating.	

Notes:
1. Only available on stacked device combinations with NAND, SRAM, and/or LPSDRAM die. Otherwise treated as RFU.
2. F2-OE# and N-RE# share the same package ball at location H9. Only one signal function is available, depending on the stacked device combination.
3. P-CRE and P-MODE# share the same package ball at location K9. Only one signal function is available, depending on the stacked device combination.
4. S-CS1# and N-WE# share the same package ball at location J2. Only one signal function is available, depending on the stacked device combination.
5. The F2-VCC signal applies to a NAND flash die if one exists; if not, the F2-VCC signal applies to the NOR flash die.

4.5 Ballouts, x16 Split Bus

4.5.1 x16 Split Bus (165-Ball) Ballout, Non-Mux

Figure 16: x16 Split Bus (165 Active Ball) Electrical Ballout, Non-Mux



4.6 Signal Descriptions, x16 Split Bus

Table 9: Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 1 of 4)

Symbol	Type	Signal Descriptions	Notes
Address and Data Signals, Non-Mux			
F-A[MAX:0]	Input	FLASH ADDRESS: Flash device signals. Dedicated address inputs for Flash memory die during read and write operations. • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs are RFU.	
D-A[MAX:0]	Input	LPSDRAM ADDRESS: LSPDRAM device signals. Dedicated address inputs for LPSDRAM memory die during read and write operations. • A[12:0] are the row and A[9:0] are the column addresses for 512-Mbit LPSDRAM. • A[12:0] are the row and A[8:0] are the column addresses for 256-Mbit LPSDRAM. • A[11:0] are the row and A[8:0] are the column addresses for 128-Mbit LPSDRAM. Unused address inputs are RFU.	
F-DQ[15:0]	Input/ Output	FLASH DATA INPUT/OUTPUTS: Flash device signals. • Inputs Flash data and commands during write cycles. • Outputs data during read cycles. • Data signals are High-Z when the device is deselected or its output is disabled.	
D-DQ[15:0]	Input/ Output	LPSDRAM DATA INPUT/OUTPUTS: LPSDRAM device signals. • Inputs LPSDRAM data and commands during write cycles. • Outputs data during read cycles. • Data signals are High-Z when the device is deselected or its output is disabled.	
Address and Data Signals, A/D Mux			
F-A[MAX:16]	Input	ADDRESS: Flash device signals. Shared address inputs for all Flash memory die during Read and Write operations. • 2-Gbit: AMAX = A26 • 1-Gbit: AMAX = A25 • 512-Mbit: AMAX = A24 • 256-Mbit: AMAX = A23 • 128-Mbit: AMAX = A22 Unused address inputs should be treated as RFU.	
F-ADQ[15:0]	Input / Output	ADDRESS-DATA MULTIPLEXED INPUTS/ OUTPUTS: AD-Mux flash lower address and data signals; LPSDRAM data signals. During AD-Mux flash Write cycles, ADQ[15:0] are used to input the lower address followed by commands or write-data. During AD-Mux flash Read cycles, ADQ[15:0] are used to input the lower address followed by read-data output. During LPSDRAM accesses, ADQ[15:0] are used to input commands and write-data during Write cycles or to output read-data during Read cycles. During NAND accesses, ADQ[7:0] are used to input commands, address, or write-data, and to output read-data. ADQ[15:0] are High-Z when the flash is deselected or its output is disabled.	
Control Signals			

Table 9: Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 2 of 4)

Symbol	Type	Signal Descriptions	Notes
F-ADV#	Input	FLASH ADDRESS VALID: Flash-specific signal; low-true input. During synchronous flash Read operations, the address is latched on the rising edge of F-ADV#, or on the first rising edge of F-CLK after F-ADV# goes low for devices that support up to 108 MHz, or on the last rising edge of F-CLK after F-ADV# goes low for devices that support up to 133 MHz. In an asynchronous flash Read operation, the address is latched on the rising edge of F-ADV#.	
F[4:1]-CE#	Input	FLASH CHIP ENABLE: Flash-specific signal; low-true input. When low, F-CE# selects the associated flash memory die. When high, F-CE# deselects the associated flash die. Flash die power is reduced to standby levels, and its data and F-WAIT outputs are placed in a High-Z state. • F1-CE# is dedicated to flash die #1. • F[4:2]-CE# are dedicated to flash die #4 through #2, respectively, if present. Otherwise, treat any unused flash chip enable as RFU. • When NAND is used, F4-CE# is dedicated for NAND die 1 and NAND die 2. Otherwise, this is RFU.	
F-CLK	Input	FLASH CLOCK: Flash-specific signal; configurable active-edge input. F-CLK synchronizes the flash memory with the system clock during synchronous operations.	
D-CLK	Input	LPSDRAM CLOCK: LPSDRAM-specific signal; rising active-edge input. D-CLK synchronizes the LPSDRAM and DDR LPSDRAM with the system clock.	1
D-CLK#	Input	DDR LPSDRAM CLOCK: DDR LPSDRAM-specific signal; falling active-edge input. D-CLK# synchronizes the DDR LPSDRAM with the system clock.	1
F-OE#	Input	FLASH OUTPUT ENABLE: Flash-specific signal; low-true input. • When low, OE# enables the output drivers of the selected flash die. • When high, OE# disables the output drivers of the selected flash die and places the output drivers in High-Z.	
F-RST#	Input	FLASH RESET: Flash-specific signal; low-true input. • When low, F-RST# resets internal operations and inhibits writes. • When high, F-RST# enables normal operation.	
F-WAIT	Output	FLASH WAIT: Flash-specific signal; configurable-true output. When asserted, F-WAIT indicates invalid output data. • F-WAIT is driven whenever F-CE# and OE# is low. • F-WAIT is High-Z whenever F-CE# or OE# is high.	
F-WE#	Input	FLASH WRITE ENABLE: Flash-specific signal; low-true input. When low, WE# enables write operations for the selected flash die.	
N-WE#	Input	NAND WRITE ENABLE: NAND-specific signal; low-true input. When low, WE# enables write operations for the selected NAND die.	1
D-WE#	Input	LPSDRAM WRITE ENABLE: LPSDRAM-specific signal; low-true input. D-WE#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-RAS#, define the LPSDRAM command or operation. D-WE# is sampled on the rising edge of D-CLK.	1
F-WP[2:1]#	Input	FLASH WRITE PROTECT: Flash-specific signals; low-true inputs. When low, F-WP# enables the Lock-Down mechanism. When high, F-WP# overrides the Lock-Down function, enabling locked-down blocks to be unlocked with the Unlock command. • F-WP1# is dedicated to flash die #1. • F-WP2# is used for NAND die when available. Otherwise, this signal is for all other NOR die.	
F-DPD	Input	FLASH DEEP POWER-DOWN: Flash-specific signal; configurable-true input. When enabled in the ECR, F-DPD is used to enter or exit Deep Power-Down mode.	
N-CLE	Input	NAND COMMAND LATCH ENABLE: NAND-specific signal; high-true input. When high, N-CLE enables commands to be latched on the rising edge of WE#.	1
N-ALE	Input	NAND ADDRESS LATCH ENABLE: NAND-specific signal; high-true input. When high, N-ALE enables addresses to be latched on the rising edge of WE#.	1

Table 9: Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 3 of 4)

Symbol	Type	Signal Descriptions	Notes
N-R/B#	Output	NAND READY/BUSY: NAND-specific signal; low-true output. • When low, N-RY/BY# indicates the NAND device is busy performing a read, program, or erase operations. • When high, N-RY/BY# indicates the NAND device is ready.	1
N-RE#	Output	NAND READ ENABLE: NAND-specific signal; drives the data onto the flash bus after the falling edge of N-RE#. This signal increments the internal column address and reads out each data.	1
D-CKE	Input	LPSDRAM CLOCK ENABLE: LPSDRAM-specific signal; high-true input. • When high, D-CKE indicates that the next D-CLK edge is valid. • When low, D-CKE indicates that the next D-CLK edge is invalid and the selected LPSDRAM die is suspended.	1
D-BA[1:0]	Input	LPSDRAM BANK SELECT: LPSDRAM-specific input signals. D-BA[1:0] selects one of four banks in the LPSDRAM die.	1
D-RAS#	Input	LPSDRAM ROW ADDRESS STROBE: LPSDRAM-specific signal; low-true input. D-RAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-RAS# is sampled on the rising edge of D-CLK.	1
D-CAS#	Input	LPSDRAM COLUMN ADDRESS STROBE: LPSDRAM-specific signal; low-true input. D-CAS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-CS#, D-RAS#, and D-WE#, define the LPSDRAM command or operation. D-CAS# is sampled on the rising edge of D-CLK.	1
D[2:1]-CE#	Input	LPSDRAM CHIP ENABLE: LPSDRAM-specific signal; low-true input. When low, D-CS# selects the associated LPSDRAM memory die and starts the command input cycle. When D-CS# is high, commands are ignored but operations continue. • D-CS#, together with A[MAX:0], D-BA[1:0], D-CKE, D-RAS#, D-CAS#, and D-WE#, define the LPSDRAM command or operation. D-CS# is sampled on the rising edge of D-CLK. • D[2:1]-CS# are dedicated to LPSDRAM die #2 and die #1, respectively, if present. Otherwise, treat any unused LPSDRAM chip selects as RFU.	1
D-DM[1:0]	Input	LPSDRAM DATA MASK: LPSDRAM-specific signal; high-true input. When high, D-DM[1:0] controls masking of input data during writes and output data during reads. • D-DM1 corresponds to the data on DQ[15:8]. • D-DM0 corresponds to the data on DQ[7:0].	1
D-DQS1 D-DQS0	Input / Output	LPSDRAM UPPER/LOWER DATA STROBE: DDR LPSDRAM-specific input/output signals. D-DQS1 and D-DQS0 provide as output the read data strobes, and as input the write data strobes. • D-DQS1 corresponds to the data on DQ[15:8]. • D-DQS0 corresponds to the data on DQ[7:0].	1
S-CS1# S-CS2#	Input	SRAM CHIP SELECTS: SRAM-specific signals. • S-CS1# low-true input. • S-CS2# high-true input. • When both are asserted, S-CS1# and S-CS2 select the SRAM die. • When either is deasserted, the SRAM die is deselected and its power is reduced to standby levels.	3
S-UB# S-LB#	Input	SRAM UPPER/LOWER BYTE ENABLES: SRAM-specific signals; low-true inputs. • When low, S-UB# enables DQ[15:8] and S-LB# enables DQ[7:0] during SRAM read and write cycles. • When high, S-UB# masks DQ[15:8] and S-LB# masks DQ[7:0].	2,3
Power Signals			
F-VPP	Power	FLASH PROGRAM/ERASE VOLTAGE: Flash specific. F-VPP supplies program or erase power to the flash die.	

Table 9: Signal Descriptions, x16 Split Bus, Non-Mux (Sheet 4 of 4)

Symbol	Type	Signal Descriptions	Notes
F[2:1]-VCC	Power	FLASH CORE POWER SUPPLY: Flash specific. F-VCC supplies the core power to the flash die. • F1-VCC is dedicated for NOR die. • F2-VCC is used for NAND die when available. Otherwise, this signal is for NOR die. (When NAND is available, the F2-VCC signal is named N-VCC.)	
D-VCC	Power	LPSDRAM CORE POWER SUPPLY: LPSDRAM specific. D-VCC supplies the core power to the LPSDRAM die.	1
S-VCC	Power	SRAM POWER SUPPLY: SRAM specific. S-VCC supplies the core power to the SRAM die.	
VCCQ	Power	FLASH I/O POWER SUPPLY: Global device I/O power. VCCQ supplies the device input/output driver voltage to the flash die.	
D-VDDQ	Power	LPSDRAM I/O POWER SUPPLY: Global device I/O power. VDDQ supplies the device input/output driver voltage to the LPSDRAM die.	1
VSS	Ground	FLASH DEVICE GROUND: Global ground reference for all flash signals and power supplies. Connect all A: VSS balls to system ground. Do not float any VSS connections.	
D-VSS	Ground	LPSDRAM DEVICE GROUND: Global ground reference for all LPSDRAM signals and power supplies. Connect all B: D-VSS balls to system ground. Do not float any VSS connections.	1
DU	—	DO NOT USE: Do not connect this ball to any power supplies, signals, or other balls. This ball can be left floating.	
RFU	—	RESERVED for FUTURE USE: Reserved by Numonyx for future device functionality and enhancement. This ball must be left floating.	

Notes:
6. Available only on stacked device combinations with NAND, and/or LPSDRAM die. Otherwise, treat the signal as RFU.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only.

NOTICE: This document contains information available at the time of its release. The specifications are subject to change without notice. Verify with your local Numonyx sales office that you have the latest datasheet before finalizing a design.

Table 10: Absolute Maximum Ratings

Parameter	Min	Max	Unit	Conditions	Notes
Temperature under Bias Expanded	–30	+85	°C	—	1
Storage Temperature	–65	+125	°C	—	1
F-VCC Voltage	–2.0	V_{CCQ} + 2.0	V	—	2,3
VCCQ and P-VCC Voltage	–2.0	V_{CCQ} + 2.0	V	—	2,4
Voltage on any input/output signal (except VCC, VCCQ,and VPP)	–2.0	V_{CCQ} + 2.0	V	—	2,4
F-VPP Voltage	–2.0	+11.5	V	—	2,3
I_{SH} Output Short Circuit Current	—	100	mA	—	5
V_{PPH} Time	—	80	Hours		6
Block Program/Erase Cycles: Main Blocks	100,000	—	Cycles	F-VPP = V_{CC} or F-VPP = V_{PPH}	6

Notes:
1. Temperature is Ambient, not Case.
2. Voltage is referenced to V_{SS}.
3. During signal transitions, minimum DC voltage may undershoot to –2.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CC} (max) + 2.0 V for periods < 20 ns.
4. During signal transitions, minimum DC voltage may undershoot to –1.0 V for periods < 20 ns; maximum DC voltage may overshoot to V_{CCQ} (max) + 1.0 V for periods < 20 ns.
5. Output shorted for no more than one second. No more than one output shorted at a time.
6. Operation beyond this limit may degrade performance.

5.2 Operating Conditions

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 11: Operating Conditions

Symbol	Description	Min	Max	Unit	Conditions
T_C	Operating Temperature (Case Temperature)	–30	+85	°C	—
V_{CC}	VCC Supply Voltage	+1.7	+2.0	V	—
V_{CCQ}	I/O Supply Voltage	+1.7	+2.0	V	—
V_{PPL}	Programming Voltage (Logic Level)	+0.9	+2.0	V	—
V_{PPH}	Factory Programming Voltage (High Level)	+8.5	+9.5	V	—

6.0 Electrical Characteristics

6.1 Initialization

Proper device initialization and operation is dependent on the power-up/down sequence, reset procedure, and adequate power-supply decoupling. The following sections describe each of these areas.

6.1.1 Power-Up/Down Characteristics

To prevent conditions that could result in spurious program or erase operations, the power-up/power-down sequence shown in Table 12 is recommended. Note that each power supply must reach its minimum voltage range before applying/removing the next supply voltage.

Table 12: Power-Up/Down Sequence

<table>
<tr><th>Power Supply Voltage</th><th colspan="4">Power-Up Sequence</th><th colspan="4">Power-Down Sequence</th></tr>
<tr><td>$V_{CC(min)}$</td><td>1st</td><td>1st</td><td rowspan="2">1st*</td><td rowspan="3">Sequencing not required*</td><td>3rd</td><td>2nd</td><td rowspan="2">2nd*</td><td rowspan="3">Sequencing not required*</td></tr>
<tr><td>$V_{CCQ(min)}$</td><td>2nd</td><td rowspan="2">2nd*</td><td>2nd</td><td rowspan="2">1st*</td></tr>
<tr><td>$V_{PP(min)}$</td><td>3rd</td><td>2nd</td><td>1st</td><td>1st</td></tr>
</table>

* Power supplies connected or sequenced together.

Device inputs must not be driven until all supply voltages reach their minimum range. RST# should be low during power transitions.

Note: If VCCQ is below VLKOQ, the device is reset.

6.1.2 Reset Characteristics

During power-up and power-down, RST#should be asserted to prevent spurious program or erase operations. While RST#is low, device operations are disabled; all inputs such as address and control are ignored; and all outputs such as data and WAIT are placed in High-Z. Invalid bus conditions are effectively masked out.

Upon power-up, RST#can be deasserted after tVCCPH, allowing the device to exit from reset. Upon exiting from reset, the device defaults to asynchronous Read Array mode, and the Status Register defaults to 0080h. Array data is available after tPHQV, or a bus-write cycle can begin after tPHWL.

If RST#is asserted during a program or erase operation, the operation will abort and array contents at that location will be invalid.

For proper system initialization, connect RST#to the low-true reset signal that asserts whenever the processor is reset. This will ensure the flash device is in the expected read mode (i.e., Read Array) upon startup.

6.1.3 Power Supply Decoupling

High-speed flash memories require adequate power-supply decoupling to prevent external transient noise from affecting device operations, and to prevent internally-generated transient noise from affecting other devices in the system.

Ceramic chip capacitors of 0.01 to 0.1 µF capacitors should be used between all VCC, VCCQ, VPPsupply connections and system ground. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the device package, or on the opposite side of the printed circuit board close to the center of the device-package footprint.

Larger (4.7 µF to 33.0 µF) electrolytic or tantulum bulk capacitors should also be distributed as needed throughout the system to compensate for voltage sags caused by circuit trace inductance.

Transient current magnitudes depend on the capacitive and inductive loading on the device's outputs. For best signal integrity and device performance, high-speed design rules should be used when designing the printed-circuit board. Circuit-trace impedances should match output-driver impedance with adequate ground-return paths. This will help minimize signal reflections (overshoot/undershoot) and noise caused by high-speed signal edge rates.

6.2 DC Current Specifications

The M18 device includes specifications for different lithographies, densities, and frequencies. For additional information on combinations, see Table 4, "M18 Product Litho/Density/Frequency Combinations" on page 10 in the Section 2.0, "Functional Description".

Table 13: DC Current Specifications (Sheet 1 of 3)

Sym	Parameter	Litho (nm)	Density (Mbit)	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{LI}	Input Load Current			—	±1	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	1
I_{LO}	Output Leakage Current			—	±1	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max V_{IN} = V_{CCQ} or V_{SS}	
I_{CCS}	V_{CC} Standby	90	256	35	95	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max CE# = V_{CCQ} RST# = V_{CCQ} or GND (for I_{CCS}) WP# = V_{IH}	1,2
			512	50	120			
		65	128	45	115			
			256	50	130			
			512	60	160			
			1,024	70	185			
I_{CCAPS}	APS	90	256	35	95	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max CE# = V_{SSQ} RST# = V_{CCQ} All inputs are at rail to rail (V_{CCQ} or V_{SSQ}).	—
			512	50	120			
		65	128	45	115			
			256	50	130			
			512	60	160			
			1,024	70	185			

Table 13: DC Current Specifications (Sheet 2 of 3)

Sym	Parameter	Litho (nm)	Density (Mbit)	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{DPD}	DPD			2	30	µA	V_{CC} = V_{CC} Max V_{CCQ} = V_{CCQ} Max CE# = V_{CCQ} RST# = V_{CCQ} ECR[15] = V_{CCQ} DPD = V_{CCQ} or V_{SSQ} All inputs are at rail to rail (V_{CCQ} or V_{SSQ}).	8
I_{CCR}	Average V_{CC} Read: Asynchronous Single Word Read f = 5 MHz, (1 CLK)			25	30	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3,4,5
I_{CCR}	Average V_{CC} Read: Page Mode Read f = 13 MHz, (17 CLK)	Burst = 16 Word		11	15	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3,4,5
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 66 MHz, LC = 7	Burst = 8 Word		22	32	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3,4,5
		Burst = 16 Word		19	26	mA		
		Burst = Continuous		25	34	mA		
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 108 MHz, LC = 10	Burst = 8 Word		26	36	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3,4,5
		Burst = 16 Word		23	30	mA		
		Burst = Continuous		30	42	mA		
I_{CCR}	Average V_{CC} Read: Synchronous Burst Read f = 133 MHz, LC = 13	Burst = 8 Word		26	35	mA	V_{CC} = V_{CC}MAX CE# = V_{IL} OE# = V_{IH} Inputs: V_{IL} or V_{IH}	1,3,4,5
		Burst = 16 Word		24	33	mA		
		Burst = Continuous		33	46	mA		
I_{CCW}, I_{CCE} I_{CCBC}	V_{CC} Program V_{CC} Erase V_{CC} Blank Check			35	50	mA	V_{PP} = V_{PPL} or V_{PP} = V_{PPH}, program/erase in progress	1,3,4,5,7
I_{CCWS}, I_{CCES}	V_{CC} Program Suspend V_{CC} Erase Suspend	90	256	35	95	µA	CE# = V_{CCQ}; suspend in progress	1,3,6
			512	50	120			
		65	128	45	115			
			256	50	130			
			512	60	160			
			1,024	70	185			
I_{PPS}, I_{PPWS}, IPPES	V_{PP} Standby V_{PP} Program Suspend V_{PP} Erase Suspend			0.2	5	µA	V_{PP} = V_{PPL}; suspend in progress	3
I_{PPR}	V_{PP} Read			2	15	µA	$V_{PP} \leq V_{CC}$	3
I_{PPW}	V_{PP} Program			0.05	0.1	mA	V_{PP} = V_{PPL} = V_{PPH}, program in progress	3

Table 13: DC Current Specifications (Sheet 3 of 3)

Sym	Parameter	Litho (nm)	Density (Mbit)	1.7 V – 2.0 V		Unit	Test Conditions	Notes
				Typ	Max			
I_{PPE}	V_{PP} Erase			0.05	0.1	mA	$V_{PP} = V_{PPL} = V_{PPH}$, erase in progress	3
I_{PPBC}	V_{PP} Blank Check			0.05	0.1	mA	$V_{PP} = V_{PPL} = V_{PPH}$, blank check in progress	3

Notes:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_C = +25 °C.
2. I_{CCS} is the average current measured over any 5 ms time interval 5 µs after CE# is deasserted.
3. Sampled, not 100% tested.
4. V_{CC} read + program current is the sum of V_{CC} read and V_{CC} program currents.
5. V_{CC} read + erase current is the sum of V_{CC} read and V_{CC} erase currents.
6. I_{CCES} is specified with the device deselected. If device is read while in erase suspend, current is I_{CCES} plus I_{CCR}
7. I_{CCW}, I_{CCE} measured over typical or max times specified in Section 7.4, “Program and Erase Characteristics” on page 68
8. I_{DPD} is the current measured 40 µs after entering DPD.

6.3 DC Voltage Specifications

Table 14: DC Voltage Specifications

Symbol	Parameter	V_{CCQ}	1.7 V – 2.0 V		Unit	Test Condition	Notes
			Min	Max			
V_{IL}	Input Low Voltage		0	0.4	V	—	1
V_{IH}	Input High Voltage		V_{CCQ} –0.4	V_{CCQ}		—	—
V_{OL}	Output Low Voltage		—	0.1		$V_{CC} = V_{CC}MIN$ $V_{CCQ} = V_{CCQ}MIN$ I_{OL} = 100 µA	—
V_{OH}	Output High Voltage		V_{CCQ} –0.1	—		$V_{CC} = V_{CC}MIN$ $V_{CCQ} = V_{CCQ}MIN$ I_{OH} = –100 µA	—
V_{PPLK}	V_{PP} Lock-Out Voltage		—	0.4		—	2
V_{LKO}	V_{CC} Lock Voltage		1.0	—		—	—
V_{LKOQ}	V_{CCQ} Lock Voltage		0.9	—		—	—

Notes:
1. During signal transitions, voltage can undershoot to –1.0 V and overshoot to maximum V_{CCQ}+1.0 V for durations of < 2 ns.
2. $V_{PP} \le V_{PPLK}$ inhibits erase and program operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.

6.4 Capacitance

Table 15: Capacitance

Symbol	Parameter	Min	Typ	Max	Unit	Condition	Notes
C_{IN}	Input Capacitance (Address, CLK, CE#, OE#, ADV#, WE#, WP#, DPD and RST#)	2	4	6	pF	V_{IN} = 0 - 2.0 V	1,2
C_{OUT}	Output Capacitance (Data and WAIT)	2	5	6		V_{OUT} = 0 - 2.0 V	

Notes:
1. T_C = +25°C, f = 1 MHz.
2. Sampled, not 100% tested.
3. Silicon die capacitance only. Add 1 pF for discrete packages; for SCSP total capacitance equals 2 pF + sum of silicon die capacitance.

7.0 NOR Flash AC Characteristics

Timing symbols used in the timing diagrams within this document conform to the following conventions:

Figure 17: Timing Symbol Notation Convention

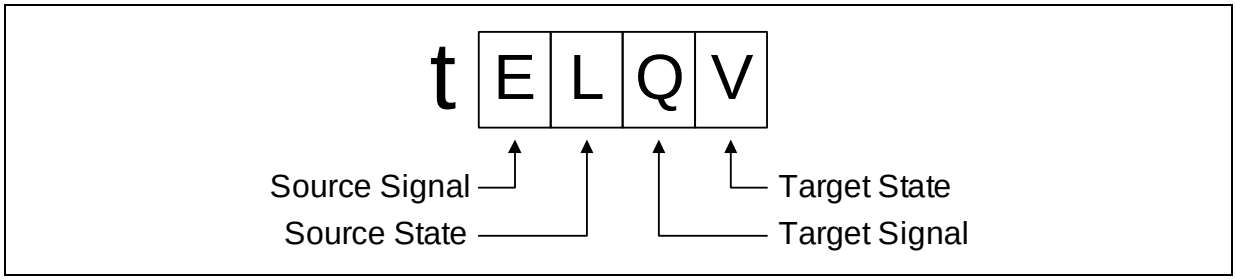


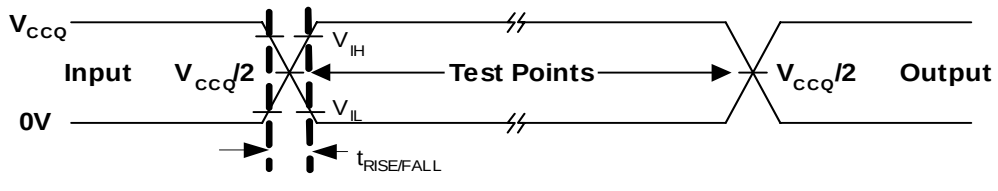
Table 16: Codes for Timing Signals and Timing States

Signal	Code	State	Code
Address	A	High	H
Data - Read	Q	Low	L
Data - Write	D	High-Z	Z
Chip Enable (CE#)	E	Low-Z	X
Output Enable (OE#)	G	Valid	V
Write Enable (WE#)	W	Invalid	I
Address Valid (ADV#)	V	—	—
Reset (RST#)	P	—	—
Clock (CLK)	C	—	—
WAIT	T	—	—

Note: Exceptions to this conventions include tACC and tAPA. tACC is a generic timing symbol that refers to the aggregate initial-access delay as determined by tAVQV, tELQV, and tGLQV (whichever is satisfied last) of the flash device. tAPA is specified in the flash device datasheet, and is the address-to-data delay for subsequent page-mode reads.

7.1 AC Test Conditions

Figure 18: AC Input/Output Reference Waveform

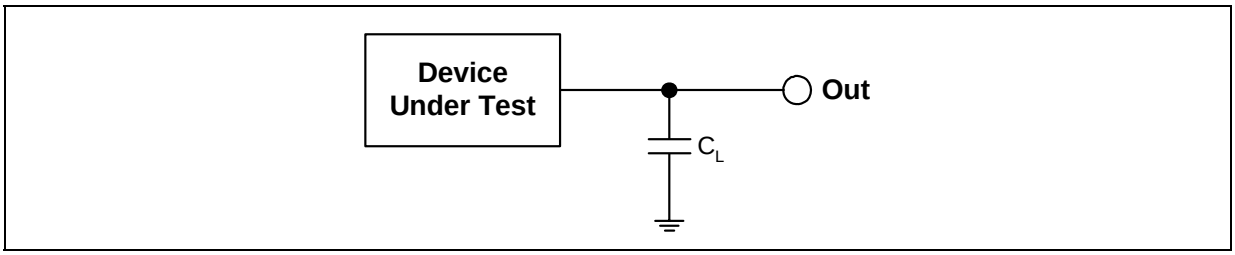


Note: AC test inputs are driven at V_{CCQ} for Logic '1' and 0.0 V for Logic '0'. Input/output timing begins and ends at $V_{CCQ}/2$.

Table 17: AC Input Requirements

Symbol	Parameter	Frequency	Min	Max	Unit	Condition
$t_{RISE/FALL}$	Inputs rise/fall time (Address, CLK, CE#, OE#, ADV#, WE#, WP#)	@133MHz, 108MHz	0.3	1.2	ns	V_{IL} to V_{IH} or V_{IH} to V_{IL}
		@66MHz	0	3		
t_{ASKW}	Address-Address skew		0	3		At $V_{CCQ}/2$

Figure 19: Transient Equivalent Testing Load Circuit

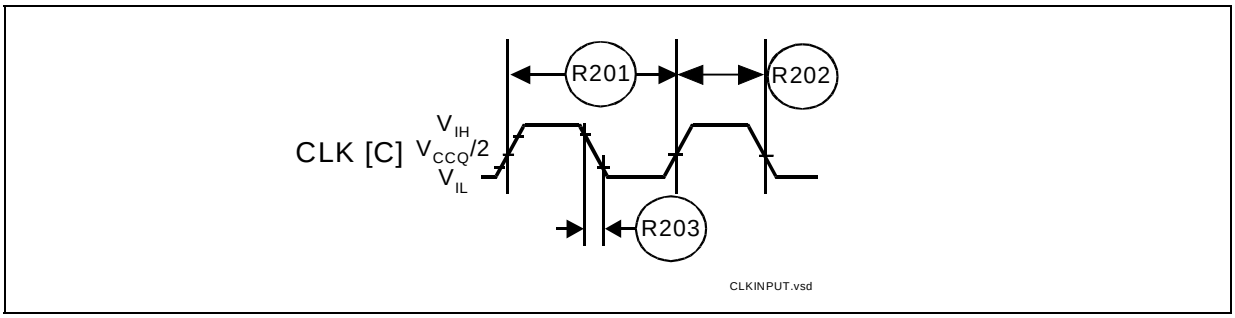


Notes:
1. See the following table for component values.
2. Test configuration component value for worst case speed conditions.
3. C_L includes jig capacitance.

Table 18: Test Configuration Component Value for Worst Case Speed Conditions

Test Configuration	C_L (pF)
1.7 V Standard Test	30
2.0 V Standard Test	30

Figure 20: Clock Input AC Waveform



7.2 Read Specifications

Read specifications for 108 MHz and 133 MHz M18 devices are included here. For additional information on lithography, density, and frequency combinations, see Table 4, “M18 Product Litho/Density/Frequency Combinations” on page 10 in the Section 2.0, “Functional Description.

Devices which support frequencies up to 133 MHz must meet additional timing specifications for synchronous reads (for address latching with CLK) as listed in Table 20, “AC Read, 133 MHz, VCCQ = 1.7 V to 2.0 V” on page 51.

Table 19: AC Read, 108 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 1 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Unit	Notes
			Min	Max		
Asynchronous Specifications						
R1	t_{AVAV}	Read cycle time	96	—	ns	—
R2	t_{AVQV}	Address to output valid	—	96	ns	—
R3	t_{ELQV}	CE# low to output valid	—	96	ns	—
R4	t_{GLQV}	OE# low to output valid	—	20	ns	2
R5	t_{PHQV}	RST# high to output valid	—	150	ns	—
R6	t_{ELQX}	CE# low to output in low-Z	0	—	ns	3
R7	t_{GLQX}	OE# low to output in low-Z	0	—	ns	2,3
R8	t_{EHQZ}	CE# high to output in high-Z	—	9	ns	3
R9	t_{GHQZ}	OE# high to output in high-Z	—	9	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change	0	—	ns	
R11	t_{EHEL}	CE# pulse width high	7	—	ns	—
R12	t_{ELTV}	CE# low to WAIT valid	—	11	ns	—
R13	t_{EHTZ}	CE# high to WAIT high Z	—	9	ns	3
R14	t_{GHTV}	OE# high to WAIT valid (AD-Mux only)	—	7	ns	—
R15	t_{GLTV}	OE# low to WAIT valid	—	7	ns	—
R16	t_{GLTX}	OE# low to WAIT in low-Z	0	—	ns	3
R17	t_{GHTZ}	OE# low to WAIT in high-Z (non-mux only)	0	9	ns	3
Latching Specifications						
R101	t_{AVVH}	Address setup to ADV# high	5	—	ns	—
R102	t_{ELVH}	CE# low to ADV# high	9	—	ns	—
R103	t_{VLQV}	ADV# low to output valid	—	96	ns	—
R104	t_{VLVH}	ADV# pulse width low	7	—	ns	—
R105	t_{VHVL}	ADV# pulse width high	7	—	ns	—
R106	t_{VHAX}	Address hold from ADV# high	5	—	ns	4
R107	t_{VHGL}	ADV# high to OE# low (AD-Mux only)	7	—	ns	—
R108	t_{APA}	Page address access (non-mux only)	—	15	ns	—
R111	t_{PHVH}	RST# high to ADV# high	30	—	ns	—
Clock Specifications						
R200	f_{CLK}	CLK frequency	—	108	MHz	—
R201	t_{CLK}	CLK period	9.26	—	ns	—
R202	$t_{CH/CL}$	CLK high/low time	0.45	0.55	CLK period	—
R203	$t_{FCLK/RCLK}$	CLK fall/rise time	0.3	1.2	ns	—
Synchronous Specifications						
R301	t_{AVCH}	Address setup to CLK high	5	—	ns	—
R302	t_{VLCH}	ADV# low setup to CLK high	5	—	ns	—

Table 19: AC Read, 108 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 2 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Unit	Notes
			Min	Max		
R303	t_{ELCH}	CE# low setup to CLK high	5	—	ns	—
R304	t_{CHQV}	CLK to output valid	—	7	ns	—
R305	t_{CHQX}	Output hold from CLK high	2	—	ns	—
R306	t_{CHAX}	Address hold from CLK high	5	—	ns	4
R307	t_{CHTV}	CLK high to WAIT valid	—	7	ns	—
R311	t_{CHVL}	CLK high to ADV# Setup	2	—	ns	—
R312	t_{CHTX}	WAIT hold from CLK	2	—	ns	—

Notes:
1. See Figure 18, "AC Input/Output Reference Waveform" on page 48 for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.
4. Address hold in synchronous burst mode is t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.

Table 20: AC Read, 133 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 1 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Units	Notes
			Min	Max		
Asynchronous Specifications						
R1	t_{AVAV}	Read cycle time	96	—	ns	—
R2	t_{AVQV}	Address to output valid	—	96	ns	—
R3	t_{ELQV}	CE# low to output valid	—	96	ns	—
R4	t_{GLQV}	OE# low to output valid	—	7	ns	2
R5	t_{PHQV}	RST# high to output valid	—	150	ns	—
R6	t_{ELQX}	CE# low to output in low-Z	0	—	ns	3
R7	t_{GLQX}	OE# low to output in low-Z	0	—	ns	2,3
R8	t_{EHQZ}	CE# high to output in high-Z	—	7	ns	3
R9	t_{GHQZ}	OE# high to output in high-Z	—	7	ns	
R10	t_{OH}	Output hold from first occurring address, CE#, or OE# change	0	—	ns	
R11	t_{EHEL}	CE# pulse width high	7	—	ns	—
R12	t_{ELTV}	CE# low to WAIT valid	—	8	ns	—
R13	t_{EHTZ}	CE# high to WAIT high Z	—	7	ns	3
R14	t_{GHTV}	OE# high to WAIT valid (AD-Mux only)	—	5.5	ns	—
R15	t_{GLTV}	OE# low to WAIT valid	—	5.5	ns	—
R16	t_{GLTX}	OE# low to WAIT in low-Z	0	—	ns	3
R17	t_{GHTZ}	OE# high to WAIT in high-Z (non-mux only)	0	7	ns	3
Latching Specifications						
R101	t_{AVVH}	Address setup to ADV# high	5	—	ns	—
R102	t_{ELVH}	CE# low to ADV# high	7	—	ns	—
R103	t_{VLQV}	ADV# low to output valid		96	ns	—

Table 20: AC Read, 133 MHz, V_{CCQ} = 1.7 V to 2.0 V (Sheet 2 of 2)

Nbr.	Symbol	Parameter[1]	96 ns		Units	Notes
			Min	Max		
R104	t_{VLVH}	ADV# pulse width low	7	—	ns	—
R105	t_{VHVL}	ADV# pulse width high	7	—	ns	—
R106	t_{VHAX}	Address hold from ADV# high	5	—	ns	—
R107	t_{VHGL}	ADV# high to OE# low (AD-Mux only)	2	—	ns	—
R108	t_{APA}	Page address access (non-mux only)	—	15	ns	—
R111	t_{PHVH}	RST# high to ADV# high	30	—	ns	—
Clock Specifications						
R200	f_{CLK}	CLK frequency	—	133	MHz	—
R201	t_{CLK}	CLK period	7.5	—	ns	—
R202	$t_{CH/CL}$	CLK high/low time	0.45	0.55	CLK Period	4
R203	$t_{FCLK/RCLK}$	CLK fall/rise time	0.3	1.2	ns	—
Synchronous Specifications						
R301	t_{AVCH}	Address setup to CLK high	2	—	ns	—
R302	t_{VLCH}	ADV# low setup to CLK high	2	—	ns	—
R303	t_{ELCH}	CE# low setup to CLK high	2.5	—	ns	—
R304	t_{CHQV}	CLK to output valid	—	5.5	ns	—
R305	t_{CHQX}	Output hold from CLK high	2	—	ns	—
R306	t_{CHAX}	Address hold from CLK high	2	—	ns	—
R307	t_{CHTV}	CLK high to WAIT valid	—	5.5	ns	—
R311	t_{CHVL}	CLK high to ADV# Setup	2	—	ns	—
R312	t_{CHTX}	WAIT hold from CLK high	2	—	ns	—
R313	t_{CHVH}	ADV# hold from CLK high	2	—	ns	—
R314	t_{CHGL}	CLK to OE# low (AD-Mux only)	2	—	ns	—
R315	t_{ACC}	Read access time from address latching clock	96	—	ns	—
R316	t_{VLVH}	ADV# pulse width low for sync reads	1	2	clks	—
R317	t_{VHCH}	ADV# high to CLK high	2	—	ns	—

Notes:
1. See Figure 18, "AC Input/Output Reference Waveform" on page 48 for timing measurements and maximum allowable input slew rate.
2. OE# may be delayed by up to $t_{ELQV} - t_{GLQV}$ after CE#'s falling edge without impact to t_{ELQV}.
3. Sampled, not 100% tested.

7.2.1 Read Timing Waveforms

The following sections show the timing waveforms for Asynchronous and Synchronous read specifications for Non-Mux and AD-Mux M18 devices.

The Synchronous read timing waveforms apply to both the 108 and 133 MHz devices. However please note that M18 devices which only support up to 108 MHz need not meet the R313 to R317 timing specifications.

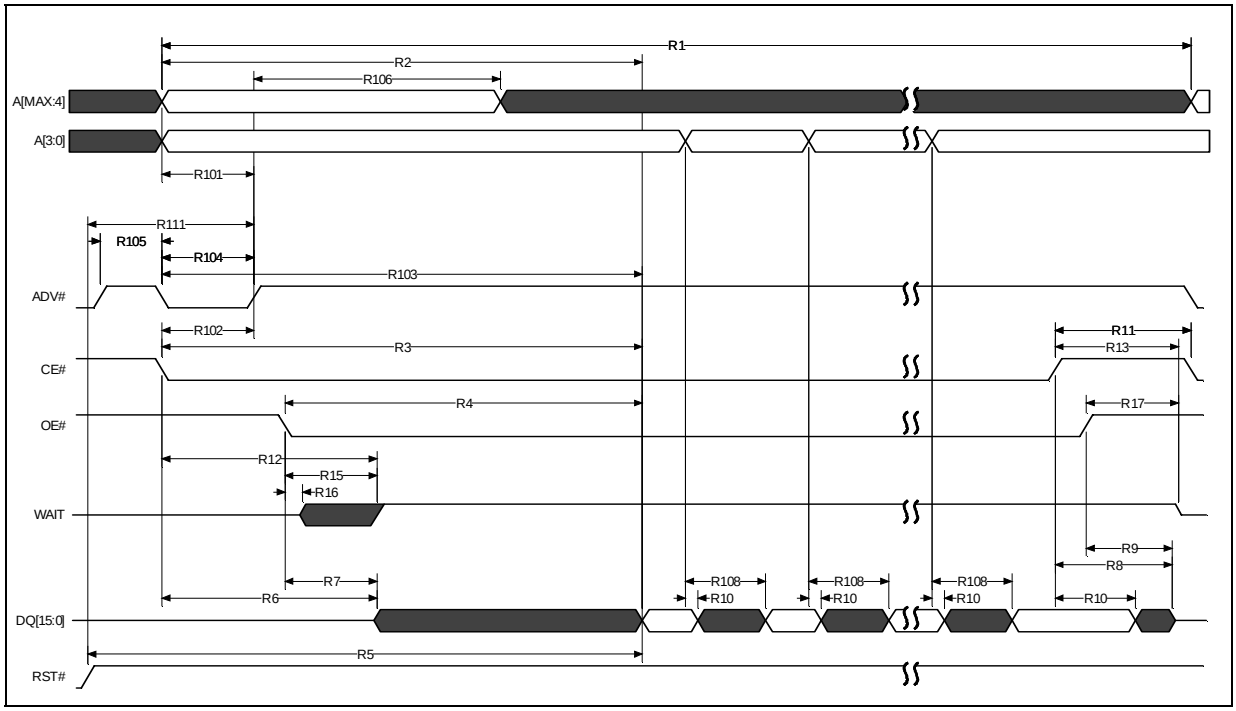
Please note that the WAIT signal polarity in all the timing waveforms is low-true (RCR10 = 0). WAIT is shown as de-asserted with valid data (RCR8 = 0). WAIT is de-asserted during asynchronous reads.

Table 21: List of Read Timing waveforms

M18 Device	Description
Non-Mux	Async Page-Mode Read
	Synchronous 8- or 16-word Burst Read
	Synchronous Continuous Mis-aligned Burst Read
	Synchronous Burst with Burst-Interrupt
ADMux	Async Single-Word Read
	Synchronous 8- or 16-word Burst Read
	Synchronous Continuous Mis-aligned Burst Read
	Synchronous Burst with Burst-Interrupt

7.2.2 Timings: Non-Mux Device, Async Read

Figure 21: Async Page-Mode Read (Non-Mux)



7.2.3 Timings: Non-Mux Device, Sync Read

Figure 22: Sync Single-Word Array / Non-Array Read, 108 MHz

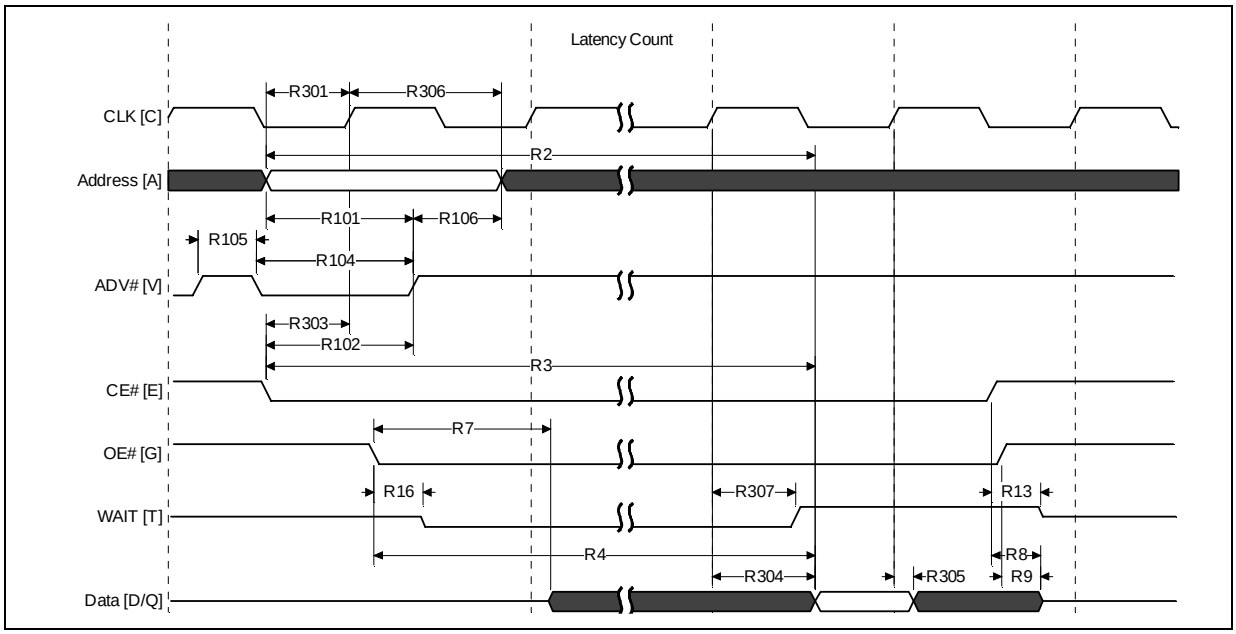
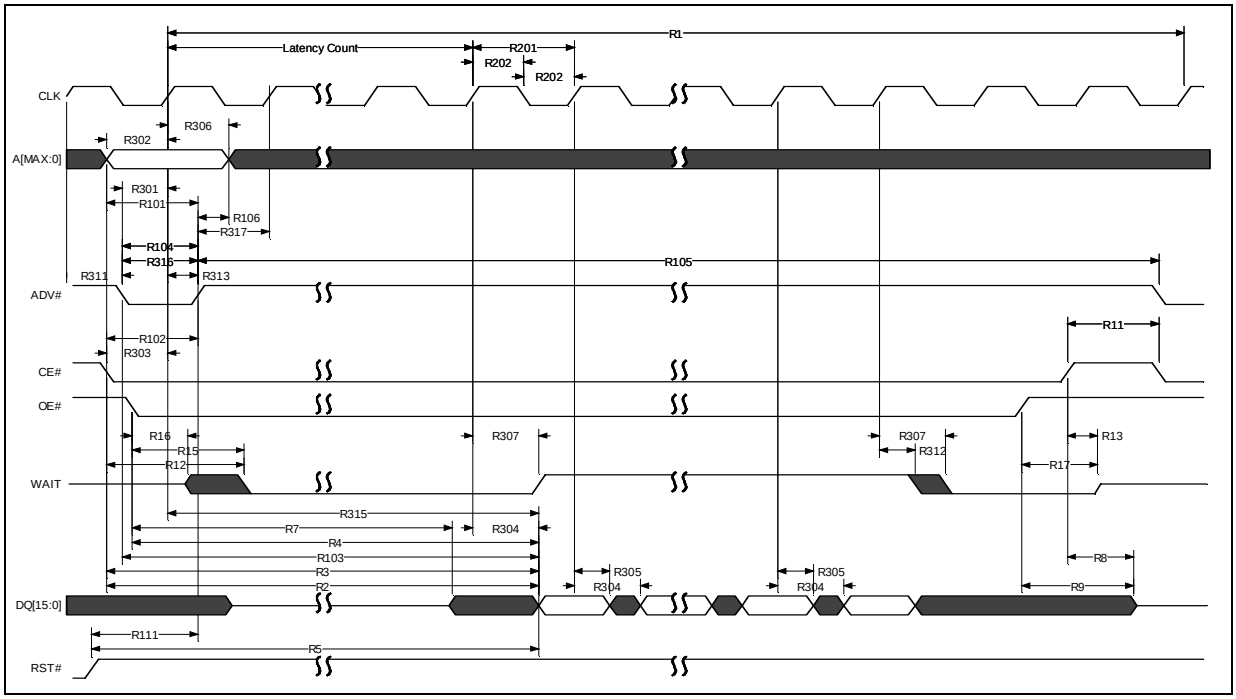


Figure 23: Synchronous 8- or 16-word Burst Read (Non-Mux)

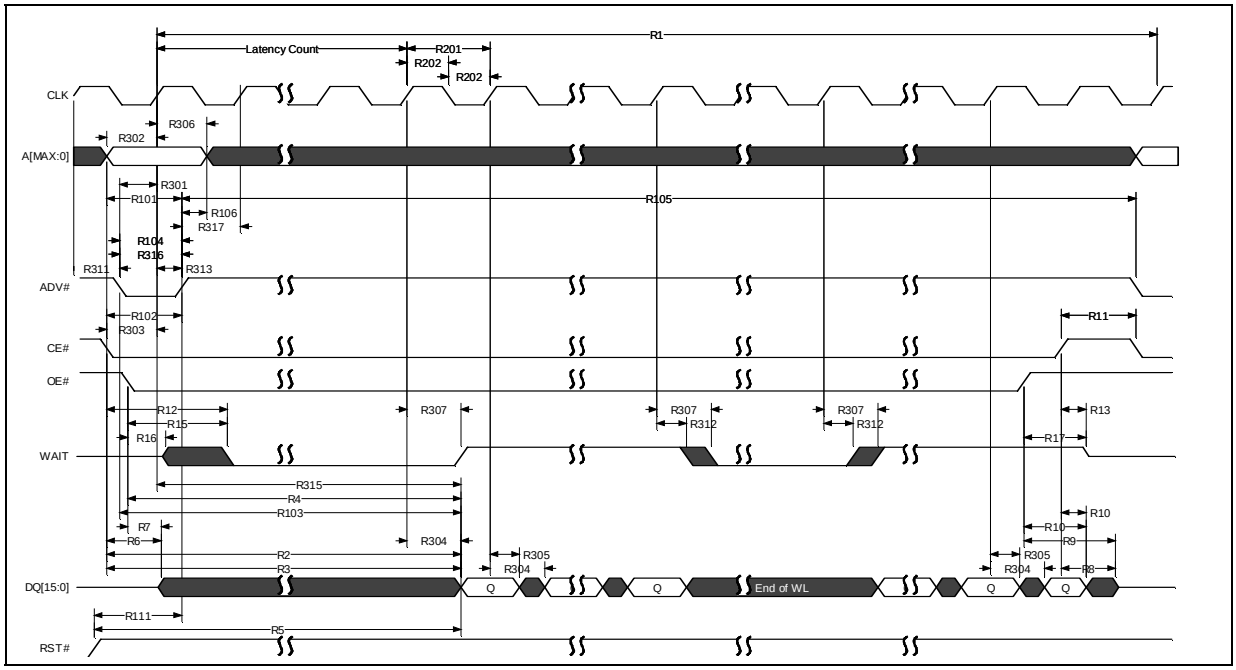


Notes:

1. 8-word and 16-word burst are always wrap-only.

2. R2, R3 and R103 apply to legacy-latching only; R315 and R316 apply to clock-only latching only.
3. For legacy-latching (ADV# OR CLK latching), ADV# can be held low throughout the synchronous read operation.

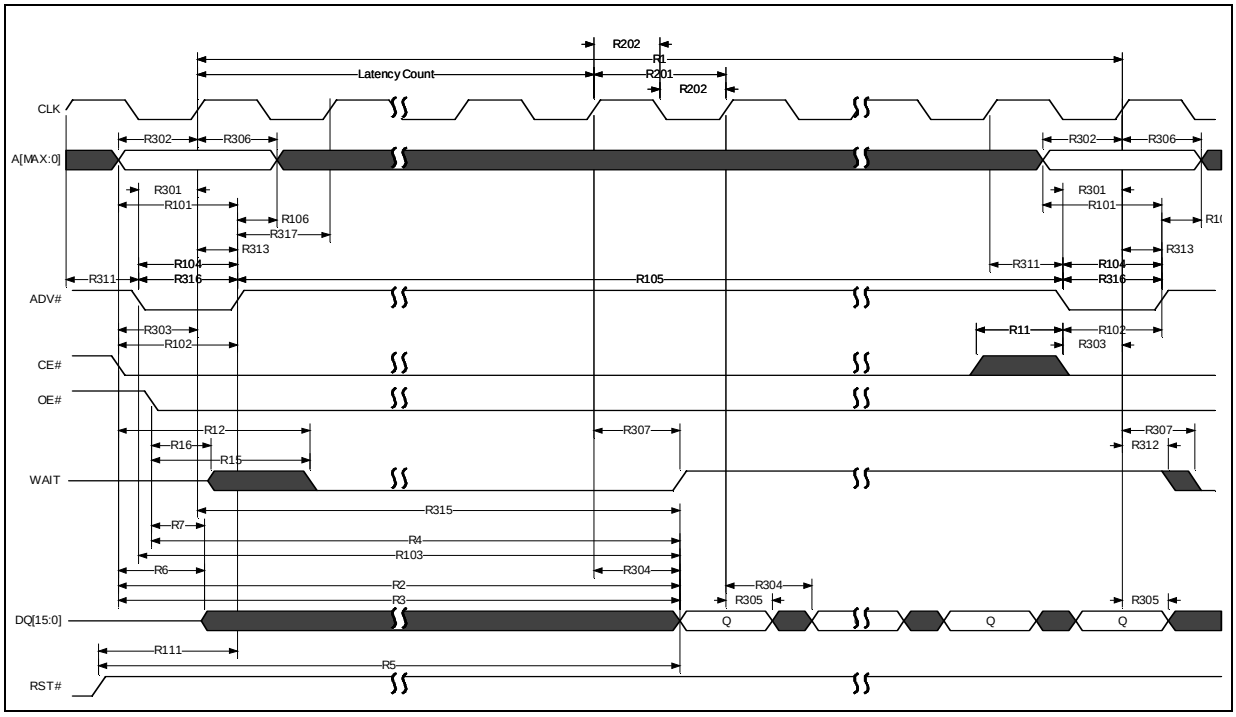
Figure 24: Synchronous Continuous Mis-aligned Burst (Non-Mux)



Notes:
1. R2, R3 and R103 apply to legacy-latching only; R315 and R316 apply to clock-only latching only.
2. For legacy-latching (ADV# OR CLK latching), ADV# can be held low throughout the synchronous read operation.

.

Figure 25: Sync Burst with Burst-Interrupt (Non-Mux)

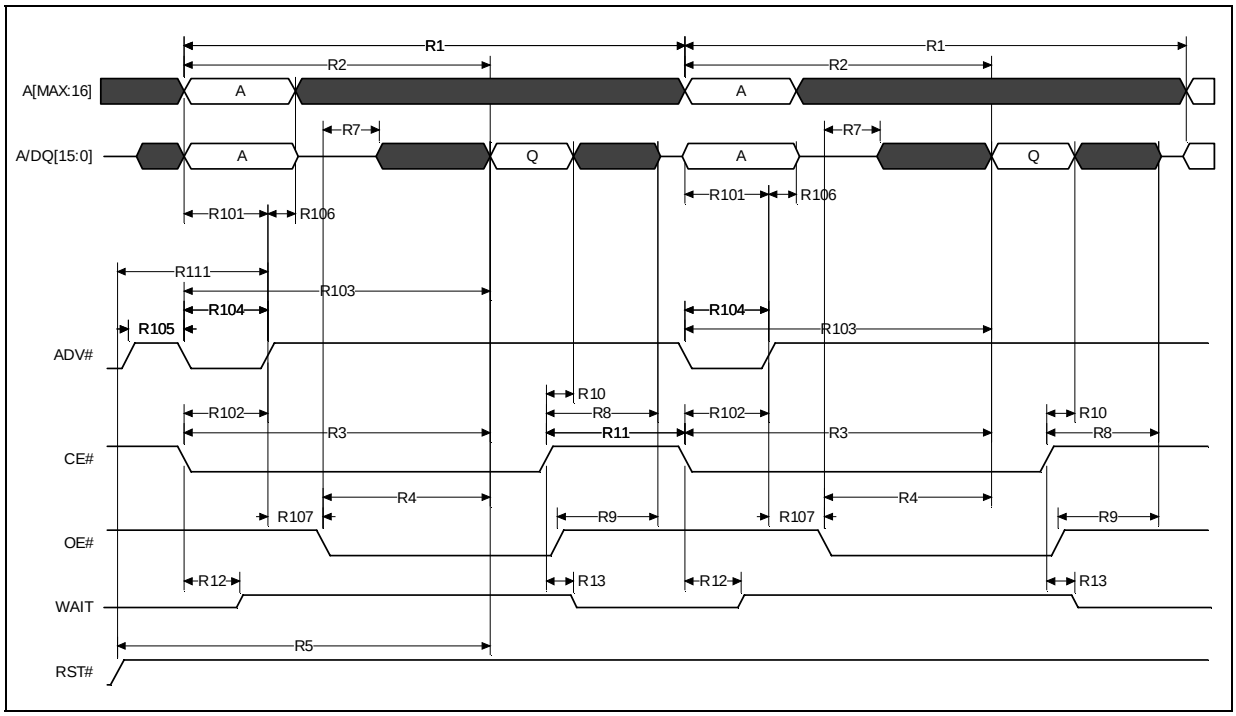


Notes:

1. R2, R3 and R103 apply to legacy-latching only; R315 and R316 apply to clock-only latching only
2. For legacy-latching (ADV# OR CLK latching), ADV# can be held low throughout the synchronous read operation.
3. A burst can be interrupted by toggling CE# or ADV#. If ADV# interrupts burst, then R105 applies.

7.2.4 Timings: AD-Mux Device, Async Read

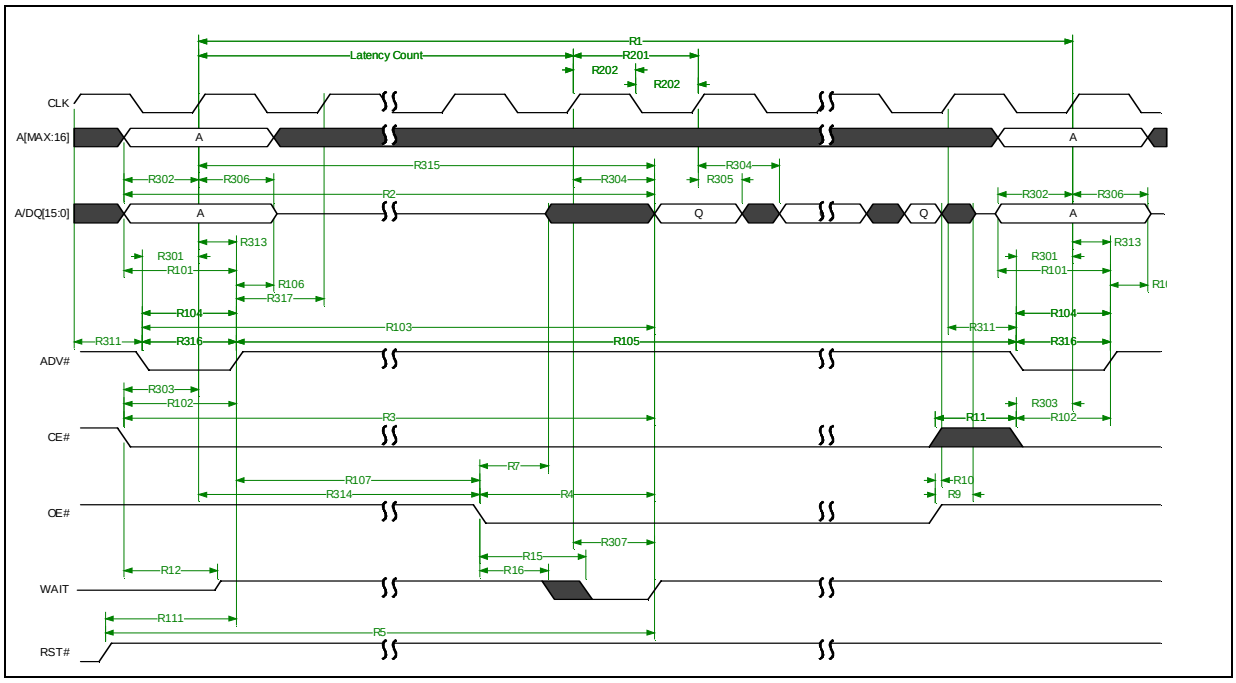
Figure 26: Async Single-Word Read (AD-Mux)



Note: Diagram shows back-to-back read operations.

7.2.5 Timings: AD-Mux Device, Sync Read

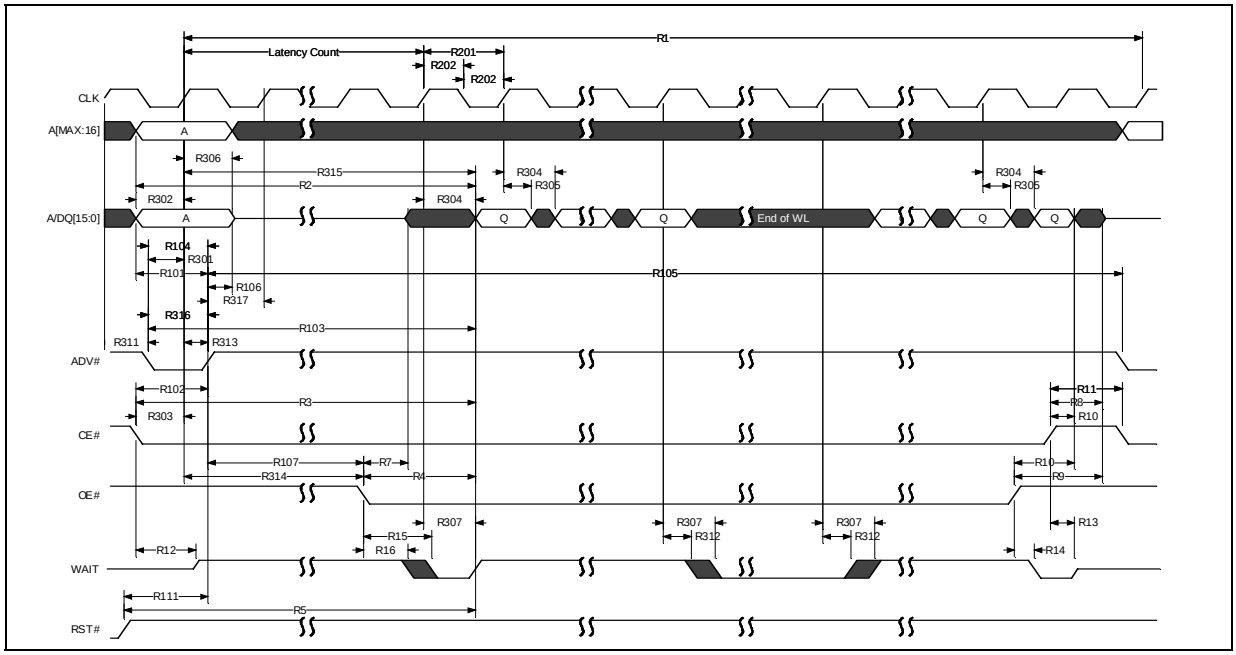
Figure 27: Synchronous 8- or 16-word burst read (AD-Mux)



Notes:

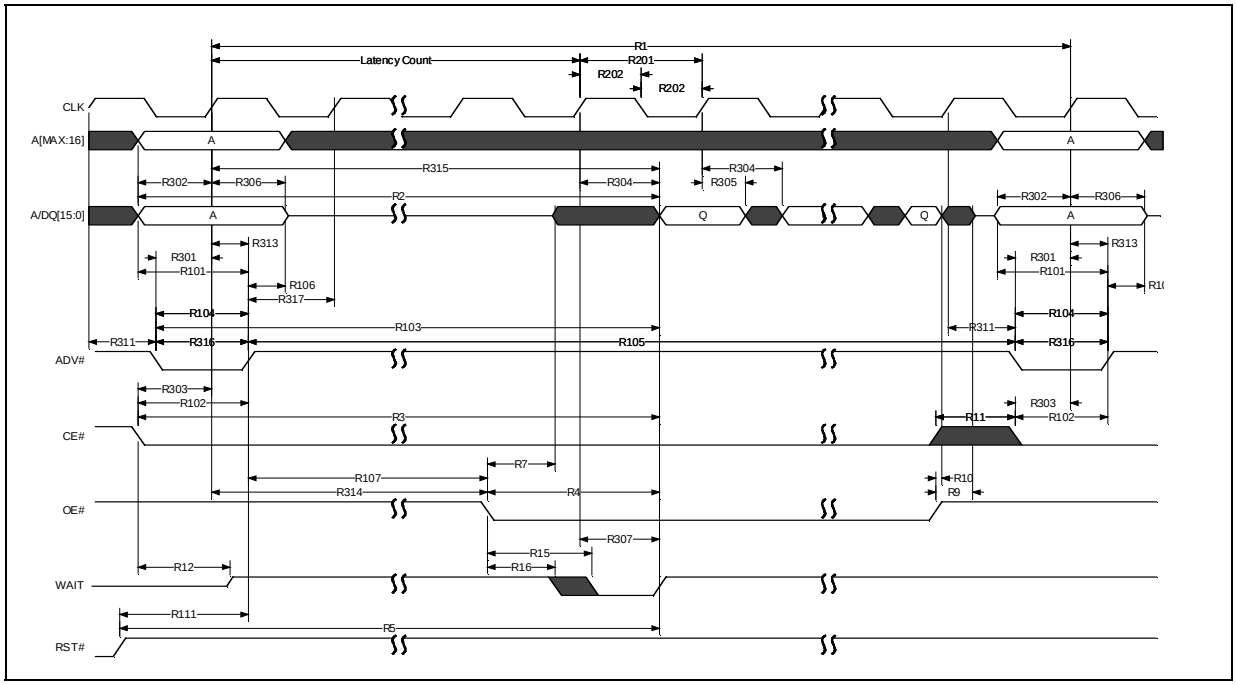
1. 8-word and 16-word burst are always wrap-only.
2. R2, R3 and R103 apply to legacy-latching only; R315 and R316 apply to clock-only latching only.

Figure 28: Synchronous Continuous Mis-Aligned Burst (AD-Mux)



Note: R2, R3 and R103 apply to legacy-latching only; R315 and R316 apply to clock-only latching only.

Figure 29: Synchronous Burst with Burst-Interrupt (AD-Mux)



Notes:
1. R2, R3 and R103 apply to legacy-latching only (ADV# OR CLK latching); R315 and R316 apply to clock-only latching only
2. A burst can be interrupted by toggling CE# or ADV#.

7.3 Write Specifications

The M18 device includes specifications for different lithographies, densities, and frequencies. For additional information on combinations, see Table 4, "M18 Product Litho/Density/Frequency Combinations" on page 10 in the Section 2.0, "Functional Description".

Table 22: AC Write Specifications

Number	Symbol	Parameter (1, 2)	Min	Max	Units	Notes
W1	t_{PHWL}	RST# high recovery to WE# low	150	—	ns	1,2,3
W2	t_{ELWL}	CE# setup to WE# low	0	—	ns	1,2
W3	t_{WLWH}	WE# write pulse width low	40	—	ns	1,2,4
W4	t_{DVWH}	Data setup to WE# high	40	—	ns	1,2
W5	t_{AVWH}	Address setup to WE# high	40	—	ns	
W6	t_{WHEH}	CE# hold from WE# high	0	—	ns	
W7	t_{WHDX}	Data hold from WE# high	0	—	ns	
W8	t_{WHAX}	Address hold from WE# high (non-mux only)	0	—	ns	
W9	t_{WHWL}	WE# pulse width high	20	—	ns	1,2,5
W10	t_{VPWH}	VPP setup to WE# high	200	—	ns	1,2,3,7
W11	t_{QVVL}	VPP hold from Status read	0	—	ns	
W12	t_{QVBL}	WP# hold from Status read	0	—	ns	
W13	t_{BHWH}	WP# setup to WE# high	200	—	ns	
W14	t_{WHGL}	WE# high to OE# low	0	—	ns	1,2,8
W15	t_{VLWH}	ADV# low to WE# high (AD-Mux only)	55	—	ns	1,2
W16	t_{WHQV}	WE# high to read valid	t_{AVQV}+30	—	ns	1,2,3,9
Write to Synchronous Read Specifications						
W19	t_{WHCH}	WE# high to Clock high	15	—	ns	1,2,3,6,9
W27	t_{WHEL}	WE# high to CE# low	9	—	ns	1,2,3,6,9
W28	t_{WHVL}	WE# high to ADV# low	7	—	ns	1,2,3,6,9
Bus Write with Active Clock Specifications						
W21	t_{VHWL}	ADV# high to WE# low	—	27	ns	1,2,10,11
W22	t_{CHWL}	Clock high to WE# low	—	27	ns	

Notes:

1. Write timing characteristics during erase suspend are the same as write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Hence, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever occurs first) to CE# or WE# low (whichever occurs last). Hence, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$).
6. t_{WHCH} must be met when transitioning from a write cycle to a synchronous burst read. In addition there must be a CE# toggle after WE# goes high.
7. VPP and WP# should be at a valid level until erase or program success is determined.
8. When doing a Read Status operation following any command that alters the Status Register data, W14 is 20ns.
9. Add 10ns if the write operations results in a RCR or block lock status change, for the subsequent read operation to reflect this change.
10. This specification is applicable only if the part is configured in synchronous mode and an active clock is running. Either t_{VHWL} or t_{CHWL} must be met depending on the whether the address is latched on ADV# or CLK.
11. These specifications are not applicable to 133 MHz devices.

7.3.1 Write Timing Waveforms

The following sections show the timing waveforms for write specifications and write-to-read and read-to-write transitions for Non-Mux and AD-Mux M18 devices.

The Synchronous read timings apply to both the 108 and 133 MHz devices. However please note that M18 devices which only support up to 108 MHz need not meet the R313 to R317 timing specifications.

Please note that the WAIT signal polarity in all the timing waveforms is low-true (RCR10 = 0). WAIT is de-asserted during asynchronous reads.

Table 23: List of Write Timing waveforms

M18 Device	Description
Non-Mux	Write to Write
	Async Read to Write
	Write to Async Read
	Sync Read to Write
	Write to Sync Read
ADMux	Write to Write
	Async Read to Write
	Write to Async Read
	Sync Read to Write
	Write to Sync Read

7.3.2 Timings: Non Mux Device

Figure 30: Write to Write (Non-Mux)

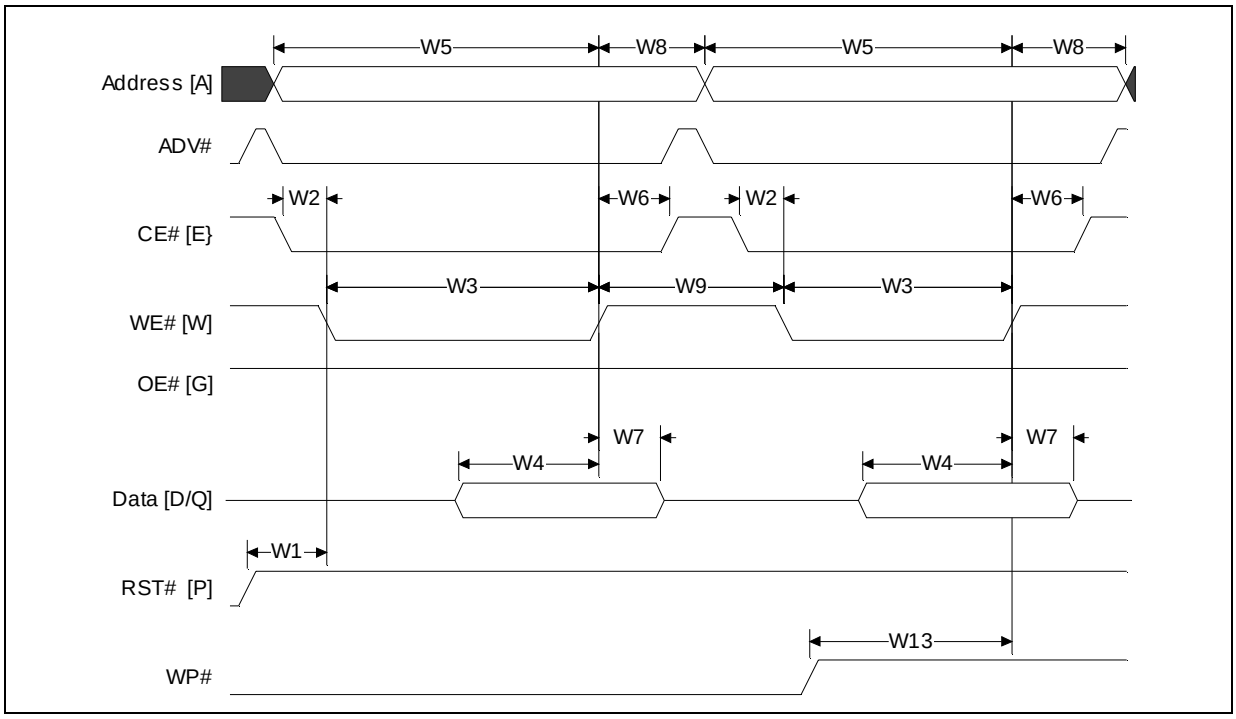


Figure 31: Async Read to Write (Non-Mux)

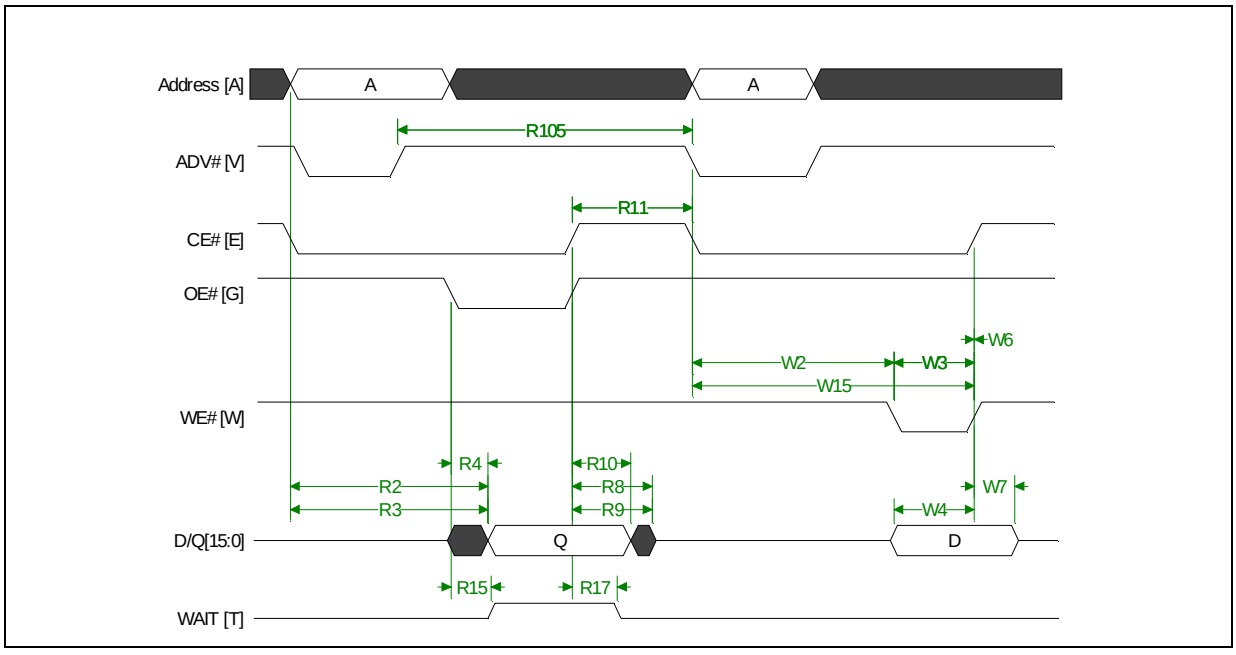


Figure 32: Write to Async Read (Non-Mux)

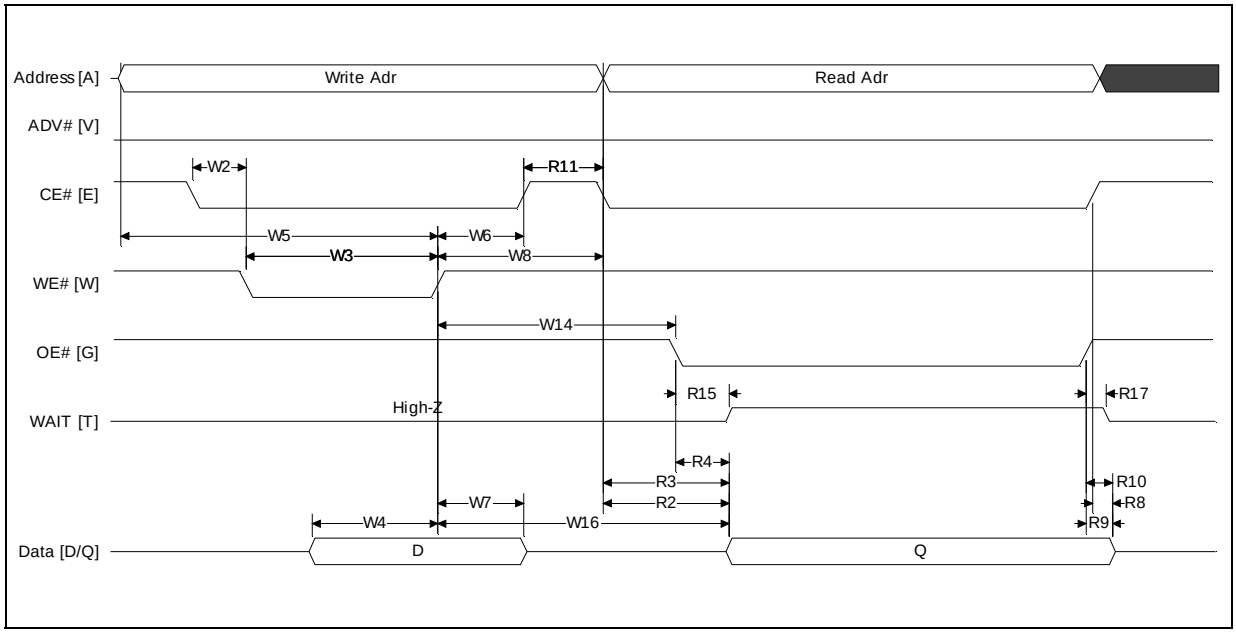


Figure 33: Sync Read to Write (Non-Mux)

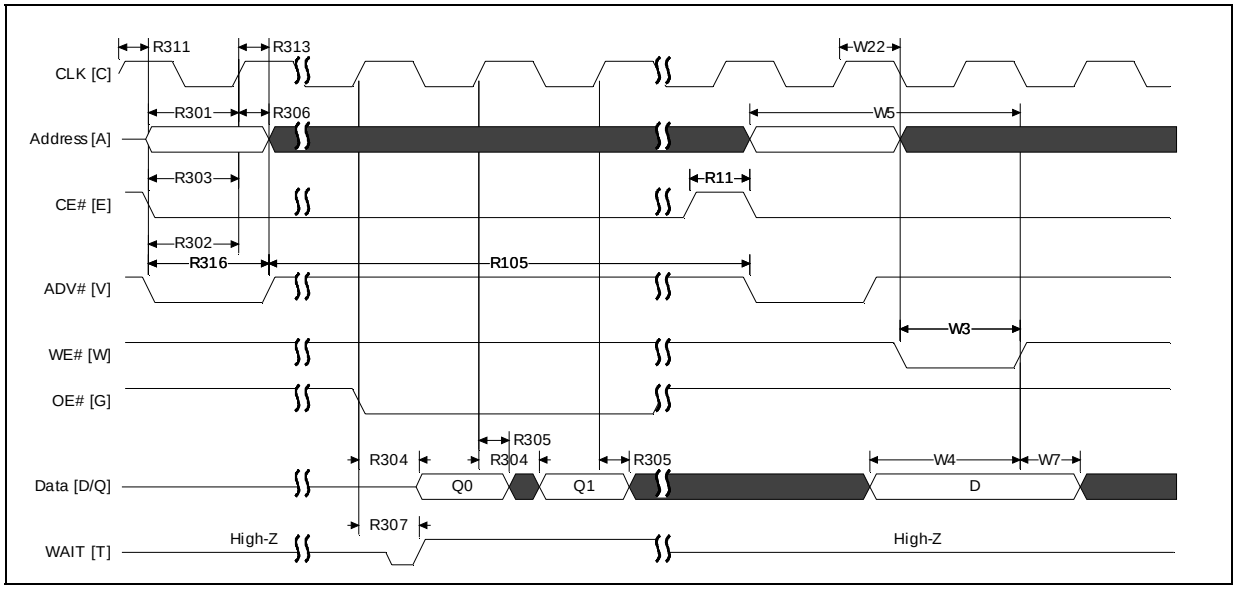
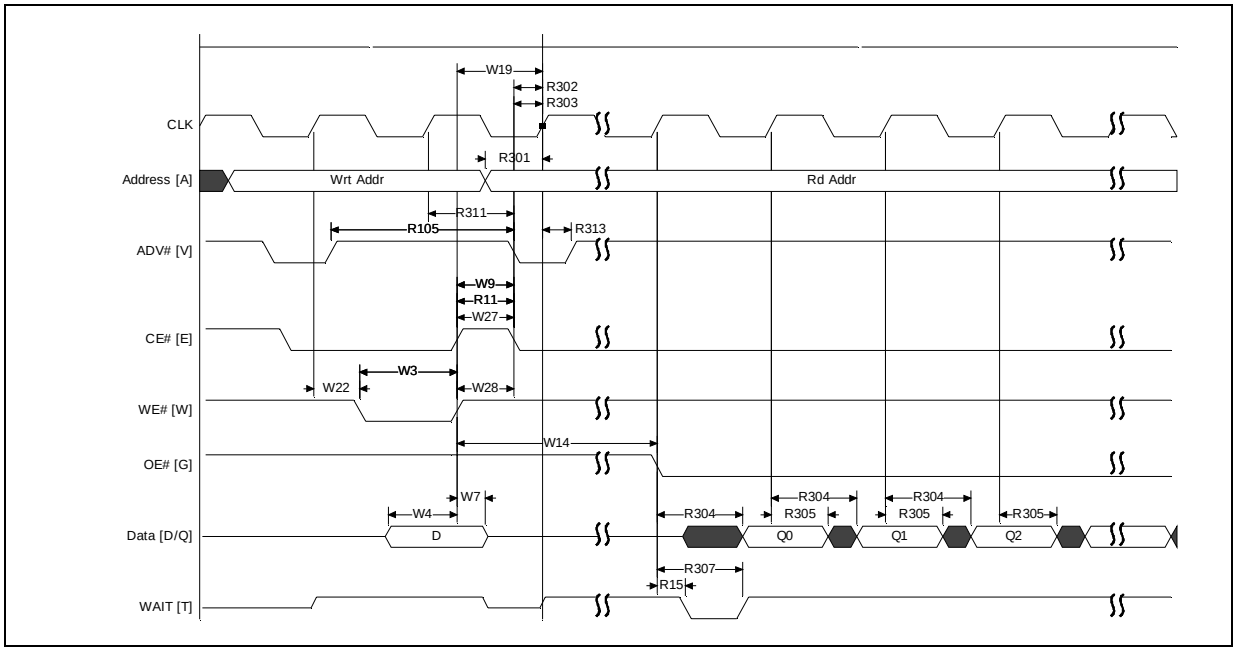


Figure 34: Write to Sync Read (Non-Mux)



7.3.3 Timings: AD-Mux Device

Figure 35: Write to Write (AD-Mux)

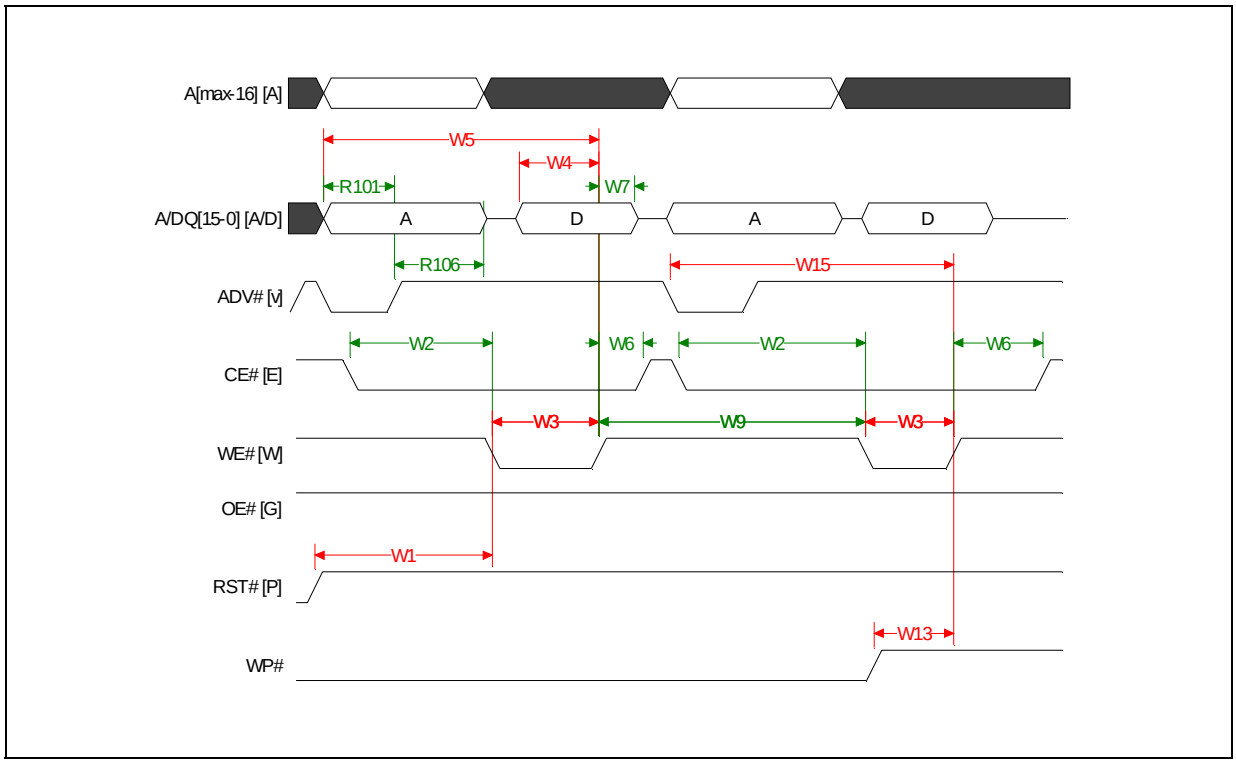


Figure 36: Async Read to Write (AD-Mux)

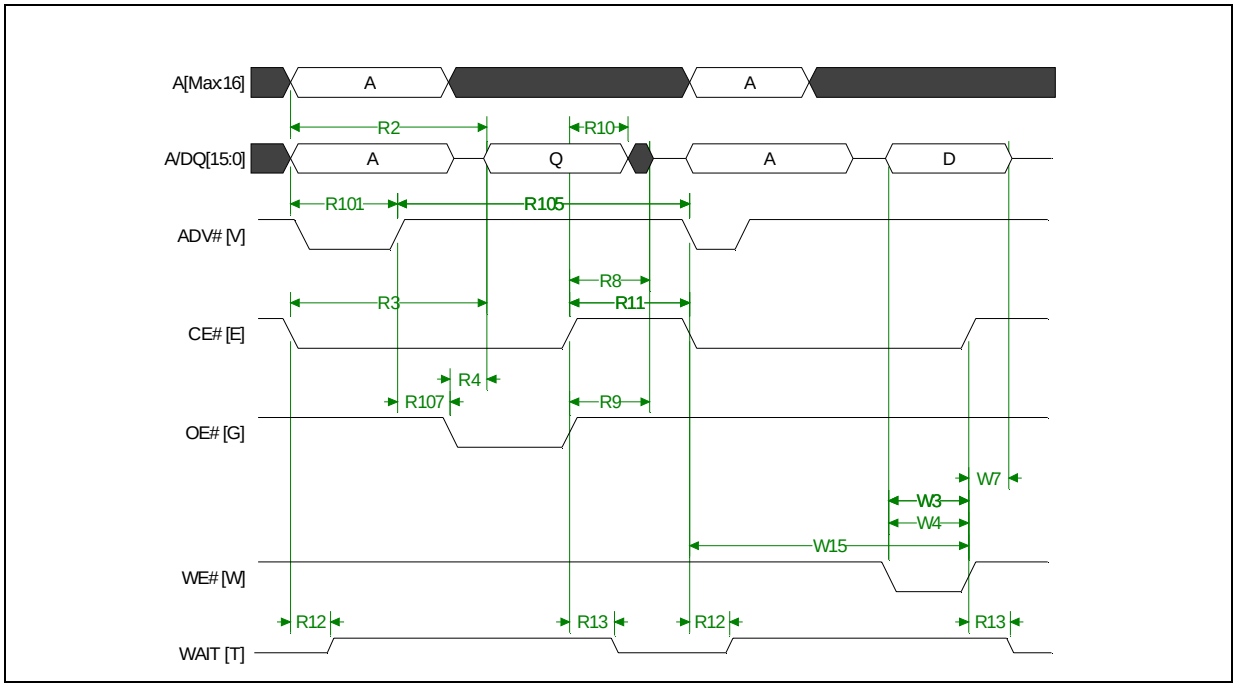


Figure 37: Write to Async Read (AD-Mux)

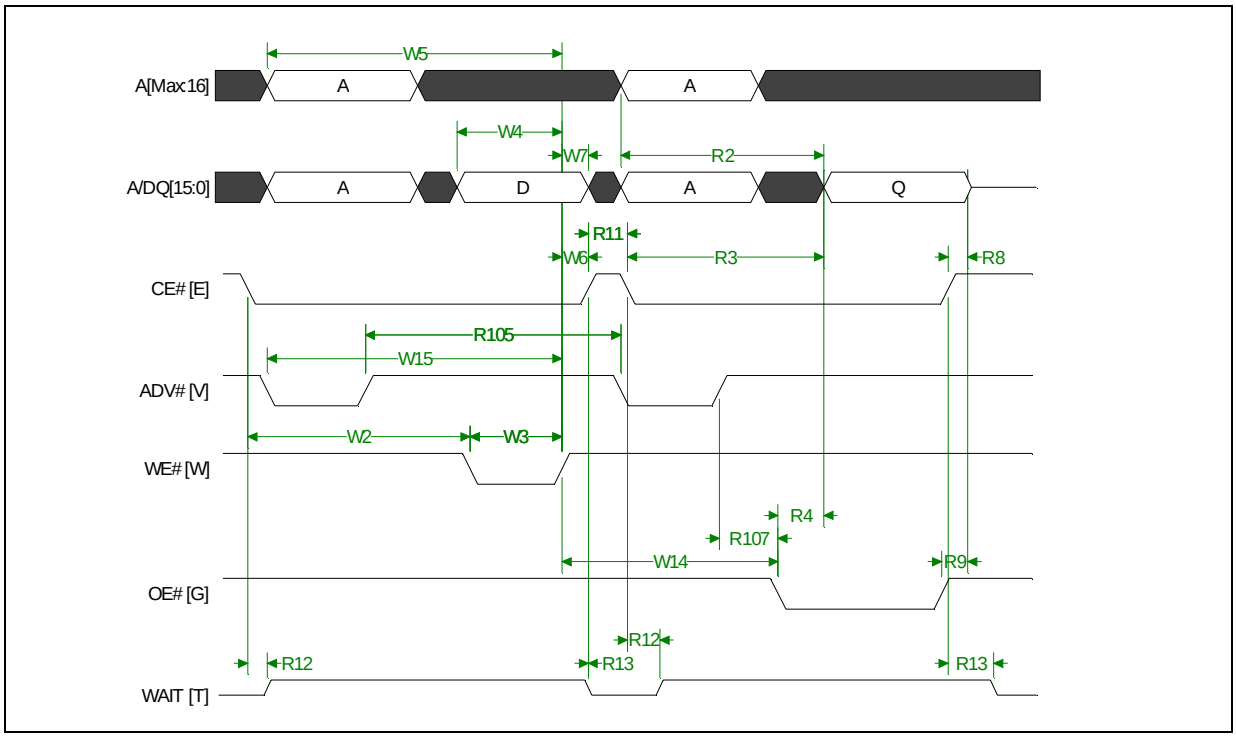
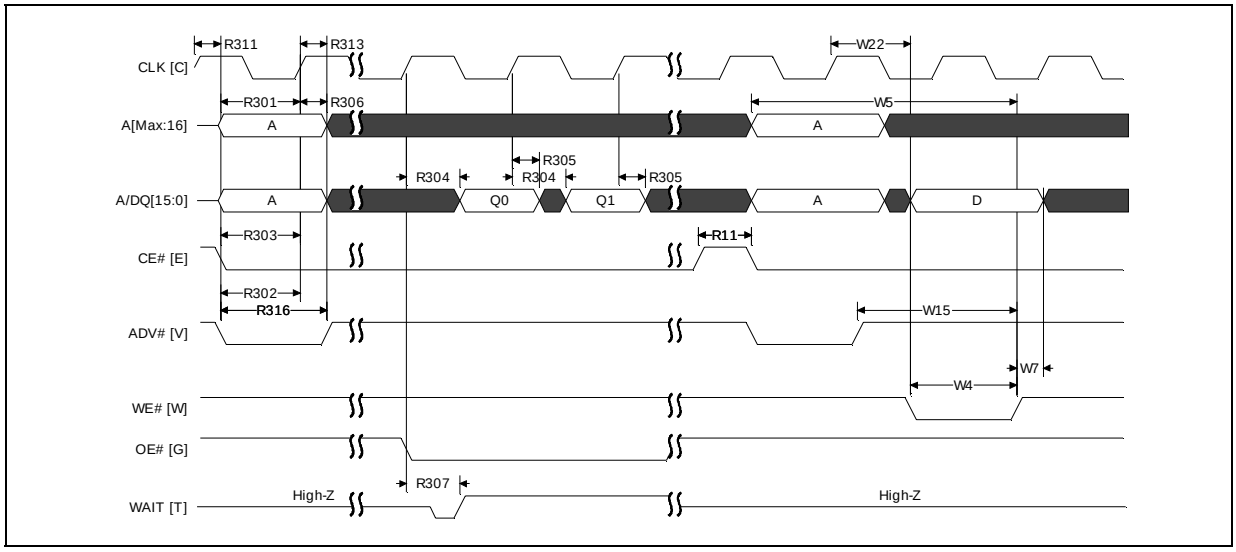
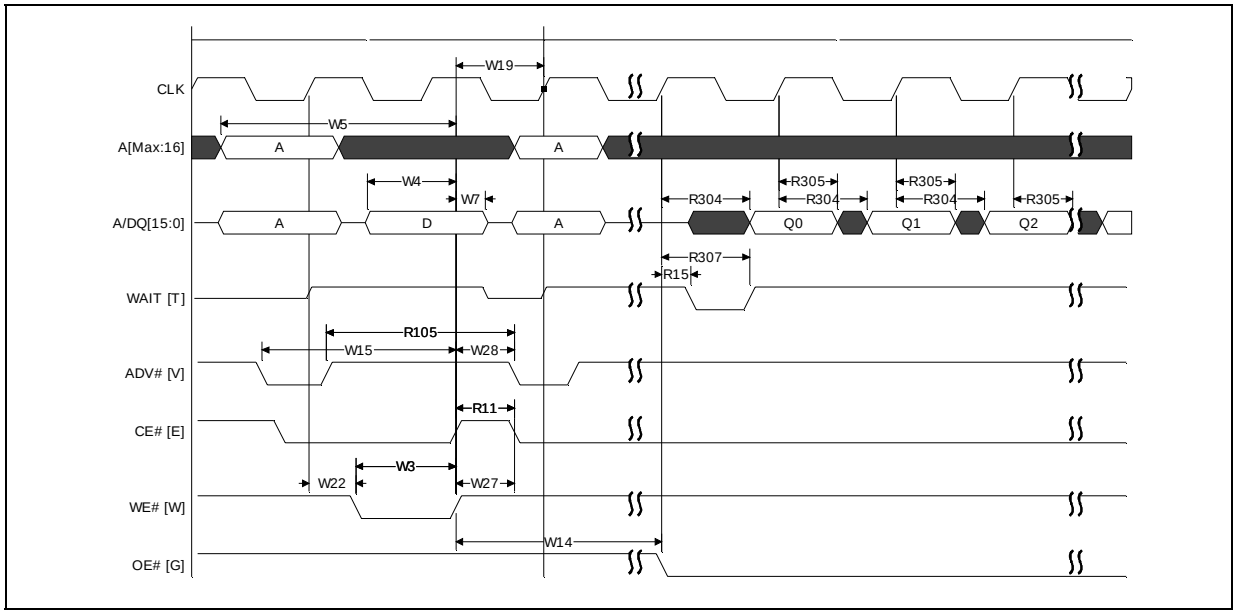


Figure 38: Sync Read to Write (AD-Mux)



Notes:
1. CLK may be stopped during write cycle.
2. W22 is the time between the Address-latching-CLK and WE#. In case of ADV#-latching, W21 must be met instead.

Figure 39: Write to Sync Read (AD-Mux)



Note: CLK may be stopped during write cycle.

7.4 Program and Erase Characteristics

The M18 device includes specifications for different lithographies, densities, and frequencies. For additional information on combinations, see Table 4, “M18 Product Litho/Density/Frequency Combinations” on page 10 in the Section 2.0, “Functional Description.

Table 24: Program-Erase Characteristics

Nbr.	Symbol	Parameter		V_{PPL}/V_{PPH}					Unit	Notes
				Litho (nm)	Density (Mbit)	Min	Typ	Max		
Conventional Word Programming										
W200	$t_{PROG/W}$	Program Time	Single word (first word)	—	—	—	115	230	µs	1,2
			Single word (subsequent word)	—	—	—	50	230		
Buffered Programming										
W200	$t_{PROG/W}$	Program Time	Single word	—	—	—	250	500	µs	1
W250	$t_{PROG/PB}$		One Buffer (512 words)	90 65	256, 512 128, 256, 512, 1024	—	2.15 1.02	4.3 2.05	ms	
Buffered Enhanced Factory Programming										
W451	$t_{BEFP/W}$	Program Time	Single word	90 65	256, 512 128, 256, 512	—	4.2 2.0	—	µs	1,3,4
W452	$t_{BEFP/Setup}$		Buffered EFP Setup	—	—	5	—	—		1
Erasing and Suspending										
W501	$t_{ERS/MAB}$	Erase Time	128-Kword Main Array Block	—	—	—	0.9	4	s	1
W600	$t_{SUSP/P}$	Suspend Latency	Program suspend	—	—	—	20	30	µs	1
W601	$t_{SUSP/E}$		Erase suspend	—	—	—	20	30		1
Blank Check										
W702	$t_{BC/MB}$	Blank Check	Main array block	—	—	—	3.2	—	ms	1

Notes:
1. Typical values measured at T_C = +25 °C and nominal voltages. Performance numbers are valid for all speed versions. Sampled, but not 100% tested.
2. First and subsequent words refer to first word and subsequent words in Control Mode programming region.
3. Averaged over entire device.
4. BEFP not validated at V_{PPL}.

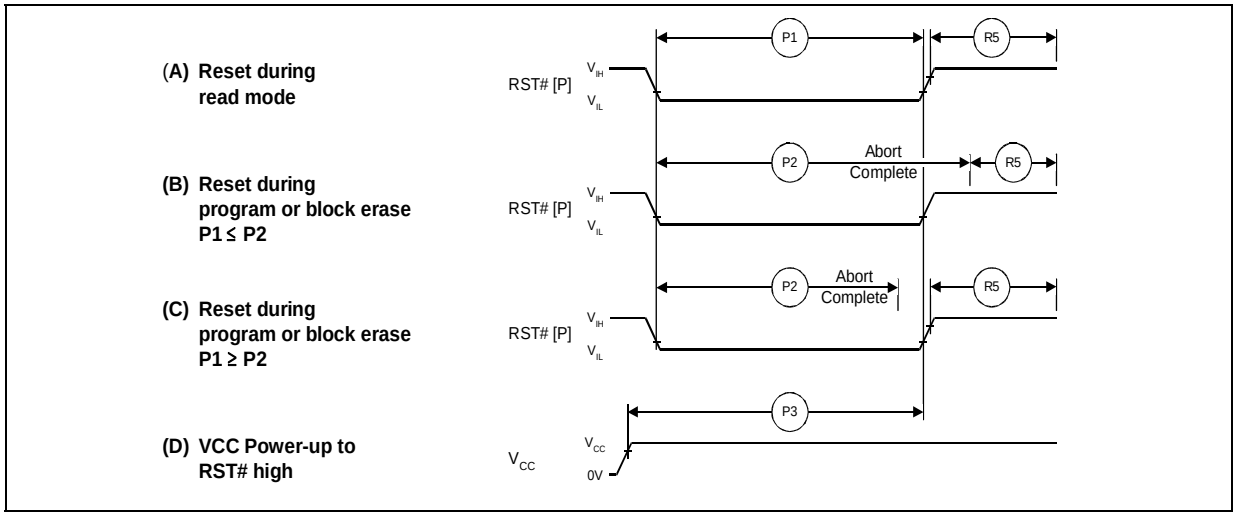
7.5 Reset Specifications

Table 25: Reset Specifications

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
P1	t_{PLPH}	RST# pulse width low	100		ns	1,2,3,4,7
P2	t_{PLRH}	RST# low to device reset during erase	—	25	µs	1,3,4,7
		RST# low to device reset during program	—	25		1,3,4,7
P3	t_{VCCPH}	V_{CC} Power valid to RST# de-assertion (high)	300	—		1,4,5,6

Notes:
1. These specifications are valid for all device versions (packages and speeds).
2. The device may reset if t_{PLPH} is < $t_{PLPH\ MIN}$, but this is not guaranteed.
3. Not applicable if RST# is tied to Vccq.
4. Sampled, but not 100% tested.
5. If RST# is tied to the V_{CC} supply, device will not be ready until t_{VCCPH} after $V_{CC} \geq V_{CC}$ min.
6. If RST# is tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until $V_{CC} \geq V_{CC}$(min).
7. Reset completes within t_{PLPH} if RST# is asserted while no erase or program operation is executing.

Figure 40: Reset Operation Timing



7.6 Deep Power Down Specifications

Table 26: Deep Power Down Specifications (Sheet 1 of 2)

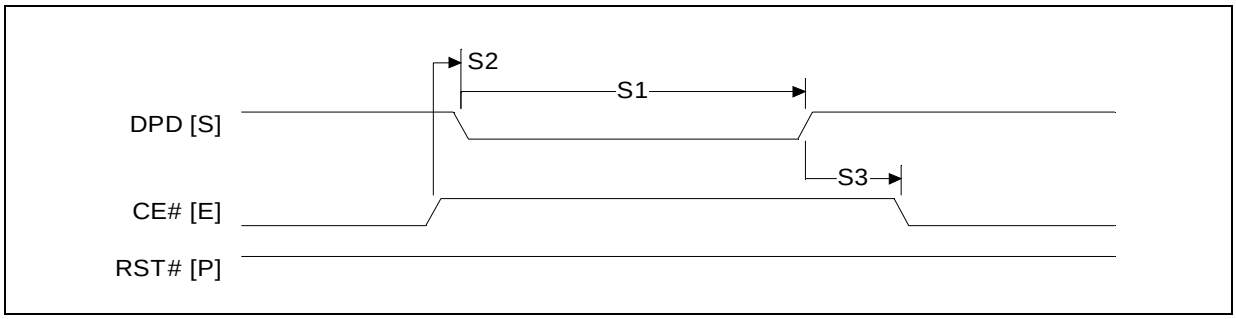
Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
S1	t_{SLSH} (t_{SHSL})	DPD asserted pulse width	100	—	ns	1,2,3

Table 26: Deep Power Down Specifications (Sheet 2 of 2)

Nbr.	Symbol	Parameter	Min	Max	Unit	Notes
S2	t_{EHSH} (t_{EHSL})	CE# high to DPD asserted	0	—	µs	1,2
S3	t_{SHEL} (t_{SLEL})	DPD deasserted to CE# low	75	—		1,2
S4	t_{PHEL}	RST# high during DPD state to CE# low (DPD deasserted to CE# low)	75	—		1,2

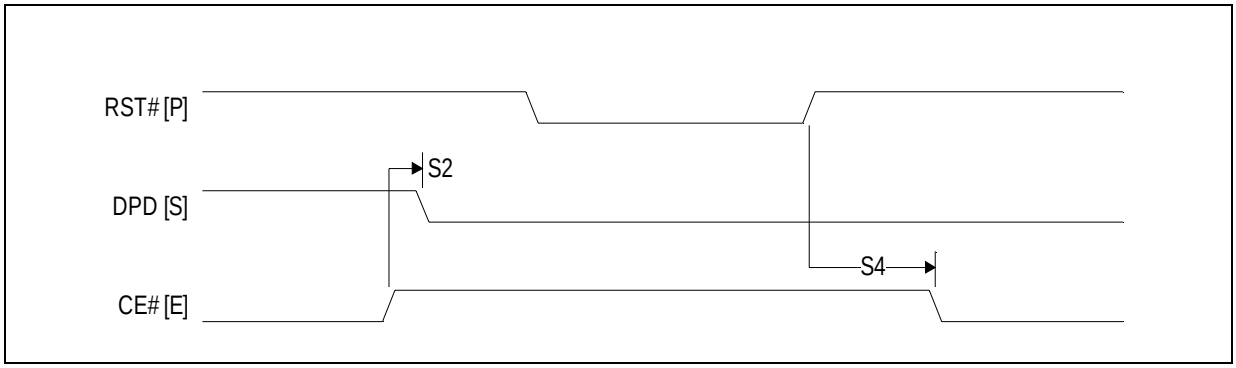
Notes:
1. These specifications are valid for all device versions (packages and speeds).
2. Sampled, but not 100% tested.
3. DPD must remain asserted for the duration of Deep Power Down mode. DPD current levels are achieved 40 µs after entering the DPD mode.

Figure 41: Deep Power Down Operation Timing



Note: DPD pin is low-true (ECR14 = 0)

Figure 42: Reset During Deep Power Down Operation Timing



Note: DPD pin is low-true (ECR14 = 0)

8.0 NOR Flash Bus Interface

The flash device uses low-true control signal inputs, and is selected by asserting the chip enable (CE#) input. The output enable (OE#) input is asserted for read operations, while the write enable (WE#) input is asserted for write operations. OE# and WE# should never be asserted at the same time; otherwise, indeterminate device operation will result. All bus cycles to or from the flash memory conform to standard microcontroller bus cycles.

Commands are written to the device to control all operations.

Table 27 shows the logic levels that must be applied to the control-signal inputs of the device for the various bus operations.

Table 27: Flash Memory Control Signals

Operation	RST#	DPD[2]	CE#[1]	OE#[1]	WE#[1]	Address[1]	Data I/O
Reset	Low	High	X	X	X	X	High-Z
Read	High	High	Low	Low	High	Valid	Output
Output Disable	High	High	Low	High	High	X	High-Z
Write	High	High	Low	High		Valid	Input
	High	High		High	Low	Valid	Input
Standby	High	High	High	X	X	X	High-Z
Deep Power-Down	High	Low	High	X	X	X	High-Z

Notes:
1. X = Don't care (High or Low)
2. DPD polarity determined by ECR14. Shown low-true here.

8.1 Bus Reads

To perform a read operation, both CE# and OE# must be asserted; #RST# and WE# must be deasserted. OE# is the data-output control and when asserted, the output data is driven on to the data I/O bus. All read operations are independent of the voltage level on VPP.

The Automatic Power Savings (APS) feature provides low power operation following reads during active mode. After data is read from the memory array and the address lines are quiescent, APS automatically places the device into standby. In APS, device current is reduced to I_{CCAPS}.

The device supports two read configurations:

- Asynchronous reads. RCR15 = 1. This is the default configuration after power-up/ reset.
  - — Non-multiplexed devices support asynchronous page-mode reads. AD-Multiplexed devices support only asychronous single-word reads.
- Synchronous Burst reads. RCR15 = 0.

8.1.1 Asynchronous single-word reads

In asynchronous single-word read mode, a single word of data corresponding to the address is driven onto the data bus after the initial access delay. The address is latched when ADV# is deasserted. For AD-multiplexed devices, ADV# must be deasserted before OE# is asserted.

If only asynchronous reads are to be performed, CLK must be tied to a valid V_{IH} or V_{IL} level, and the WAIT signal can be floated. In addition, for non-multiplexed devices, ADV# must be tied to ground.

8.1.2 Asynchronous Page Mode (Non-multiplexed devices only)

In asynchronous page mode, sixteen data words are “sensed” simultaneously from the flash memory array and loaded into an internal page buffer. The buffer word corresponding to the initial address is driven onto the data bus after the initial access delay. Subsequent words in the page are output after the page access delay. A[3:0] bits determine which page word is output during a read operation. A[MAX:4] and ADV# must be stable throughout the page access.

WAIT is deasserted during asynchronous page mode. ADV# can be driven high to latch the address, or held low throughout the read cycle. CLK is not used for asynchronous page-mode reads, and is ignored.

8.1.3 Synchronous Burst Mode

Synchronous burst mode is a clock-synchronous read operation that improves the read performance of flash memory over that of asynchronous reads.

Synchronous burst mode is enabled by programming the Read Configuration Register (RCR) of the flash memory device. The RCR is also used to configure the burst parameters of the flash device, including Latency Count, burst length of 8, 16 and continuous, and WAIT polarity.

Three additional signals are used for burst mode: CLK, ADV#, and WAIT.

The address for synchronous read operations is latched on the ADV# rising edge or the first rising CLK edge after ADV# low, whichever occurs first for devices that support up to 108 MHz. For devices that support up to 133 MHz, the address is latched on the last CLK edge when ADV# is low.

During synchronous read modes, the first word is output from the data buffer on the rising CLK edge after the initial access latency delay. Subsequent data is output on rising CLK edges following a t_{CHQV} delay. However, for a synchronous non-array read, the same word of data will be output on successive rising clock edges until the burst length requirements are satisfied.

8.1.3.1 WAIT Operation

Upon power up or exit from reset, WAIT polarity defaults to low-true operation (RCR10 = 0). During *synchronous* reads (RCR15 = 0), WAIT asserts when read data is *invalid*, and deasserts when read data is *valid*. During *asynchronous* reads (RCR15 = 1), WAIT is deasserted. During writes, WAIT is High-Z on non-mux devices, and deasserted on AD-mux devices. Table 28 summarizes WAIT behavior.

Table 28: WAIT Behavior Summary

Device Operation		CE#	OE#	WE#	WAIT	Notes
Device not selected	Standby	High	X	X	High-Z	1
Non-Mux Device	Output Disable	Low	High	High	High-Z	
	Sync Read		Low	High	Active	2
	Async Read		Low	High	Deasserted	
	Write		High	Low	High-Z	
AD-Mux Device	Output Disable		High	High	Deasserted	
	Sync Read		Low	High	Active	2
	Async Read		Low	High	Deasserted	
	Write		High	Low	Deasserted	

Notes:
1. X = don't care (high or low).
2. Active: WAIT asserted = invalid data; WAIT deasserted = valid data.

8.2 Bus Writes

To perform a write operation, both CE# and WE# are asserted while RST# and OE# are deasserted. All device write operations are asynchronous, with CLK being ignored, but CLK can be kept active/toggling. During a write operation in non-muxed devices, address and data are latched on the rising edge of WE# or CE#, whichever occurs first. During a write operation in muxed devices, address is latched during the rising edge of ADV# OR CE# whichever occurs first and Data is latched during the rising edge of WE# OR CE# whichever occurs first.

8.3 Reset

The device enters a reset mode when RST# is asserted. In reset mode, internal circuitry is turned off and outputs are placed in a high-impedance state. The device shuts down any operation in progress, a process which takes a minimum amount of time to complete.

To return from reset mode, RST# must be deasserted. Normal operation is restored after a wake-up interval.

8.4 Deep Power-Down

The device enters DPD mode when the following two conditions are met: ECR15 is set(1) and DPD is asserted. The two conditions can be satisfied in any order. ECR14 bit determines the DPD asserted logic level. While in this mode, RST# and CE# must be deasserted.

The device exits DPD mode when DPD is deasserted. There is an exit latency before the device returns to standby mode and any operations are allowed. See the datasheet for the timing specifications.

The device should not be placed in DPD mode when a program/erase operation is ongoing or suspended. If the device enters DPD mode in the middle of a program, erase or suspend, the operation is terminated and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid.

While in DPD mode, the read-mode of each partition, configuration registers (RCR and ECR), and block lock bits, are preserved. Status register is reset to 0080h; i.e., if the Status register contains error bits, they will be cleared.

8.5 Standby

When CE# is deasserted, the device is deselected and placed in standby, substantially reducing power consumption. In standby, data outputs are placed in high-Z, independent of the level placed on OE#. If deselected during a Program or Erase operation, the device continues to consume active power until the operation is complete. There is no additional latency for subsequent read operations.

8.6 Output Disable

When OE# is deasserted with CE# asserted, the device outputs are disabled. Output pins are placed in a high-impedance state. WAIT is deasserted in AD-muxed devices and driven to High-Z in non-multiplexed devices.

8.7 Bus Cycle Interleaving

When issuing commands to the device, a read operation can occur between the two write cycles of a 2-cycle command. (See Figure 43 and Figure 44) However, a write operation cannot occur between the two write cycles of a 2-cycle command and will cause a command sequence error (See Figure 45).

Figure 43: Operating Mode with Correct Command Sequence Example

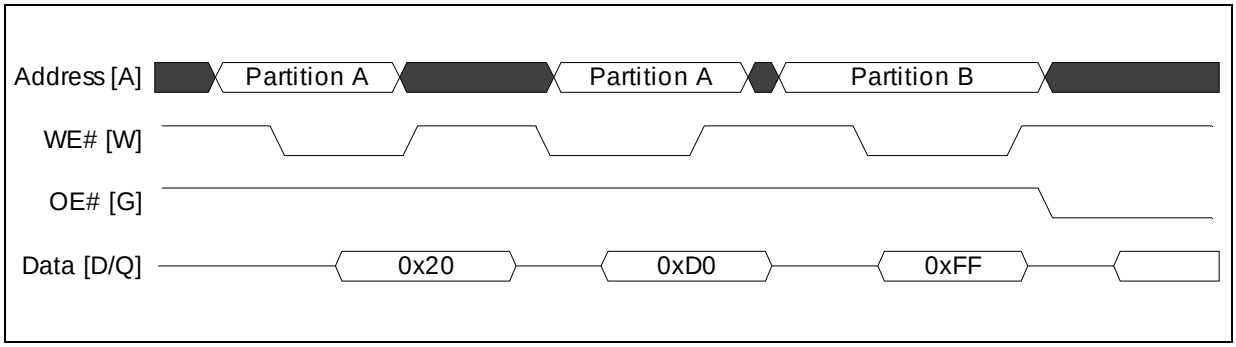


Figure 44: Operating Mode with Correct Command Sequence Example

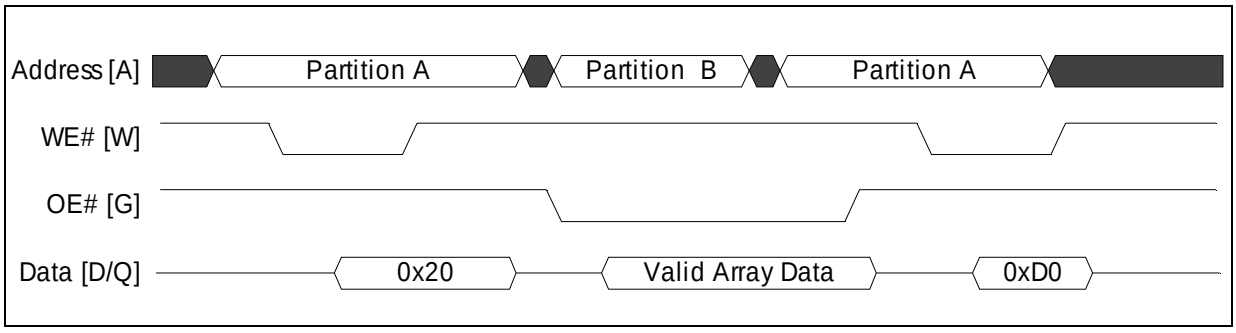
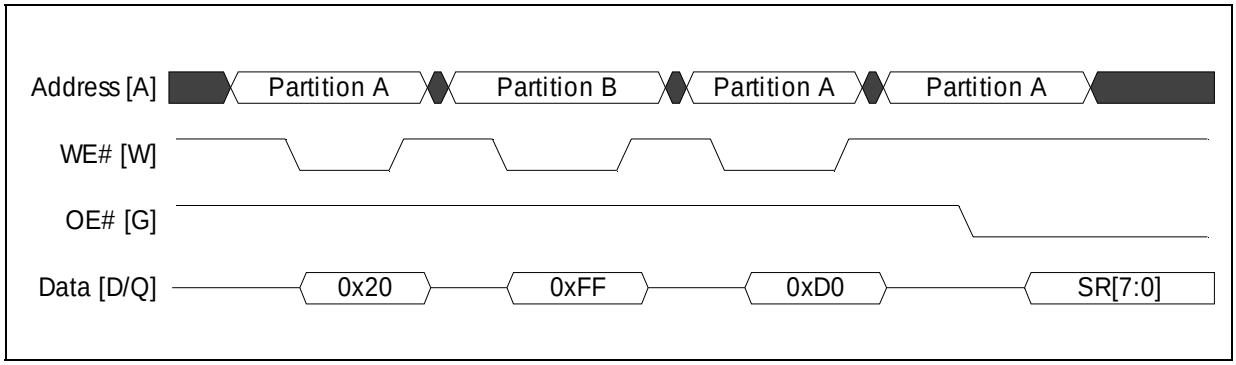


Figure 45: Operating Mode with Illegal Command Sequence Example



8.7.1 Read Operation During Program Buffer fill

Due to the large buffer size of devices, the system interrupt latency may be impacted during the buffer fill phase of a buffered programming operation. Please refer to the relevant Application Note listed in Section 1.4, “Additional Information” on page 7 to implement a software solution for your system.

8.8 Read-to-Write and Write-to-Read Bus Transitions

Consecutive read and write bus cycles must be properly separated from each other to avoid bus contention. These cycle separation specs are described in the sections below.

8.8.1 Write to Asynchronous read transition

To transition from a bus write to an asynchronous read operation, either CE# or ADV# must be toggled after WE# goes high.

8.8.2 Write to synchronous read transition

To transition from a bus write to a synchronous read operation, either CE# or ADV# must be toggled after WE# goes high. In addition, W19 (t_{WHCH} -WE# high to CLK high) must be met.

8.8.3 Asynchronous/Synchronous read to write transition

To transition from a asynchronous/synchronous read to a write operation, either CE# or ADV# must be toggled after OE# goes high.

8.8.4 Bus write with active clock

To perform a bus write when the device is in synchronous mode and the clock is active, W21 (t_{VHWL}- ADV# High to WE# Low) or W22 (t_{CHWL} -Clock high to WE# low) must be met.

9.0 NOR Flash Operations

This section describes the operational features of NOR flash memory. Operations are command-based—command codes are first issued to the device, and then the device performs the desired operation. All command codes are issued to the device using bus-write cycles as explained in Section 3.0, "NOR Flash Bus Interface" on page 10. A complete list of available command codes can be found in Section 5.0, "Device Command Codes" on page 40.

9.1 Status Register

The Status Register (SR) is a 16-bit, read-only register that indicates device and partition status, and operational errors. To read the Status Register, issue the Read Status Register command. Subsequent reads output Status Register information on AD/DQ[15:10].

SR *status bits* are set and cleared by the device. SR *error bits* are set by the device, and must be cleared using the Clear Status Register command. Upon power-up or exit from reset, the Status Register defaults to 0080h.

Table 29: Status Register Bit Definitions (Sheet 1 of 2)

Status Register (SR) Bits									Default Value = 0080h
Reserved	Region Program Status	Ready Status	Erase Suspend Status	Erase Error	Program Error	Program /Erase Voltage Error	Program Suspend Status	Block-Locked Error	Partition Status
15-10	9-8	7	6	5	4	3	2	1	0

Bit	Name		Description
15-10	Reserved		Reserved for future use; these bits will always be set to zero.
9-8	Region Program Status		SR9 SR8 0 0 = Region program successful. 1 0 = Region program error - Attempted write with object data to Control Mode region. 0 1 = Region program error - Attempted rewrite to Object Mode region. 1 1 = Region program error - Attempted write using illegal command. SR4 will also be set along with SR[8,9] for the above error conditions.
7	Ready Status		0 = Device is busy; SR[9:8], SR[6:1] are invalid; 1 = Device is ready; SR[9:8], SR[6:1] are valid.
6	Erase Suspend Status		0 = Erase suspend not in effect. 1 = Erase suspend in effect.
5	Erase Error / Blank Check Error	Command Sequence Error	SR5 SR4 0 0 = Program or erase operation successful. 0 1 = Program error - operation aborted. 1 0 = Erase error: operation aborted / Blank check error: operation failed. 1 1 = Command sequence error - command aborted.
4	Program Error		
3	V_{PP} Error		0 = V_{PP} within acceptable limits during program or erase operation. 1 = V_{PP} not within acceptable limits during program or erase operation.

Table 29: Status Register Bit Definitions (Sheet 2 of 2)

Status Register (SR) Bits									Default Value = 0080h
Reserved	**Region Program Status**	**Ready Status**	**Erase Suspend Status**	**Erase Error**	**Program Error**	**Program /Erase Voltage Error**	**Program Suspend Status**	**Block-Locked Error**	**Partition Status**
15-10	**9-8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Bit	Name	Description
2	**Program Suspend Status**	0 = Program suspend not in effect. 1 = Program suspend in effect.
1	**Block-Locked Error**	0 = Block NOT locked during program or erase - operation successful. 1 = Block locked during program or erase - operation aborted.
0	**Partition Status**	SR7 SR0 0 0 = Active program or erase operation in addressed partition. BEFP: Program or Verify complete, or Ready for data. 0 1 = Active program or erase operation in other partition. BEFP: Program or Verify in progress. 1 0 = No active program or erase operation in any partition. BEFP: Operation complete 1 1 = Reserved.

9.1.1 Clearing the Status Register

The Status Register (SR) contain status and error bits which are set by the device. SR *status bits* are cleared by the device; however, SR *error bits* are cleared by issuing the Clear Status Register command. Resetting the device also clears the Status Register.

Table 30: Clear Status Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	**Data Bus**	**Address Bus**	**Data Bus**
Clear Status Register	Device Address	0050h	---	---

Depending on the current state of the partition, issuing the Clear Status Command will place the addressed partition in Read Status mode. Please see 'Next State' Table for further details. Other partitions are not affected.

Note: Care should be taken to avoid Status Register ambiguity. If a command sequence error occurs while in an Erase Suspend condition, the Status Register will indicate a Command Sequence error by setting SR4 and SR5. When the erase operation is resumed (and finishes), any errors that may have occurred during the erase operation will be masked by the Command Sequence error. To avoid this situation, clear the Status Register prior to resuming a suspended erase operation.

The Clear Status Register command functions independent of the voltage level on VPP.

9.2 Read Configuration Register

The Read Configuration Register (RCR) is a 16-bit read/write register used to select bus-read modes, and to configure synchronous-burst read characteristics of the flash device. All Read Configuration Register bits are set and cleared using the Program Read Configuration Register command.

Upon power-up or exit from reset, the Read Configuration Register defaults to asynchronous mode (RCR15 = 1; RCR[14:11] and RCR[9:0] are ignored).

To read the RCR value, issue the Read Device Information command to the desired partition. Subsequent reads from the <partition base address> + 05h will output RCR[15:0] on the data bus.

When using a Latency Count of Code 2 and a Data Hold of two cycles (CR9 = 1), WAIT must be configured to deassert with valid data (CR8 = 0).

Table 31: Read Configuration Register Bit Definitions

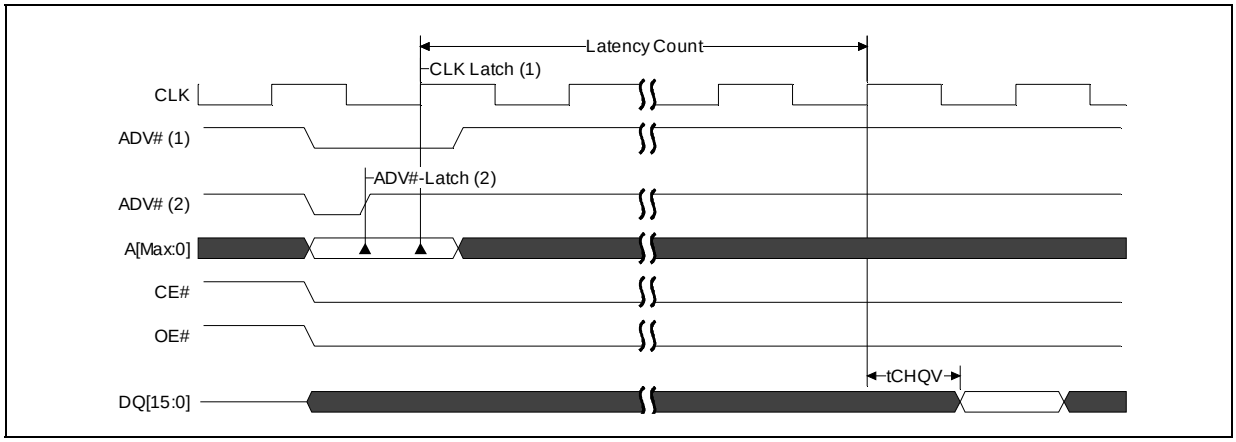
Read Configuration Register (RCR)											Default: CR15 = 1
Read Mode	Latency Count				WAIT Polarity	R	WAIT Delay	Reserved	Burst Length		
15	14	13	12	11	10	9	8	7:3	2	1	0

Bit	Name	Description
15	Read Mode	0 = Synchronous burst-mode reads 1 = Asynchronous page-mode reads (default)
14:11	Latency Count	Bits: 14 13 12 11 0 0 1 1 = 3 0 1 0 0 = 4 0 1 0 1 = 5 0 1 1 0 = 6 0 1 1 1 = 7 1 0 0 0 = 8 1 0 0 1 = 9 1 0 1 0 = 10 1 0 1 1 = 11 1 1 0 0 = 12 (Other bit settings are reserved)
10	WAIT Polarity	0 = WAIT signal is active low (default) 1 = WAIT signal is active high
9	Reserved	Write 0 to reserved bits
8	WAIT Delay	0 = WAIT de-asserted with valid data 1 = WAIT de-asserted one cycle before valid data (default)
7:3	Reserved	Write 0 to reserved bits
2:0	Burst Length	0 1 0 = 8-word burst (wrap only) 0 1 1 = 16-word burst (wrap only) 1 1 1 = Continuous-word burst (no-wrap; default) (Other bit settings are reserved)

9.2.1 Latency Count

The Latency Count value programmed into RCR[14:11] is the number of valid CLK edges from address-latch to the start of the data-output delay. When the Latency Count has been satisfied, output data is driven after tCHQV.

Figure 46: Latency Count Period



Notes:
1. Address latched on valid clock edge with ADV# low and LC count begins.
2. Address latched on ADV# rising edge. LC count begins on subsequent valid CLK edge.

Table 32: CLK Frequencies for LC Settings

V_{CCQ} = 1.7 V to 2.0 V	
Latency Count Setting	**Frequency Supported (MHz)**
3	≤ 32.6 MHz
4	≤ 43.5 MHz
5	≤ 54.3 MHz
6	≤ 65.2 MHz
7	≤ 76.1 MHz
8	≤ 87 MHz
9	≤ 97.8 MHz
10	≤ 108.7 MHz
11	≤ 119.6 MHz
12	≤ 130.4 MHz
13	≤ 133.3 MHz

9.3 Enhanced Configuration Register

The Enhanced Configuration Register (ECR) is a volatile 16-bit, read/write register used to select Deep Power Down (DPD) operation and to modify the output-driver strength of the flash device. All Enhanced Configuration Register bits are set and cleared using the Program Enhanced Configuration Register command. Upon power-up or exit from reset, the Enhanced Configuration Register defaults to 0004h.

To read the value of the ECR, issue the Read Device Information command to the desired partition. Subsequent reads from the <partition base address> + 06h returns ECR[15:0].

Table 33: Enhanced Configuration Register Bit Definitions

Enhanced Configuration Register					Default = 0004h
Deep Power Down (DPD) Mode	DPD Polarity	Reserved	Output Driver Control		
15	14	13:3	2	1	0

Bit	Name	Description
15	Deep Power Down (DPD) Mode	0 = DPD Disabled (default) 1 = DPD Enabled
14	DPD Pin Polarity	0 = Active Low (default) 1 = Active High
13:3	Reserved	Write 0 to reserved bits
2:0	Output Driver Control	Bits: 2 1 0 0 0 1 = 1 0 1 0 = 2 0 1 1 = 3 1 0 0 = 4 (default) 1 0 1 = 5 1 1 0 = 6 (Other bit settings are reserved)

9.3.1 Output Driver Control

Output Driver Control enables the user to adjust the device's output-driver strength of the data I/O bus and WAIT signal. Upon power-up or reset, ECR[2:0] defaults to an output impedance setting of 30 Ohms. To change the output-driver strength, ECR[2:0] must be programmed to the desired setting as shown in Table 34, "Output Driver Control Characteristics".

Table 34: Output Driver Control Characteristics

Control Bits ECR[2:0]	Impedance @ VCCQ/2 (Ohm)	Driver Multiplier	Load Driven at Same Speed (pF)
001 (1)	90	1/3	10
010 (2)	60	1/2	15
011 (3)	45	2/3	20
100 (4) default	30	1	30
101 (5)	20	3/2	35
110 (6)	15	2	40

9.3.2 Programming the ECR

The ECR is programmed by issuing the Program Enhanced Configuration Register command. This is a two-cycle command sequence requiring a Setup command to be issued first, followed by a Confirm command. Bus-write cycles to the flash device between the setup and confirm commands are not allowed—a command sequence error will result. However, flash bus-read cycles between the Setup and Confirm commands are allowed.

Table 35: Program Enhanced Configuration Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Program Enhanced Configuration Register	Register Data	0060h	Register Data	0004h

To program the Enhanced Configuration Register, the desired settings for ECR[15:0] are placed on the address bus. The setup command (0060h) is driven on the data bus. Upon issuing the setup command, the device/addressed partition is automatically changed to Read Status Register mode.

Next, the Confirm command (0004h) is driven on the data bus. After issuing the Confirm command, the addressed partition is automatically switched to Read Array mode.

This command functions independently of the applied VPP voltage.

Note: Since the desired register value is placed on the address lines, any hardware-connection offsets between the host's address outputs and the flash device's address inputs must be considered, similar to programming the RCR.

9.4 Read Operations

The following types of data can be read from the device: array data, device information, CFI data, and device status Upon power-up or return from reset, the device defaults to Read Array mode. To change the device's read mode, the appropriate command must be issued to the device. Table 36, "Read Mode Command Bus Cycles" shows the command codes used to configure the device for the desired read mode. The following sections describe each read mode.

Table 36: Read Mode Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Read Array	Partition Address	00FFh	---	---
Read Status Register	Partition Address	0070h	---	---
Read Device Information	Partition Address	0090h	---	---
CFI Query	Partition Address	0098h	---	---

9.4.1 Read Array

Upon power-up or exit from reset, the device defaults to Read Array mode. Issuing the Read Array command places the addressed partition in Read Array mode. Subsequent reads output array data. The addressed partition remains in Read Array mode until a different read command is issued, or a program or erase operation is performed in that partition, in which case, the read mode is automatically changed to Read Status.

To changea partition to Read Array mode while it is programming or erasing, first issue the Suspend command. After the operation has been suspended, issue the Read Array command to the partition. When the program or erase operation is subsequently resumed, the read state of the partition will not change. To change the read state of the partition to Status read mode, issue a Read Status command to the partition.

Note: Issuing the Read Array command to a partition that is actively programming or erasing causes subsequent reads from that partition to output invalid data. Valid array data is output only after the program or erase operation has finished.

The Read Array command functions independent of the voltage level on VPP.

9.4.2 Read Status Register

Issuing the Read Status Register command places the addressed partition in Read Status Register mode. Subsequent reads from that partition output Status Register information. The addressed partition remains in Read Status Register mode until a different read-mode command is issued to that partition. Performing a program, erase, or block-lock operation also changes the partition's read mode to Read Status Register mode.

The Status Register is updated on the falling edge of CE#, or OE# when CE# is low. Status Register contents are valid only when SR7 = 1.

The Read Status Register command functions independent of the voltage level on VPP.

9.4.3 Read Device Information

Issuing the Read Device Information command places the addressed partition in Read Device Information mode. Subsequent reads output device information on the data bus. The address offsets for reading the available device information are shown here.

Table 37: Device Information Summary

Device Information	Address Bus	Data Bus
Device Manufacturer Code (Numonyx)	Partition Base Address + 00h	0089h
Device ID Code	Partition Base Address + 01h	Device IDs
Main Block Lock Status	Block Base Address + 02h	D0 = Lock Status D1 = Lock-Down Status
Read Configuration Register	Partition Base Address + 05h	Configuration Register Data
Enhanced Configuration Register	Partition Base Address + 06h	Enhanced Configuration Register Data
OTP Lock Register 0	Partition Base Address + 80h	Lock Register 0 Data
OTP Register - Factory Segment	Partition Base Address + 81h to 84h	Factory-Programmed Data
OTP Register - User-Programmable Segment	Partition Base Address + 85h to 88h	User Data
OTP Lock Register 1	Partition Base Address + 89h	Lock Register 1 Data
OTP Registers 1 through 16	Partition Base Address + 8Ah to 109h	User Data

The addressed partition remains in Read Device Information mode until a different read command is issued. Also, performing a program, erase, or block-lock operation changes the addressed partition to Read Status Register mode.

Note: Issuing the Read Device Information command to a partition that is actively programming or erasing changes that partition's read mode to Read Device Information mode. Subsequent reads from that partition will return invalid data until the program or erase operation has completed.

The Read Device Information command functions independent of the voltage level on VPP.

9.4.4 CFI Query

Issuing the CFI Query command places the addressed partition in CFI Query mode. Subsequent reads from that partition output CFI information.

The addressed partition remains in CFI Query mode until a different read command is issued, or a program or erase operation is performed, which changes the read mode to Read Status Register mode.

Note: Issuing the CFI Query command to a partition that is actively programming or erasing changes that partition's read mode to CFI Query mode. Subsequent reads from that partition will return invalid data until the program or erase operation has completed.

The CFI Query command functions independent of the voltage level on VPP.

9.5 Programming Modes

To understand programming modes, it is also important to understand the fundamental memory array configuration. The flash device main array is divided as follows:

- The main array of the 128-Mbit device is divided into eight 16-Mbit partitions. Each parition is divided into eight 256-KByte blocks: 8 x 8 = 64 blocks in the main array of a 128-Mbit device.
- The main array of the 256-Mbit device is divided into eight 32-Mbit partitions. Each partition is divided into sixteen 256-KByte blocks: 8 x 16 = 128 blocks in the main array of a 256-Mbit device.
- The main array of the 512-Mbit device is divided into eight 64-Mbit partitions. Each partition is divided into thirty-two 256-KByte blocks: 8 x 32 = 256 blocks in the main array of a 256-Mbit device.
- The main array of the 1-Gbit device is divided into eight 128-Mbit partitions. Each partition is divided into sixty-four 256-KByte blocks: 8 x 64 = 512 blocks in the main array of a 1-Gbit device.

Each block is divided into as many as two-hundred-fifty-six 1-KByte programming regions. Each region is divided into as many as thirty-two 32-Byte segments.

Each programming region in a flash block can be configured for one of two programming modes: Control Mode or Object Mode. The programming mode is automatically set based on the data pattern when a region is first programmed. The selection of either Control Mode or Object Mode is done according to the specific needs of the system with consideration given to two types of information:

- Control Mode: Flash File System (FFS) or Header information, including frequently changing code or data
- Object Mode: Large, infrequently changing code or data, such as objects or payloads

By implementing the appropriate programming mode, software can efficiently organize how information is stored in the flash memory array.

Control Mode programming regions and Object Mode programming regions can be intermingled within the same erase block. However, the programming mode of any region within a block can be changed only after erasing the entire block.

9.5.1 Control Mode

Control Mode programming is invoked when only the A-half (A3 = 0) of the programming region is programmed to 0s, as shown in Figure 47, “Configurable Programming Regions: Control Mode and Object Mode” on page 85. The B-half (A3 = 1) remains erased. Control mode allows up to 512 bytes of data to be programmed in the region. The information can be programmed in bits, bytes, or words.

Control Mode supports the following programming methods:

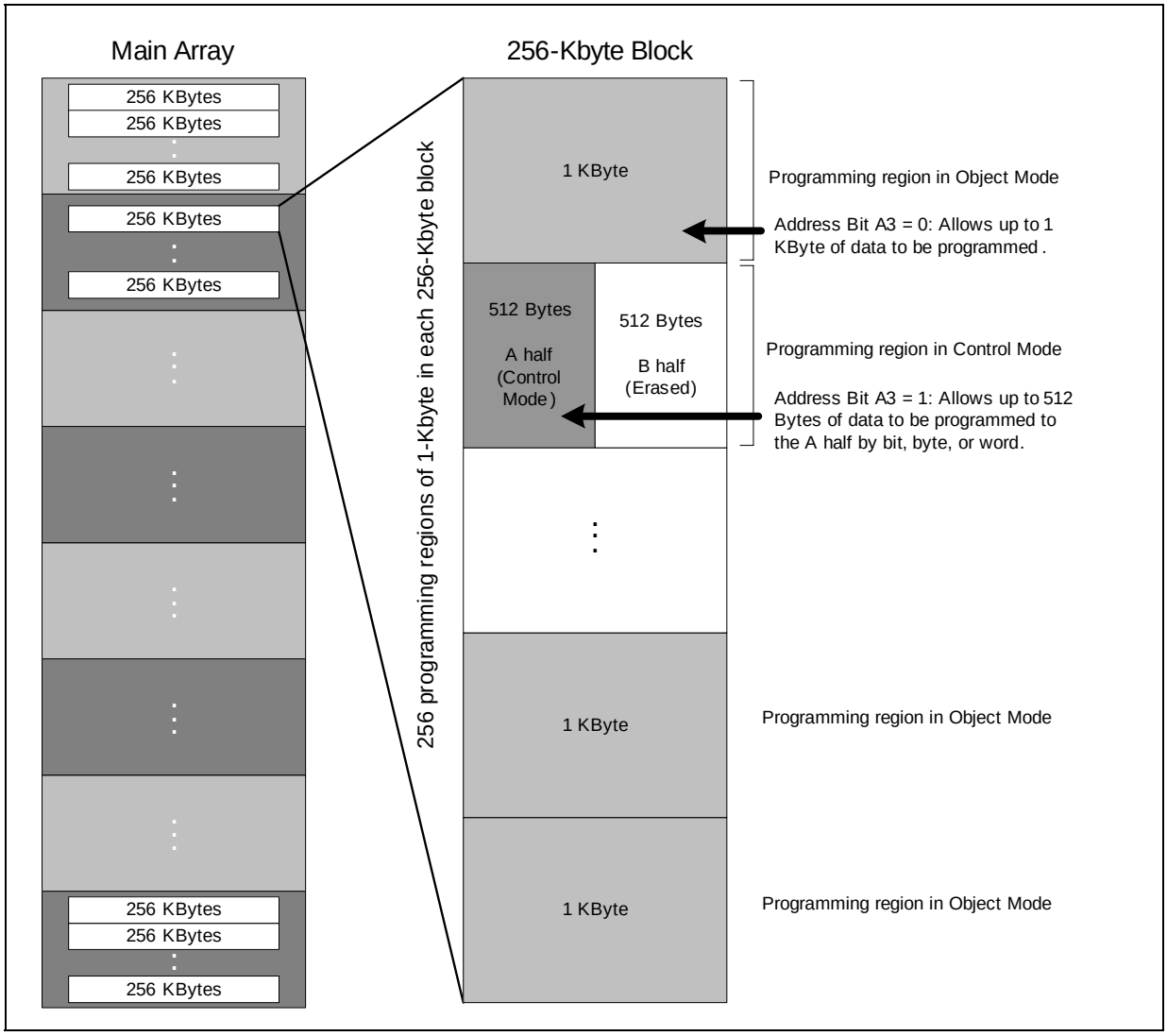
- Single-word Programming (0041h)
- Buffered Programming (00E9h/00D0h), and
- Buffered Enhanced Factory Programming (0080h/00D0h)

When buffered programming is used in Control Mode, all addresses must be in the A-half of the buffer (A3 = 0). During buffer fill, the B-half (A3 = 1) addresses do not need to be filled with 0xFFFF.

Control Mode programming is useful for storing dynamic information, such as FFS Headers, File Info, and so on. Typically, Control Mode programming does not require the entire 512 bytes of data to be programmed at once. It may also contain data that is changed after initial programming using a technique known as “bit twiddling”. Header information can be augmented later with additional new information within a Control Mode-programmed region. This allows implementation of legacy file systems, as well as transaction-based power-loss recovery.

In a control mode region, programming operations can be performed multiple times. However, care must be taken to avoid programming any zero’s in the B-half (A3 = 1) of the region. Violation of this usage will cause SR4 and SR9 to be set, and the program operation will be aborted. See Table 38, “Programming Region Next State Table” on page 88 for details.

Figure 47: Configurable Programming Regions: Control Mode and Object Mode



9.5.2 Object Mode

Object mode programming is invoked when one or more bits are programmed to zero in the B-half of the programming region (A3 = 1). Object mode allows up to 1KB to be stored in a programming region. Multiple regions are used to store more than 1Kbyte of information. If the object is less than 1Kbyte, the unused content will remain as 0xFFFF (erased).

Object Mode supports two programming methods:

— Buffered Programming (00E9h/00D0h), and

— Buffered Enhanced Factory Programming (0080h/00D0h)

Single-word programming (0041h) is not supported in Object mode. To perform multiple programming operations within a programming region, Control mode must be used.

Object mode is useful for storing static information, such as objects or payloads, that rarely change.

Once the programming region is configured in Object mode, it cannot be augmented or over-written without first erasing the entire block containing the region. Subsequent programming operations to a programming region configured in Object mode will cause SR4 and SR8 to be set and the program operation to be aborted. See Table 38, “Programming Region Next State Table” on page 88 for details.

Note: Issuing the 41h command to the B-half of an erased region will set error bits SR8 and SR9, and the programming operation will not proceed. See Table 38, “Programming Region Next State Table” on page 88 for more details.

Figure 48: Configurable Programming Regions: Control Mode and Object Mode Segments

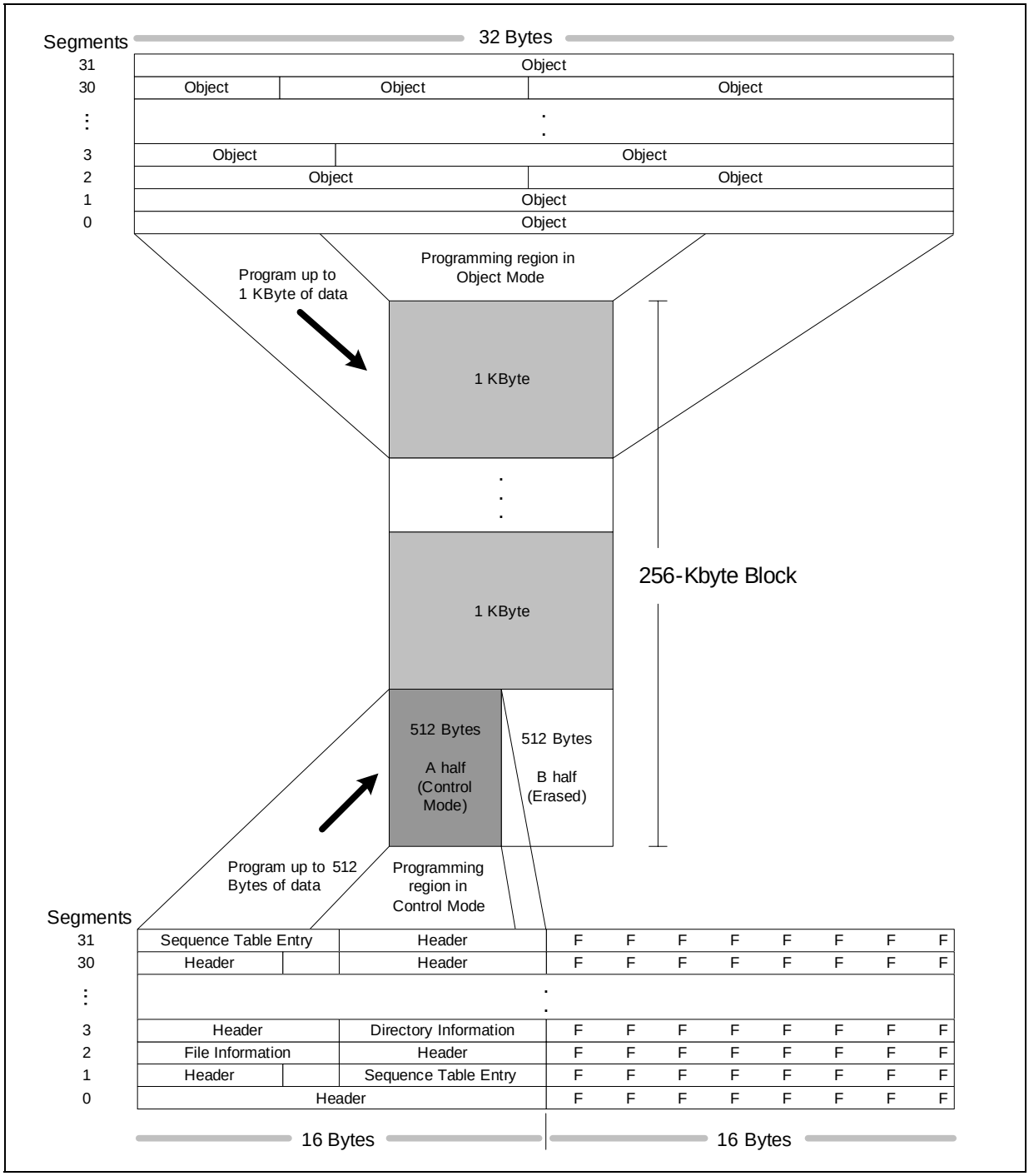


Table 38: Programming Region Next State Table

Current State of Programming Region	Command Issued			
	0041h to B-half (A3 = 1)	0041h to A-half (A3 = 0)	00E9h to B-half (A3 = 1)	00E9h to A-half (A3 = 0)
Erased	Program Fail; Illegal Command SR[4,8,9] = 1	Program Successful SR[4,8,9] = 0 Region configured to Control Mode	Program Successful SR[4,8,9] = 0 Region configured to Object Mode	Program Successful SR[4,8,9] = 0 Region configured to Control Mode
Control Mode		Program Successful SR[4,8,9] = 0	Program Fail; Object data to Control mode region SR[4,9] = 1 SR8 = 0	Program Successful SR[4,8,9] = 0
Object Mode		Program Fail; Rewrite to Object mode region SR[4,8] = 1 SR9 = 0		

9.6 Programming Operations

Programming the flash array changes ‘ones’ to ‘zeros’. To change zeros to ones, an Erase operation must be performed. Only one programming operation can occur at a time. Programming is permitted during Erase Suspend.

Information is programmed into the flash array by issuing the appropriate command. Table 39, “Programming Commands Bus Cycles” shows the two-cycle command sequences used for programming.

Table 39: Programming Commands Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Single-Word Program	Device Address	0041h	Device Address	Array Data
Buffered Program	Device Address	00E9h	Device Address	00D0h
Buffered Enhanced Factory Program	Device Address	0080h	Device Address	00D0h

Caution: **All programming operations require the addressed block to be unlocked, and a valid V_{PP} voltage applied throughout the programming operation. Otherwise, the programming operation will abort, setting the appropriate Status Register error bit(s).**

The following sections describe each programming method.

9.6.1 Single-Word Programming

Main array programming is performed by first issuing the Single-Word Program command. This is followed by writing the desired data at the desired array address. The read mode of the addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

Note: Issuing the Read Status Register command to another partition switches that partition's read mode to Read Status Register mode, thereby allowing programming progress to be monitored from that partition's address.

Single-Word Programming is supported in Control mode only. The array address specified must be in the A-half of the programming region.

During programming, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1). The Status Register should be checked for any errors, then cleared.

The only valid commands during programming are Read Array, Read Device Information, CFI Query, Read Status and Program Suspend. After programming has finished, any valid command can be issued.

Note: Issuing the Read Array, Read Device Information, or CFI Query command to a partition that is actively programming causes subsequent reads from that partition to output invalid data. Valid data is output only after the program operation has finished.

Standby power levels are not realized until the programming operation has finished. Asserting RST# immediately aborts the programming operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed.

9.6.2 Buffered Programming

Buffered Programming programs multiple words simultaneously into the flash memory array. Data is first written to a write buffer and then programmed into the flash memory array in buffer-size increments. This can significantly reduce the effective word-write time. Section 6.0, "Flow Charts" on page 41 contains a flow chart of the buffered-programming operation.

Note: Optimal performance and power consumption is realized only by aligning the start address on 32-word boundaries, e.g., A[4:0] = 00000b. Crossing a 32-word boundary during a Buffered Programming operation can cause the programming time to double.

Buffered Programming is supported in both Control mode and Object mode. In Object mode, the region must be programmed only once between erases. However in Control mode, the region may be programmed multiple times.

Caution: **When using the Buffered Program command in Object mode, the start address must be aligned to the 512-word buffer boundary. In Control mode, the programming array address specified must be in the A-half of the programming region.**

First issue the Read Status command to the desired partition. The read mode of the addressed partition is changed to Read Status Register mode.

Poll SR7 to determine write-buffer availability (0 = not available, 1 = available). If the write buffer is not available, re-issue the Read Status command and check SR7; repeat until SR7 = 1.

If desired issue a Read Array command to the desired partition to change the read mode of the partition to Array reads.

To perform a buffered programming operation, issue the Buffered Program setup command at the desired starting address. Next, issue a word count at the desired starting address. The word count is the total number of words to be written into the write buffer, minus one. This value can range from 0000h (one word) up to a maximum of 01FFh (512 words). Exceeding the allowable range causes the operation to abort.

Following the word count, subsequent bus-write cycles fill the write buffer with user-data up to the word count.

Note: User-data is programmed into the flash array at the address issued when filling the write buffer.

The Confirm command (00D0h) is issued after all user-data is written into the write buffer. The read mode of the device/addressed partition is automatically changed to Read Status Register mode. If other than the Confirm command is issued to the device, a command sequence error occurs and the operation aborts.

After the Confirm command has been issued, the write-buffer contents are programmed into the flash memory array. The Status Register indicates a busy status (SR7 = 0) during array programming.

During array programming, the only valid commands are Read Array, Read Device Information, CFI Query, Read Status, and Program Suspend. After array programming has completed (SR7 = 1), any valid command can be issued. Reading from another partition is allowed while data is being programmed into the flash memory array from the write buffer.

Note: Issuing the Read Array, Read Device Information, or CFI Query command to a partition that is actively programming or erasing causes subsequent reads from that partition to output invalid data. Valid data is output only after the program or erase operation has finished.

Upon completion of array programming, the Status Register indicates ready (SR7 = 1b). A full Status Register check should be performed to check for any programming errors. Then the Status Register should be cleared using the Clear Status Register command.

A subsequent buffered programming operation can be initiated by repeating the buffered programming sequence. Any errors in the Status Register caused by the previous operation must be cleared to prevent them from masking any errors that may occur during the subsequent operation.

9.6.3 Buffered Enhanced Factory Programming (BEFP)

Buffered Enhanced Factory Programming (BEFP) improves programming performance through the use of the write buffer, elevated programming voltage (V_{PPH}), and enhanced programming algorithm. User-data is written into the write buffer, then the buffer contents are automatically written into the flash array in buffer-size increments.

BEFP is allowed in both Control Mode and Object Mode. The programming mode selection for the entire flash array block is driven by the specific type of information, such as header or object data. Header/object data is aligned on a 1 KB programming region boundary in the main array block.

Internal verification during programming (inherent to MLC technology) and Status Register error checking are used to determine proper completion of the programming operation. This eliminates delays incurred when switching between single-word program and verify operations.

BEFP consists of three distinct phases:

1. Setup Phase: V_{PPH} and block-lock checks
2. Program/Verify Phase: buffered programming and verification
3. Exit Phase: block-error check

Section 6.0, "Flow Charts" on page 41 contains a flow chart of the BEFP operation. Table 40, "BEFP Requirements and Considerations" on page 91 lists specific BEFP requirements and considerations.

Note: For BEFP voltage and temperature operating restrictions, see the datasheet. The block erase cycles in Table 40, "BEFP Requirements and Considerations" are recommended for optimal performance. If exceeded some degradation in performance may occur; however, the internal algorithm will still function correctly.

Table 40: BEFP Requirements and Considerations

BEFP Requirements	Temperature (T_{CASE}) must be 25 °C, ± 5 °C
	Voltage on V_{CC} must be within the allowable operating range
	Voltage on VPP must be within the allowable operating range
	Block being programmed must be erased and unlocked
BEFP Considerations	Block cycling below 100 erase cycles
	Reading from another partition during EFP (RWW) is not allowed
	BEFP programs within one block at a time
	BEFP cannot be suspended

9.6.3.1 Setup Phase

Issuing the BEFP Setup and Confirm command sequence starts the BEFP algorithm. The read mode of the addressed partition is automatically changed to Read Status Register mode.

The address used when issuing the setup/confirm commands must be buffer-size aligned within the block being programmed -- buffer contents cannot cross block boundaries.

Caution: **The Read Status Register command must not be issued -- it will be interpreted as data to be written to the write buffer.**

A setup delay ($t_{BEFP/Setup}$) occurs while the internal algorithm checks V_{PP} and block-lock status. If errors are detected, the appropriate Status Register error bits are set and the operation aborts.

The Status Register should be polled for successful BEFP setup, indicated by SR[7,0] = 0 (Device Busy, Buffer Ready for Data).

9.6.3.2 Program / Verify Phase

Data is first written into the write buffer, then programmed into the flash array. During the buffer-fill sequence, the address used must be buffer-size aligned. Use of any other address will cause the operation to abort with a program fail error, and any data previously loaded in the buffer will not be programmed into the array.

The buffer-fill data is stored in sequential buffer locations starting at address 00h. A word count equal to the maximum buffer size is used, therefore, the buffer must be completely filled. If the amount of data is less than the maximum buffer size, the remaining buffer locations must be "padded" with FFFFh to completely fill the buffer.

Flash array programming starts as soon as the write buffer is full. Data words from the write buffer are programmed into sequential array locations. SR0 = 1 indicates the write buffer is not available while the BEFP algorithm programs the array.

The Status Register should be polled for SR0 = 0 (Buffer Ready for Data) to determine when the array programming has completed, and the write buffer is again available for loading. The internal address is automatically incremented to enable subsequent array programming to continue from where the previous buffer-fill/array-program sequence ended within the block. This cycle can be repeated to program the entire block.

To exit the Program/Verify Phase, write FFFFh to an address outside of the block.

9.6.3.3 Exit Phase

The Status Register should be polled for SR7 = 1 (Device Ready) indicating the BEFP algorithm has finished running, and the device has returned to normal operation. A full error check should be performed to ensure the block was programmed successfully.

9.7 Block Erase Operations

Erasing a block changes ‘zeros’ to ‘ones’. To change ones to zeros, a program operation must be performed (see Section 9.6, “Programming Operations). Erasing is performed on a block basis— an entire block is erased each time an erase command sequence is issued. Once a block is fully erased, all addressable locations within that block read as logical ‘ones’ (FFFFh).

Only one block-erase operation can occur at a time. A block-erase operation is not permitted during Program Suspend.

To perform a block-erase operation, issue the Block Erase command sequence at the desired block address. Table 41 shows the two-cycle Block Erase command sequence.

Table 41: Block-Erase Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Block Erase	Device Address	0020h	Block Address	00D0h

Caution: **All block-erase operations require the addressed block to be unlocked, and a valid voltage applied to VPP throughout the block-erase operation. Otherwise, the operation aborts, setting the appropriate Status Register error bit(s).**

The Erase Confirm command latches the address of the block to be erased. The addressed block is preconditioned (programmed to all zeros), erased, and then verified. The read mode of the addressed partition is automatically changed to Read Status Register mode, and remains in effect until another read-mode command is issued.

Note: Issuing the Read Status Register command to another partition switches that partition’s read mode to the Read Status Register, thereby allowing block-erase progress to be monitored from that partition’s address. SR0 indicates whether the addressed partition or other partition is erasing.

During a block-erase operation, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1). The Status Register should be checked for any errors, and then cleared.

The only valid commands during a block erase operation are Read Array, Read Device Information, CFI Query, Read Status and Erase Suspend. After the block-erase operation has completed, any valid command can be issued.

Note: Issuing the Read Array command to a partition that is actively erasing a main block causes subsequent reads from that partition to output invalid data. Valid array data is output only after the block-erase operation has finished.

Standby power levels are not realized until the block-erase operation has finished. Asserting RST# immediately aborts the block-erase operation, and array contents at the addressed location are indeterminate. The addressed block should be erased, and the data re-programmed.

9.8 Blank Check Operation

Blank Check is used to see if a main-array block is completely erased. A Blank Check operation is performed one block at a time, and cannot be used during Program Suspend or Erase Suspend.

To use Blank Check, first issue the Blank Check setup command followed by the confirm command. The read mode of the addressed partition is automatically changed to Read Status Register mode, which remains in effect until another read-mode command is issued.

Table 42: Blank Check Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Blank Check	Block Address	00BCh	Block Address	00D0h

During a blank check operation, the Status Register indicates a busy status (SR7 = 0). Upon completion, the Status Register indicates a ready status (SR7 = 1).

Note: Issuing the Read Status Register command to another partition switches that partition's read mode to Read Status Register mode, thereby allowing the blank check operation to be monitored from that partition's address.

The Status Register should be checked for any errors, and then cleared. If the Blank Check operation fails, i.e., the block is not completely erased, then the Status Register will indicate a Blank Check error (SR[7,5] = 1).

The only valid command during a Blank Check operation is Read Status. Blank Check cannot be suspended. After the blank check operation has completed, any valid command can be issued.

9.9 Suspend and Resume

Program and erase operations of the main array can be suspended to perform other device operations, and then subsequently resumed. However, OTP Register programming or blank check operations cannot be suspended.

To suspend an on-going erase or program operation, issue the Suspend command to any device address; the corresponding partition is not affected. Table 43 shows the Suspend and Resume command bus-cycles.

Note: Issuing the Suspend command does not change the read mode of the partition. The partition will be in Read Status Register mode from when the erase or program command was first issued, unless the read mode was changed prior to issuing the Suspend command.

Table 43: Suspend and Resume Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Suspend	Device Address	00B0h	---	---
Resume	Device Address	00D0h	---	---

The program or erase operation suspends at pre-determined points during the operation after a delay of t_{SUSP}. Suspend is achieved when SR[7,6] = 1 (erase-suspend) or SR[7,2] = 1 (program-suspend).

Note: Throughout the Block Erase Suspend or Program Suspend period, the addressed block must remain unlocked and a valid voltage applied to VPP. Otherwise, the erase or program operation will abort, setting the appropriate Status Register error bit(s). Also, WP# must remain unchanged.

Asserting RST# aborts suspended block-erase and programming operations -- array contents at the addressed locations are indeterminate. The addressed block should be erased, and the data re-programmed.

Not all commands are allowed when the device is suspended. Table 44 shows which device commands are allowed during Program Suspend or Erase Suspend.

Table 44: Valid Commands During Suspend

Device Command	Program Suspend	Erase Suspend
Read Array	Allowed	Allowed
Read Status Register	Allowed	Allowed
Clear Status Register	Allowed	Allowed
Read Device Information	Allowed	Allowed
CFI Query	Allowed	Allowed
Word Program	Not Allowed	Allowed
Buffered Program	Not Allowed	Allowed
Buffered Enhanced Factory Program	Not Allowed	Not Allowed
Block Erase	Not Allowed	Not Allowed
Program/Erase Suspend	Not Allowed	Not Allowed
Program/Erase Resume	Allowed	Allowed

During Suspend, reading from a block that is being erased or programmed is not allowed. Also, programming to a block that is in erase-suspend state is not allowed, and if attempted, will result in Status Register program error to be set (SR4 = 1).

A block-erase under program-suspend is not allowed. However, word-program under erase-suspend is allowed, and can be suspended. This results in a simultaneous erase-suspend/ program-suspend condition, indicated by SR[7,6,2] = 1.

To resume a suspended program or erase operation, issue the Resume command to any device address. The read mode of the resumed partition is unchanged; issue the Read Status Register command to return the partition to Read Status mode. The operation continues where it left off, and the respective Status Register suspend bits are cleared.

When the Resume command is issued during a simultaneous erase-suspend/ program-suspend condition, the programming operation is resumed first. Upon completion of the programming operation, the Status Register should be checked for any errors, and cleared. The resume command must be issued again to complete the erase operation. Upon completion of the erase operation, the Status Register should be checked for any errors, and cleared.

9.10 Simultaneous Operations

The multi-partition architecture of the flash device allows programming or erasing to occur in one partition while reads are performed from another partition. Only status reads are allowed in partitions that are busy programming or erasing.

Note: When OTP Registercommands are issued to a parameter any partition address, the OTP Registeris mapped onto that partition.

Table 45, "Read-While-Program and Read-While-Erase Rules" shows the rules for reading from a partition while simultaneously programming or erasing within another partition.

Table 45: Read-While-Program and Read-While-Erase Rules

	Read modes allowed when program / erase busy in partition A		
Active Operation	**Read Status**	**Array Reads**	**Non-Array Reads[1]**
Main-Array Program	All partitions	All partitions except busy partition A	All partitions except busy partition A
Main-Array Erase	All partitions	All partitions except busy partition A	All partitions except busy partition A
OTP Register Program	All partitions	All partitions except busy partition A	Not allowed

Note: OTP Register, Device Information, CFI Query.

9.11 Security

The flash device incorporates features for protecting main-array contents and for implementing system-level security schemes. The following sections describe the available features.

9.11.1 Block Locking

Two methods of block-lock control are available: software and hardware. Software control uses the Block Lock and Block Unlock commands; hardware control uses WP# along with the Block Lock-Down command.

Upon power up or exit from reset, all main array blocks are locked, but not locked down. Locked blocks cannot be erased or programmed.

Block lock and unlock operations are independent of the voltage level on V_{PP}.

Table 46 summarizes the command bus-cycles.

Table 46: Block Locking Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Lock Block	Block Address	0060h	Block Address	0001h
Unlock Block	Block Address	0060h	Block Address	00D0h
Lock-Down Block	Block Address	0060h	Block Address	002Fh

To lock, unlock, or lock-down a block, first issue the setup command to any address within the desired block. The read mode of the addressed partition is automatically changed to Read Status Register mode. Next, issue the desired confirm command to the block's address. Note that the confirm command determines the operation performed. The Status Register should be checked for any errors, and then cleared.

The lock status of a block can be determined by issuing the Read Device Information command, and then reading from <block base address> + 02h. DQ0 indicates the lock status of the addressed block (0 = unlocked, 1 = locked), and DQ1 indicates the lock-down status of the addressed block (0 = lock-down not issued; 1 = locked-down issued). Section 9.4.3, "Read Device Information" on page 82 summarizes the details of this operation.

Blocks cannot be locked or unlocked while being actively programmed or erased. Blocks can be locked or unlocked during erase-suspend, but not during program-suspend.

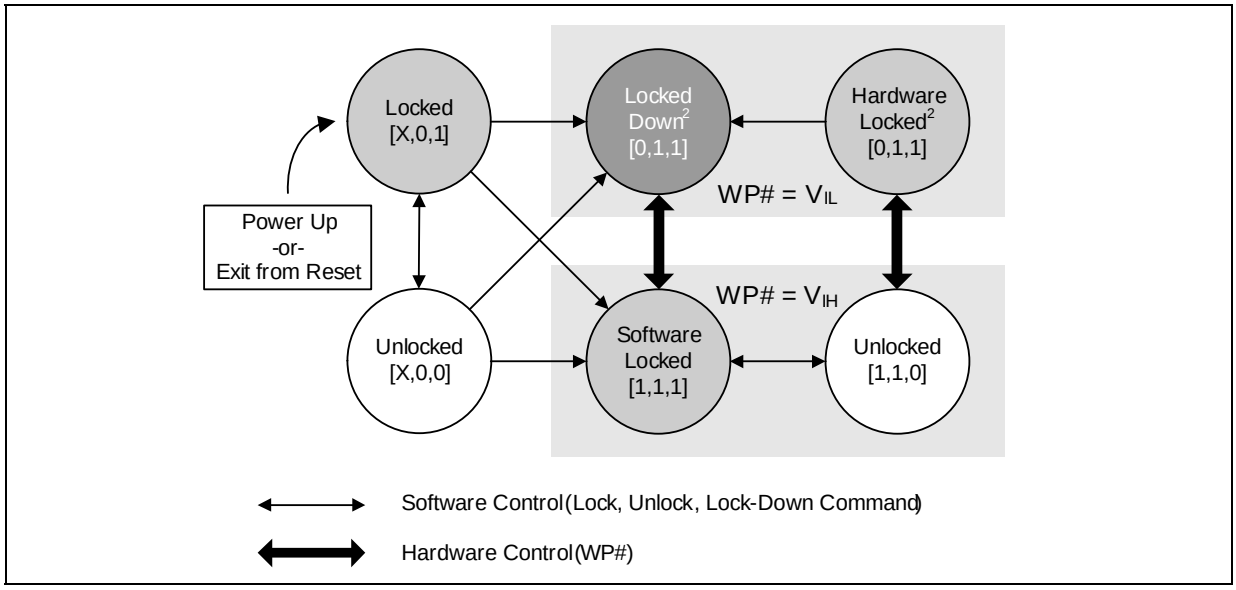
Note: If a block-erase operation is suspended, and then the block is locked or locked down, the lock status of the block will be changed immediately. When resumed, the erase operation will still complete.

Block lock-down protection is dependent on WP#. When WP# = V_{IL}, blocks locked down are locked, and cannot be unlocked using the Block Unlock command. When WP# = V_{IH}, block lock-down protection is disabled—locked-down blocks can be individually unlocked using the Block Unlock command. Subsequently, when WP# = V_{IL}, previously locked-down blocks are once again locked and locked-down, including locked-down blocks that may have been unlocked while WP# was de-asserted.

A locked-down block can only be unlocked by issuing the Unlock Block command with WP# deasserted. To return an unlocked block to the locked-down state, a Lock-Down command must be issued prior to asserting WP#.

Issuing the Block Lock-Down command to an unlocked block does not lock the block. However, asserting WP# after issuing the Block Lock-Down command locks (and locks down) the block. Lock-down for all blocks is cleared upon power-up or exit from reset. Figure 49 summarizes block-locking operations.

Figure 49: Block Locking Operations



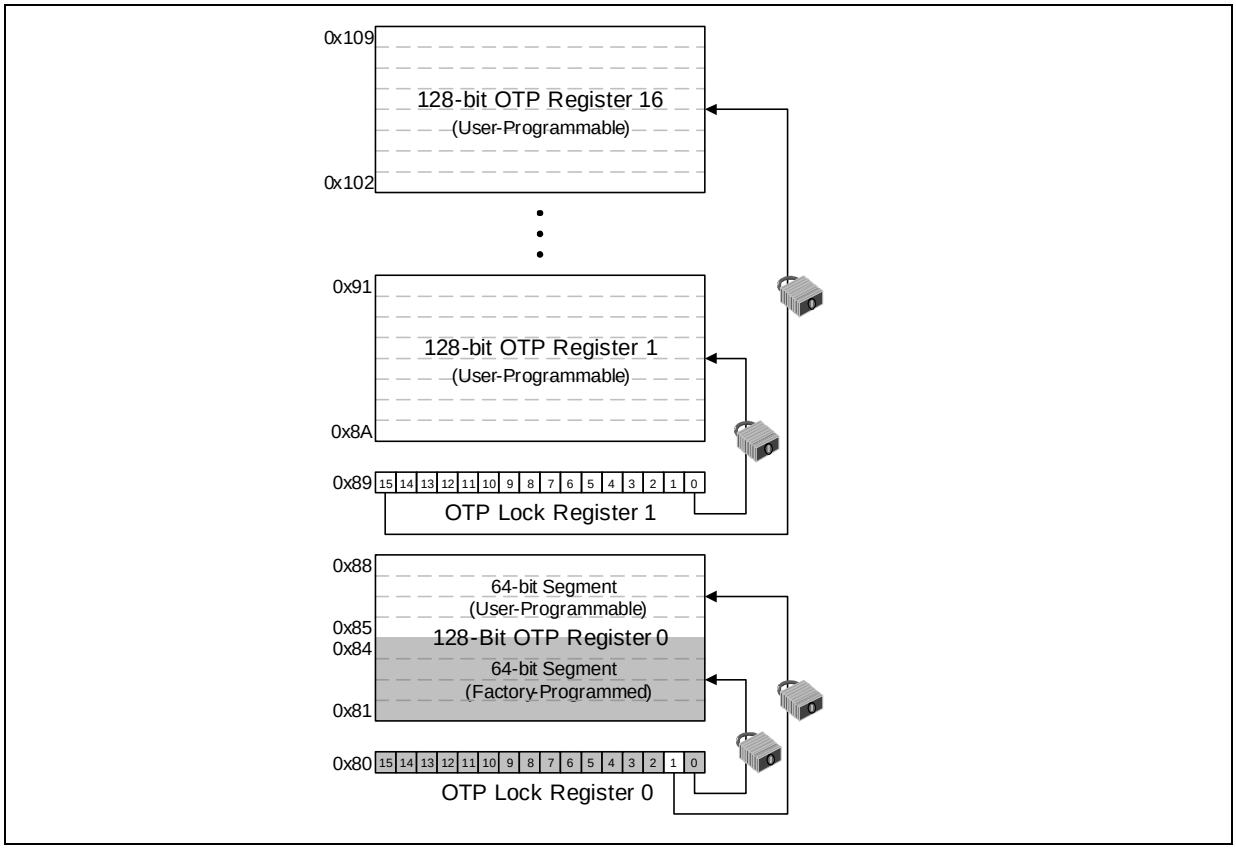
Notes:
1. [n,n,n] denotes logical state of WP#, DQ1,and DQ0, respectively; X = Don't Care.
2. [0,1,1] states should be tracked by system software to differentiate between the Hardware-Locked state and the Lock-Down state.

9.11.2 One-Time Programmable (OTP) Registers

The device contains seventeen 128-bit One-Time Programmable (OTP) Registers, and twoa 16-bit OTP Lock Registers, as shown in Figure 50, "2-Kbit OTP Registers" on page 98. The OTP Lock Register 0 is used for locking the OTP Register 0, and OTP Lock Register 1 is used for locking OTP Registers 1 through 16.

The OTP Register 0 consists of two 64-bit segments: a lower segment that is pre-programmed with a unique 64-bit value and locked at the factory; and an upper segment that contains all "ones" and is user-programmable. OTP Registers 1 through 16 contain all "ones" and are user-programmable.

Figure 50: 2-Kbit OTP Registers



Each register contains OTP bits that can only be programmed from “one” to “zero” - register bits cannot be erased from “zero” back to “one”. This feature makes the OTP registers particularly useful for implementing system-level security schemes, for permanently storing data, or for storing fixed system parameters.

OTP Lock Register bits “lock out” subsequent programming of the corresponding OTP register. Each OTP Register can be locked by programming its corresponding lock bit to zero. As long as an OTP register remains unlocked (that is, its lock bit = 1), any of its remaining “one” bits can be programmed to “zero”.

Caution: **Once an OTP Register is locked, it cannot be unlocked. Attempts to program a locked OTP Register will fail with error bits set.**

To program any OTP bits, first issue the Program OTP Register setup command at any device address. Next, write the desired OTP Register data at the desired OTP Register address. OTP Register and OTP Lock Register programming is performed 16 bits at a time; only “zeros” within the data word affect any change to the OTP register bits.

Table 47: Program OTP Register Command Bus Cycles

Command	Setup Write Cycle		Confirm Write Cycle	
	Address Bus	Data Bus	Address Bus	Data Bus
Program OTP Register	Device Address	00C0h	OTP Register Address	Register Data

Attempting to program an OTP register outside of the OTP register space causes a program error (SR4 = 1). Attempting to program a locked OTP Register causes a program error and a lock error (SR4 = 1, SR1 = 1).

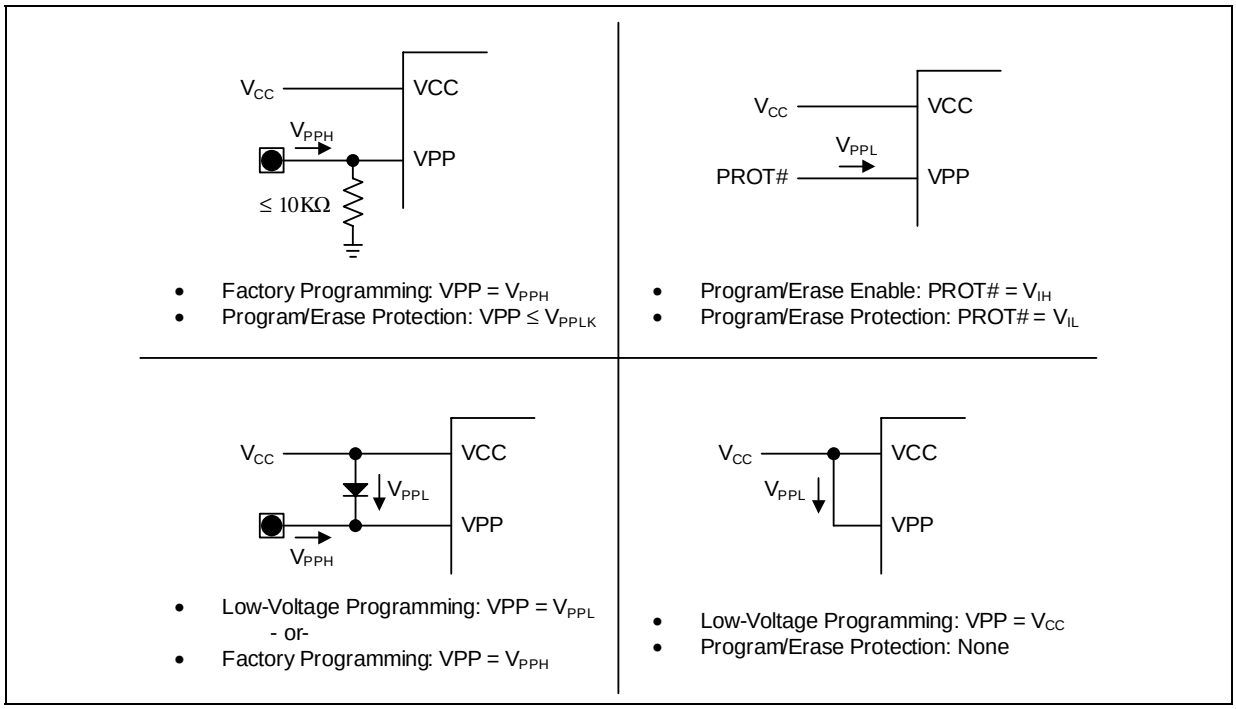
To read from any of the OTP registers, first issue the Read Device Information command. Then read from the desired OTP Register address offset. For additional details, refer to Section 9.4.3, "Read Device Information" on page 82.

9.11.3 Global Main-Array Protection

Global main-array protection can be implemented by controlling V_{PP}. When programming or erasing main-array blocks, V_{PP} must be equal to, or greater than V_{PPL} (min). When V_{PP} is below V_{PPLK}, program or erase operations are inhibited, thus providing absolute protection of the main array.

Various methods exist for controlling V_{PP}, ranging from simple logic control to off-board voltage control. Figure 51 shows example V_{PP} supply connections that can be used to support program/erase operations and main-array protection.

Figure 51: Example VPP Supply Connections



- Factory Programming: VPP = V_{PPH}
- Program/Erase Protection: VPP ≤ V_{PPLK}
- Program/Erase Enable: PROT# = V_{IH}
- Program/Erase Protection: PROT# = V_{IL}
- Low-Voltage Programming: VPP = V_{PPL}
  - or-
- Factory Programming: VPP = V_{PPH}
- Low-Voltage Programming: VPP = V_{CC}
- Program/Erase Protection: None

10.0 Device Command Codes

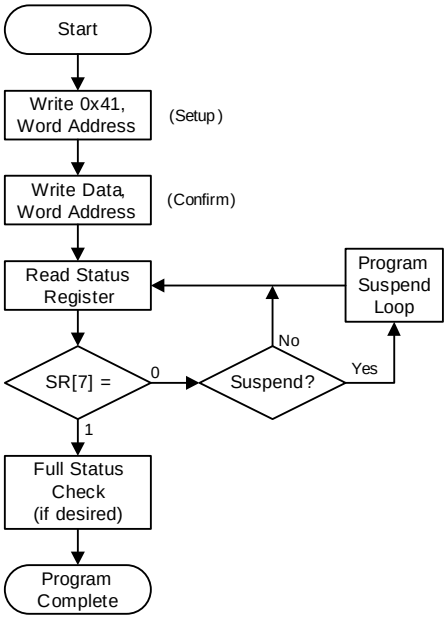
Table 48: Command Bus Operations

Command		Code (Setup/Confirm)	Description
Registers	Program Read Configuration Register	0060h/0003h	Issuing this command sequence programs the Read Configuration Register. The RCR value is placed on the address bus.
	Program Enhanced Configuration Register	0060h/0004h	Issuing this command sequence programs the Enhanced Configuration Register. The ECR value is placed on the address bus.
	Program OTP Register	00C0h	Issuing this command programs the Protection Registers or the Lock Registers associated with them.
Read Modes	Read Array	00FFh	Issuing this command places the addressed partition in Read Array mode. Subsequent reads outputs array data.
	Read Status Register	0070h	Issuing this command places the addressed partition in Read Status mode. Subsequent reads outputs Status Register data.
	Clear Status Register	0050h	Issuing this command clears all error bits in the Status Register.
	Read Device Information	0090h	Issuing this command places the addressed partition in Read Device Information mode. Subsequent reads from specified address offsets outputs unique device information.
	CFI Query	0098h	Issuing this command places the addressed partition in CFI Query mode. Subsequent reads from specified address offsets outputs CFI data.
Program/Erase Operations	Word Program	0041h	This command prepares the device for programming a single word into the flash array. On the next bus write cycle, the address and data are latched and written to the flash array. The addressed partition automatically switches to Read Status Register mode.
	Buffered Program	00E9h/00D0h	This command sequence initiates and executes a buffered programming operation. Additional bus write/read cycles are required between the setup and confirm commands to properly perform this operation. The addressed partition automatically switches to Read Status Register mode.
	Buffered Enhanced Factory Program	0080h/00D0h	This command sequence initiates and executes a BEFP operation. Additional bus write/read cycles are required after the confirm command to properly perform the operation. The addressed partition automatically switches to Read Status Register mode.
	Block Erase	0020h/00D0h	Issuing this command sequence erases the addressed block. The addressed partition automatically switches to Read Status mode.
	Program/Erase Suspend	00B0h	Issuing this command to any device address *initiates* a suspend of a program or block-erase operation already in progress. SR6 = 1 indicates erase suspend, and SR2 = 1 indicates program suspend.
	Program/Erase Resume	00D0h	Issuing this command to any device address resumes a suspended program or block-erase operation. A program suspend nested within an erase suspend is resumed first.
	Blank Check	00BCh/00D0h	This command sequence initiates the blank check operation on a block.
Security	Lock Block	0060h/0001h	Issuing this command sequence sets the lock bit of the addressed block.
	Unlock Block	0060h/00D0h	Issuing this command sequence clears the lock bit of the addressed block.
	Lock Down Block	0060h/002Fh	Issuing this command sequence locks down the addressed block.

11.0 Flow Charts

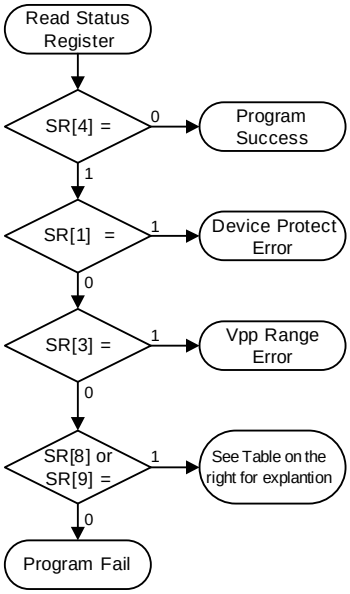
Figure 52: Word Program for Main Array Flowchart

WORD PROGRAM PROCEDURE



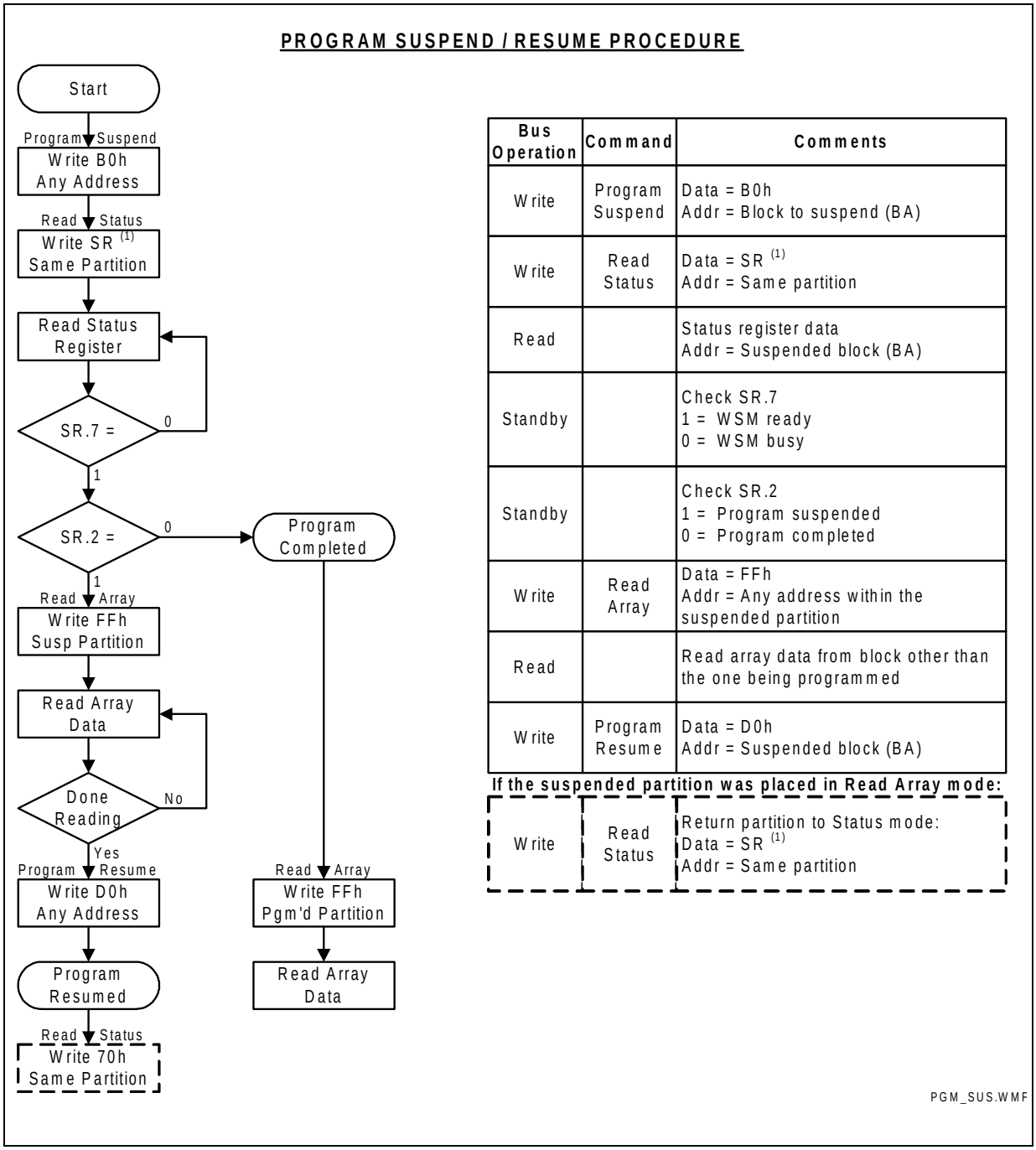
Bus Operation	Command	Comments
Write	Program Setup	Data = 0x41 Addr = Location to program
Write	Data	Data = Data to program Addr = Location to program
Read	None	Main or Parameter status register data
Idle	None	Check SR[7] 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent Word Program operations. Full Status Register check can be done after each program, or after a sequence of program operations. Write 0xFF after the last operation to set to the Read Array state.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Idle	None	Check SR[4]: 1 = Data Program Error
Idle	None	Check SR[1]: 1 = Block locked; operation aborted
Idle	None	Check SR[3]: 1 = V_{PP} Error
Idle	None	Check SR[8] AND SR[9]: 00 = Region program successful 10 = Attempted write with object data to Control Mode region 01 = Attempted rewrite to Object Mode region 11 = Attempted write using illegal command.
SR[3] MUST be cleared before the Write State Machine will allow further program attempts. If an error is detected, clear the Status Register before continuing operations - only the Clear Staus Register command clears the Status Register error bits		

Figure 53: Program Suspend/Resume Flowchart

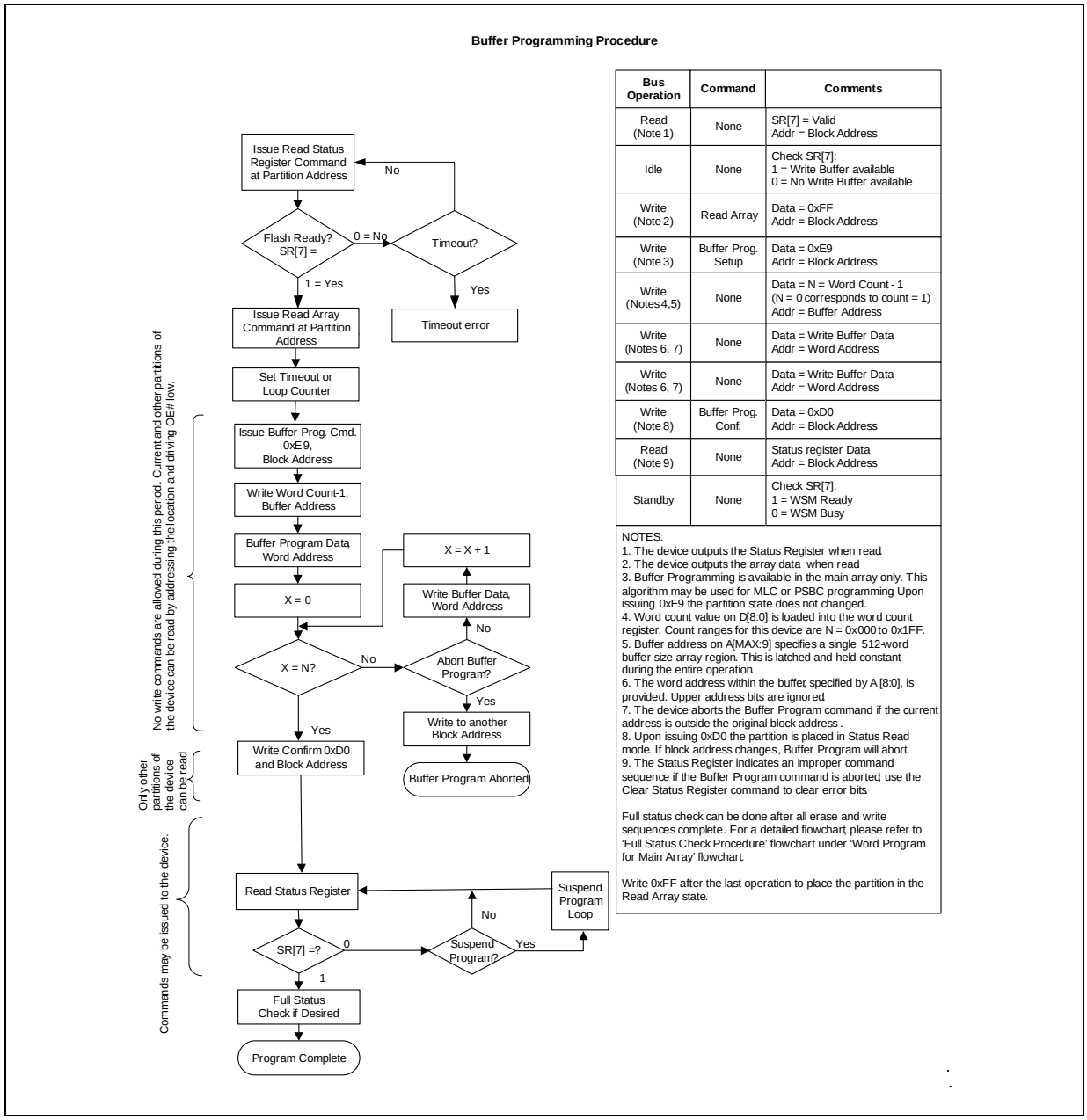


Bus Operation	Command	Comments
Write	Program Suspend	Data = B0h Addr = Block to suspend (BA)
Write	Read Status	Data = SR (1) Addr = Same partition
Read		Status register data Addr = Suspended block (BA)
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FFh Addr = Any address within the suspended partition
Read		Read array data from block other than the one being programmed
Write	Program Resume	Data = D0h Addr = Suspended block (BA)

If the suspended partition was placed in Read Array mode:

Write	Read Status	Return partition to Status mode: Data = SR (1) Addr = Same partition

Figure 54: Buffered Program Flowchart



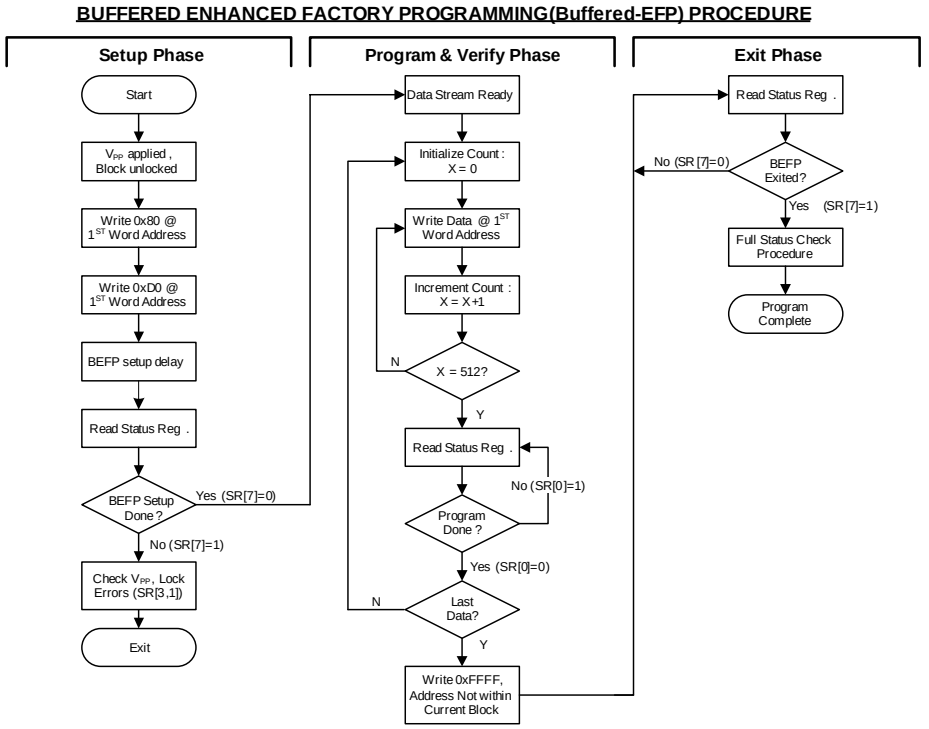
Bus Operation	Command	Comments
Read (Note 1)	None	SR[7] = Valid Addr = Block Address
Idle	None	Check SR[7]: 1 = Write Buffer available 0 = No Write Buffer available
Write (Note 2)	Read Array	Data = 0xFF Addr = Block Address
Write (Note 3)	Buffer Prog. Setup	Data = 0xE9 Addr = Block Address
Write (Notes 4,5)	None	Data = N = Word Count - 1 (N = 0 corresponds to count = 1) Addr = Buffer Address
Write (Notes 6, 7)	None	Data = Write Buffer Data Addr = Word Address
Write (Notes 6, 7)	None	Data = Write Buffer Data Addr = Word Address
Write (Note 8)	Buffer Prog. Conf.	Data = 0xD0 Addr = Block Address
Read (Note 9)	None	Status register Data Addr = Block Address
Standby	None	Check SR[7]: 1 = WSM Ready 0 = WSM Busy

NOTES:
1. The device outputs the Status Register when read.
2. The device outputs the array data when read.
3. Buffer Programming is available in the main array only. This algorithm may be used for MLC or PSBC programming. Upon issuing 0xE9 the partition state does not changed.
4. Word count value on D[8:0] is loaded into the word count register. Count ranges for this device are N = 0x000 to 0x1FF.
5. Buffer address on A[MAX:9] specifies a single 512-word buffer-size array region. This is latched and held constant during the entire operation.
6. The word address within the buffer, specified by A [8:0], is provided. Upper address bits are ignored.
7. The device aborts the Buffer Program command if the current address is outside the original block address .
8. Upon issuing 0xD0 the partition is placed in Status Read mode. If block address changes, Buffer Program will abort.
9. The Status Register indicates an improper command sequence if the Buffer Program command is aborted, use the Clear Status Register command to clear error bits.

Full status check can be done after all erase and write sequences complete. For a detailed flowchart, please refer to 'Full Status Check Procedure' flowchart under 'Word Program for Main Array' flowchart.

Write 0xFF after the last operation to place the partition in the Read Array state.

Figure 55: Buffered EFP Flowchart



BEFP Setup

Bus State	Operation	Comments
Write	Unlock Block	V_{PPH} applied to VPP
Write (Note 2)	BEFP Setup	Data = 0x80 @ 1ST Word Address
Write	BEFP Confirm	Data = 0xD0 @ 1ST Word Address
Read	Status Register	Data = Status Reg . Data Address = 1ST Word Addr
Standby	BEFP Setup Done ?	Check SR [7]: 0 = BEFP Ready 1 = BEFP Not Ready
Standby	Error Condition Check	If SR[7] is set, check: SR[3] set = V_{PP} Error SR[1] set = Locked Block

BEFP Program & Verify

Bus State	Operation	Comments
Read	Status Register	Data = Status Register Data Address = 1ST Word Addr.
Standby	Data Stream Ready ?	Check SR [0]: 0 = Ready for Data 1 = Not Ready for Data
Standby	Initialize Count	X = 0
Write (Note 3)	Load Buffer	Data = Data to Program Address = 1ST Word Addr.
Standby	Increment Count	X = X+1
Standby	Buffer Full?	X = 512 ? Yes = Read SR [0] No = Load Next Data Word
Read	Status Register	Data = Status Reg . data Address = 1ST Word Addr.
Standby	Program Done?	Check SR [0]: 0 = Program Done 1 = Program in Progress
Standby	Last Data?	No = Fill buffer again Yes = Exit
Write	Exit Prog & Verify Phase	Data = 0xFFFF @ address not in current block

BEFP Exit

Bus State	Operation	Comments
Read	Status Register	Data = Status Reg . Data Address = 1ST Word Addr
Standby	Check Exit Status	Check SR [7]: 0 = Exit Not Completed 1 = Exit Completed

Repeat for subsequent blocks ;

After BEFP exit , a full Status Register check can determine if any program error occurred ;

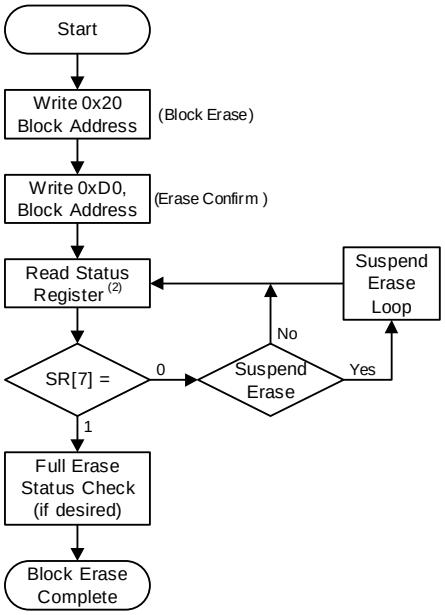
See full Status Register check procedure in the Word Program flowchart .

Write 0xFF to enter Read Array state .

NOTES:
1. BEFP is available in the main array only .
2. First-word address to be programmed within the target block must be aligned on a write -buffer boundary .
3. Write-buffer contents are programmed sequentially to the flash array starting at the first word address ; WSM internally increments addressing .

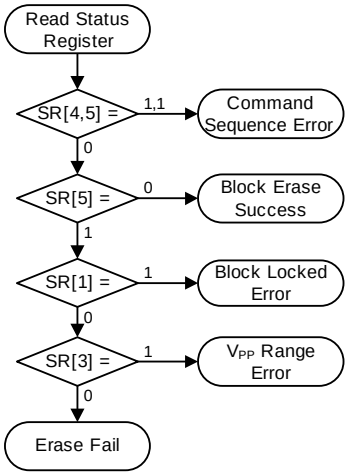
Figure 56: Block Erase for Main Array Flowchart

BLOCK ERASE PROCEDURE



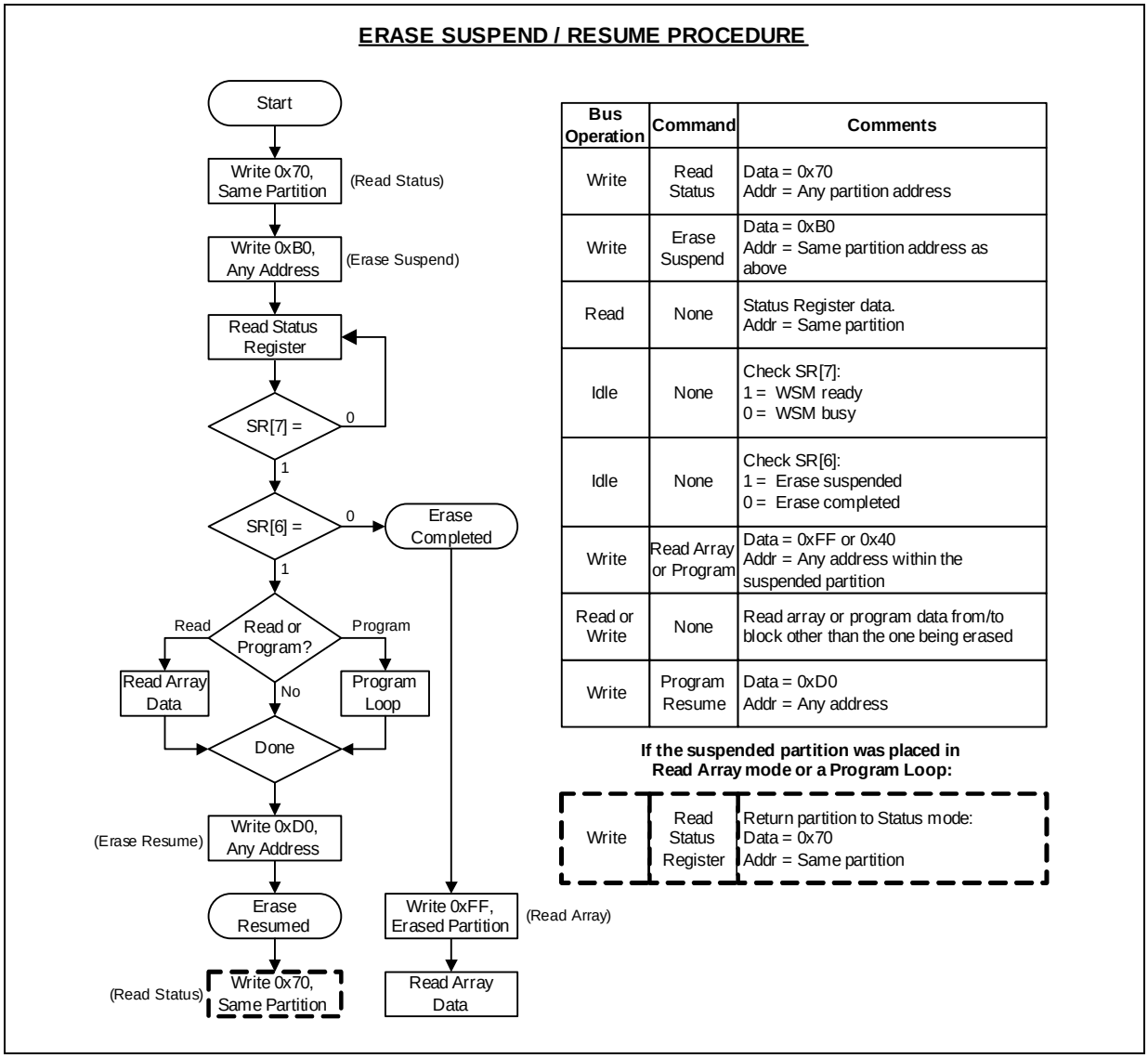
Bus Operation	Command	Comments
Write	Block Erase Setup	Data = 0x20 Addr = Block to be erased (BA)
Write	Erase Confirm	Data = 0xD0 Addr = Block to be erased (BA)
Read	None	Status Register data
Idle	None	Check SR[7]: 1 = WSM ready 0 = WSM busy
Repeat for subsequent block erasures. Full Status register check can be done after each block erase or after a sequence of block erasures. Write 0xFF after the last operation to enter read array mode		

FULL ERASE STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Idle	None	Check SR[4,5]: Both 1 = Command Sequence Error
Idle	None	Check SR[5]: 1 = Block Erase Error
Idle	None	Check SR[1]: 1 = Attempted erase of locked block; erase aborted.
Idle	None	Check SR[3]: 1 = V_{PP} Range Error
SR[1,3] must be cleared before the Write State Machine will allow further erase attempts. Only the Clear Status Register command clears SR[1, 3, 4, 5]. If an error is detected, clear the Status register before attempting an erase retry or other error recovery.		

Figure 57: Erase Suspend/Resume Flowchart

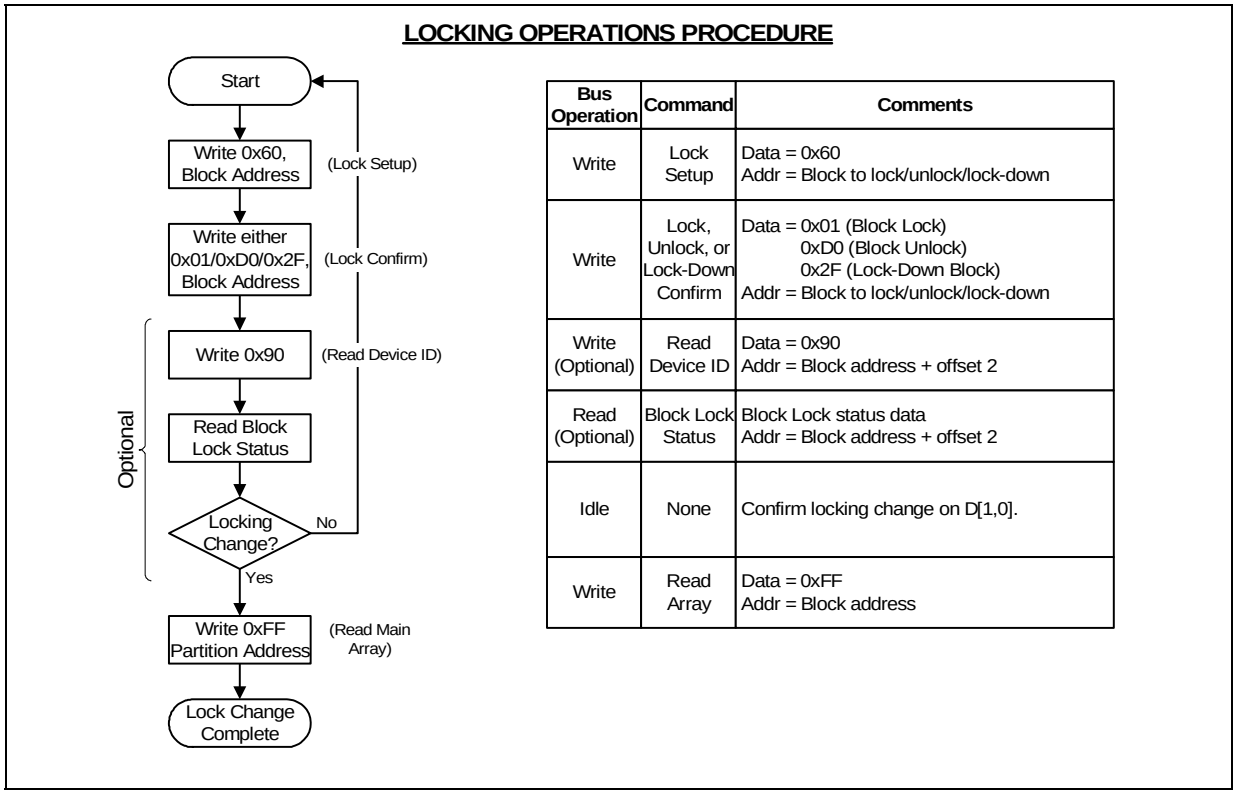


Bus Operation	Command	Comments
Write	Read Status	Data = 0x70 Addr = Any partition address
Write	Erase Suspend	Data = 0xB0 Addr = Same partition address as above
Read	None	Status Register data. Addr = Same partition
Idle	None	Check SR[7]: 1 = WSM ready 0 = WSM busy
Idle	None	Check SR[6]: 1 = Erase suspended 0 = Erase completed
Write	Read Array or Program	Data = 0xFF or 0x40 Addr = Any address within the suspended partition
Read or Write	None	Read array or program data from/to block other than the one being erased
Write	Program Resume	Data = 0xD0 Addr = Any address

If the suspended partition was placed in Read Array mode or a Program Loop:

Write	Read Status Register	Return partition to Status mode: Data = 0x70 Addr = Same partition

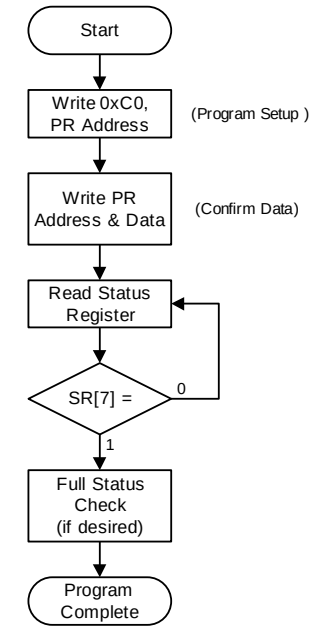
Figure 58: Main Array Block Lock Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 0x60 Addr = Block to lock/unlock/lock-down
Write	Lock, Unlock, or Lock-Down Confirm	Data = 0x01 (Block Lock) 0xD0 (Block Unlock) 0x2F (Lock-Down Block) Addr = Block to lock/unlock/lock-down
Write (Optional)	Read Device ID	Data = 0x90 Addr = Block address + offset 2
Read (Optional)	Block Lock Status	Block Lock status data Addr = Block address + offset 2
Idle	None	Confirm locking change on D[1,0].
Write	Read Array	Data = 0xFF Addr = Block address

Figure 59: Protection Register Programming Flowchart

PROTECTION REGISTER PROGRAMMING PROCEDURE



Bus Operation	Command	Comments
Write	Program PR Setup	Data = 0xC0 Addr = First Location to Program
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read	None	Status Register Data
Idle	None	Check SR[7]: 1 = WSM Ready 0 = WSM Busy

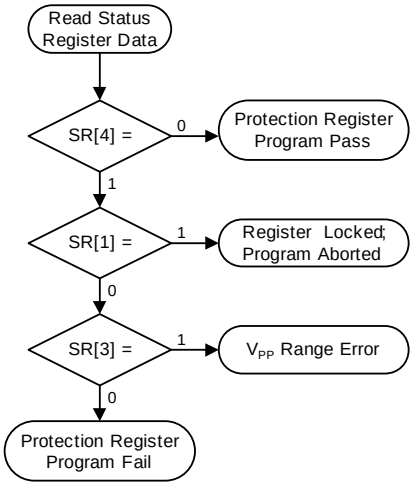
Program Protection Register operation addresses must be within the Protection Register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full Status Register check can be done after each program, or after a sequence of program operations.

Write 0xFF after the last operation to set Read Array state

FULL STATUS CHECK PROCEDURE



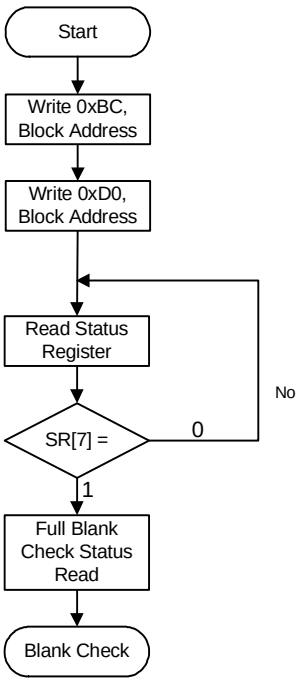
Bus Operation	Command	Comments
Idle	None	Check SR[4]: 1 = Programming Error
Idle	None	Check SR[1]: 1 = Block locked; operation aborted
Idle	None	Check SR[3]: 1 = V_{PP} Range Error

SR[3] must be cleared before the Write State Machine will allow further program attempts.

Only the Clear Staus Register command clears SR[1, 3, 4].

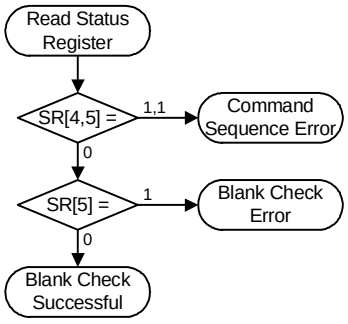
If an error is detected, clear the Status register before attempting a program retry or other error recovery.

Figure 60: Blank Check Operation Flowchart



BLANK CHECK PROCEDURE

Bus Operation	Command	Comments
Write	Blank Check Setup	Data = 0xBC Addr = Block to be read (BA)
Write	Blank Check Confirm	Data = 0xD0 Addr = Block to be read (BA)
Read	None	Status Register data.
Idle	None	Check SR[7]: 1 = WSM ready 0 = WSM busy
Repeat for subsequent block Blank Check. Full Status register check should be read after Blank Check has been performed on each block.		



FULL BLANK CHECK STATUS CHECK PROCEDURE

Bus Operation	Command	Comments
Idle	None	Check SR[4,5]: Both 1 = Command Sequence Error
Idle	None	Check SR[5]: 1 = Blank Check Error
SR[1,3] must be cleared before the Write State Machine will allow Blank Check to be performed. Only the Clear Status Register command clears SR[1, 3, 4, 5]. If an error is detected, clear the Status register before attempting a Blank Check retry or other error recovery.		

12.0 Common Flash Interface

The Common Flash Interface (CFI) is part of an overall specification for multiple command-set and control-interface descriptions. It describes the database structure containing the data returned by a read operation after issuing the CFI Query command. System software can parse this database structure to obtain information about the flash device, such as block size, density, bus width, and electrical specifications. The system software will then know which command set(s) to use to properly perform flash writes, block erases, reads and otherwise control the flash device.

12.1 Query Structure Output

The Query database allows system software to obtain information for controlling the flash device. This section describes the device's CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (A/DQ_{7-0}) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two Query-structure bytes, ASCII "Q" and "R," appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes. The device outputs ASCII "Q" in the low byte (A/DQ_{7-0}) and 00h in the high byte (A/DQ_{15-8}).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table 49: Summary of Query Structure Output as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII
Device Addresses	00010:	51	"Q"
	00011:	52	"R"

Table 50: Example of Query Structure Output of x16 Devices (Sheet 1 of 2)

Word Addressing			Byte Addressing		
Offset	Hex Code	Value	Offset	Hex Code	Value
A_X - A_0	A_{15} - A_0		A_X - A_0	A_7 - A_0	
00010h	0051	"Q"	00010h	0051	"Q"
00011h	0052	"R"	00011h	0052	"R"
00012h	0059	"Y"	00012h	0059	"Y"
00013h	P_ID_{LO}	PrVendor	00013h	P_ID_{LO}	PrVendor
00014h	P_ID_{HI}	ID#	00014h	P_ID_{LO}	ID#

Table 50: Example of Query Structure Output of x16 Devices (Sheet 2 of 2)

Word Addressing			Byte Addressing		
Offset	**Hex Code**	**Value**	**Offset**	**Hex Code**	**Value**
A_X - A_0	**A_{15} - A_0**		**A_X - A_0**	**A_7 - A_0**	
00015h	P_{LO}	PrVendor	00015h	P_ID_{HI}	ID#
00016h	P_{HI}	TblAdr	00016h		
00017h	A_ID_{LO}	AltVendor	00017h		
00018h	A_ID_{HI}	ID#	00018h		

12.2 Block Status Register

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR[1]) allows system software to determine the success of the last block erase operation. BSR[1] can be used just after power-up to verify that the VCC supply was not accidentally removed during an erase operation. Only issuing another operation to the block resets this bit. The Block Status Register is accessed from word address 02h within each block.

Table 51: Block Status Register

Offset	Length	Description	Address	Value
(BA + 2)h	1	Block Lock Status Register	BA + 2	-00 or -01
(BA + 2)h	1	BSR.0 Block Lock Status: 0 = Unlocked 1 = Locked	BA + 2	(bit 0): 0 or 1
(BA + 2)h	1	BSR.1 Block Lock Down Status: 0 = Not Locked Down 1 = Locked Down	BA + 2	(bit 0): 0 or 1
(BA + 2)h	1	BSR.2-3, 6-7: Reserved for future use	BA + 2	(bit 0): 0 or 1
Note: BA = The beginning of a Block Address; that is, 020000h is the beginning location in word mode of the 256-KB block 1.				

12.3 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 52: CFI Identification (Sheet 1 of 2)

Offset	Length	Description	Address	Hex Code	Value
10h	3	Query unique ASCII string “QRY”	10	--51	“Q”
			11	--52	“R”
			12	--59	“Y”

Table 52: CFI Identification (Sheet 2 of 2)

Offset	Length	Description	Address	Hex Code	Value
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms.	13	--00	
			14	--02	
15h	2	Extended Query Table primary algorithm address.	15	--0A	
			16	--01	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists.	17	--00	
			18	--00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists.	19	--00	
			1A	--00	

Table 53: System Interface Information (Sheet 1 of 2)

Offset	Length	Description	Address	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage. bits 0-3 BCD 100 mV bits 4-7 BCD volts	1B	--17	1.7 V
1Ch	1	V_{CC} logic supply maximum program/erase voltage. bits 0-3 BCD 100 mV bits 4-7 BCD volts	1C	--20	2.0 V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage. bits 0-3 BCD 100 mV bits 4-7 hex volts	1D	--85	8.5 V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage. bits 0-3 BCD 100 mV bits 4-7 hex volts	1E	--95	9.5 V
1Fh	1	"n" such that typical single word program timeout = 2^n µs.	1F	--06	64 µs
20h	1	"n" such that typical full buffer write timeout = 2^n µs.	20	--0B (256, 512 Mbit - 90 nm; 1024 Mbit - 65 nm) --0A (128. 256, 512 Mbit - 65 nm)	2048 µs (256, 512 Mbit - 90 nm; 1024 Mbit - 65 nm) 1024 µs (128. 256, 512 Mbit - 65 nm)
21h	1	"n" such that typical block erase timeout = 2^n ms.	21	--0A	1 s
22h	1	"n" such that typical full chip erase timeout = 2^n ms.	22	--00	NA
23h	1	"n" such that maximum word program timeout = 2^n times typical.	23	--02	256 µs

Table 53: System Interface Information (Sheet 2 of 2)

Offset	Length	Description	Address	Hex Code	Value
24h	1	"n" such that maximum buffer write timeout = 2^n times typical.	24	--02 (256, 512 Mbit - 90 nm; 128, 256, 512 Mbit - 65 nm) --01 (1024 Mbit - 65 nm)	8192 µs (256, 512 Mbit - 90 nm; 128, 256, 512 Mbit - 65 nm) 4096 µs (1024 Mbit - 65 nm)
25h	1	"n" such that maximum block erase timeout = 2^n times typical.	25	--02	4 s
26h	1	"n" such that maximum chip erase timeout = 2^n times typical.	26	--00	NA

12.4 Device Geometry Definition

Table 54: Device Geometry Definition

Offset	Length	Description	Address	Hex Code	Value
27h	1	*n* such that device size in bytes = 2^n.	27:		
		Flash device interface code assignment: *n* such that *n* + 1 specifies the bit field that represents the flash device width capabilities as described here: 7 6 5 4 3 2 1 0	Table 55, "Device Geometry Definition: Addr, Hex Code, Value" on page 114		
28h	2	— — — — x64 x32 x16 x8	28:	--01	x16
		15 14 13 12 11 10 9 8			
		— — — — — — — —	29:	--00	
2Ah	2	*n* such that maximum number of bytes in write buffer = 2^n.	2A: 2B:	--0A --00	1024
2Ch	1	Number of erase block regions (x) within the device: 1) x = 0 means no erase blocking; the device erases in bulk. 2) x specifies the number of device regions with one or more contiguous, same-size erase blocks. 3) Symmetrically blocked partitions have one blocking region.	2C:	Table 55, "Device Geometry Definition: Addr, Hex Code, Value" on page 114	
2Dh	4	Erase block region 1 information: bits 0 - 15 = y, y + 1 = number of identical-size erase blocks. bits 16 - 31 = z, region erase block(s) size are z x 256 bytes.	2D: 2E: 2F: 30:		
31h	4	Reserved for future erase block region information.	31: 32: 33: 34:		
35h	4	Reserved for future erase block region information.	35: 36: 37: 38:		

Table 55: Device Geometry Definition: Addr, Hex Code, Value

Address	128 Mbit		256 Mbit		512 Mbit		1 Gbit	
	B	T	B	T	B	T	B	T
27	18	—	19	—	1A	—	1B	—
28	01	—	01	—	01	—	01	—
29	00	—	00	—	00	—	00	—
2A	0A	—	0A	—	0A	—	0A	—
2B	00	—	00	—	00	—	00	—
2C	01	—	01	—	01	—	01	—
2D	3F	—	7F	—	FF	—	FF	—
2E	00	—	00	—	00	—	01	—
2F	00	—	00	—	00	—	00	—
30	04	—	04	—	04	—	04	—

12.5 Numonyx-Specific Extended Query Table

Table 56: Primary Vendor-Specific Extended Query (Sheet 1 of 2)

Offset P = 10Ah	Length	Description (Optional flash features and commands	Address	Hex Code	Value
(P+0)h	3	Primary extended query table. Unique ASCII string *PRI*	10A:	--50	P
(P+1)h			10B:	--52	R
(P+2)h			10C:	--49	I
(P+3)h	1	Major version number, ASCII	10D:	--31	1
(P+4)h	1	Minor version number, ASCII	10E:	--34	4

Table 56: Primary Vendor-Specific Extended Query (Sheet 2 of 2)

Offset P = 10Ah	Length	Description (Optional flash features and commands	Address	Hex Code	Value
(P+5)h (P+6)h (P+7)h (P+8)h	4	Optional feature and command support: (1 = yes; 0 = no) Bits 10 - 31 are reserved; undefined bits are 0. If the value in bit 31 is 1, an additional 31 bit field of optional features follows the bit 30 field.	10F: 110: 111: 112:	--E6 (Non-Mux) --66 (A/D Mux) --07 --00 --00	
		Bit 0: Chip erase supported.	Bit 0 = 0		No
		Bit 1: Suspend erase supported.	Bit 1 = 1		Yes
		Bit 2: Suspend program supported.	Bit 2 = 1		Yes
		Bit 3: Legacy lock/unlock supported.	Bit 3 = 0		No
		Bit 4: Queued erase supported.	Bit 4 = 0		No
		Bit 5: Instant individual block locking supported.	Bit 5 = 1		Yes
		Bit 6: OTP bits supported.	Bit 6 = 1		Yes
		Bit 7: Page mode read supported.	Bit 7 = 0		No: A/D Mux Yes: Non-Mux
		Bit 8: Synchronous read supported.	Bit 8 = 1		Yes
		Bit 9: Simultaneous operations supported.	Bit 9 = 1		Yes
		Bit 30: CFI links to follow.	Bit 30 = 0		No
		Bit 31: Another *Optional Features* field to follow.	Bit 31 = 0		No
(P+9)h	1	Supported functions after Suspend: Read Array, Status, Query. Other supported options include: Bits 1 - 7: Reserved; undefined bits are 0.	113:	--01	
		Bit 0: Program supported after Erase Suspend.	Bit 0 = 1		Yes
(P+A)h	2	Block Lock Status Register mask: Bits 2 - 3 and 6 - 15 are reserved; undefined bits are 0.	114: 115:	--33 --00	
(P+B)h	2	Bit 0: Block Lock Bit Status register active.	Bit 0 = 1		Yes
	2	Bit 1: Block Lock Down bit Status active.	Bit 1 = 1		Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage: Bits 0 - 3: BCD value in 100 mV Bits 4 - 7: BCD value in volts	116:	--18	1.8 V
(P+D)h	1	V_{PP} optimum program/erase supply voltage: Bits 0 - 3: BCD value in 100 mV Bits 4 - 7: Hex value in volts	117:	--90	9.0 V

Table 57: One Time Programmable (OTP) Register Information

Offset P = 10Ah	Length	Description	Address	Hex Code	Value
(P+E)h	1	Number of OTP register fields in JEDEC ID space. 00h indicates that 256 OTP fields are available.	118:	--02	2
(P+F)h (P+10)h (P+11)h (P+12)h	4	OTP Field 1: OTP Description: This field describes user available OTP register bytes. Some are preprogrammed with device-unique serial numbers. Others are user programmable. Bits 0 - 15 point to the OTP register Lock byte, the register's first byte. The following bytes are factory preprogrammed and user-programmable:			
		Bits 0 - 7 = Lock/bytes JEDEC plane physical low address.	119:	--80	80h
		Bits 8 - 15 = Lock/bytes JEDEC plane physical high address.	11A:	--00	00h
		Bits 16 - 23 = *n* where 2^n equals factory preprogrammed bytes.	11B:	--03	8 byte
		Bits 24 - 31 = *n* where 2^n equals user programmable bytes.	11C:	--03	8 byte
(P+13)h (P+14)h (P+15)h (P+16)h (P+17)h (P+18)h (P+19)h (P+1A)h (P+1B)h (P+1C)h	10	OTP Field 2: OTP Description			
		Bits 0 - 31 point to the OTP register physical Lock word address in the JEDEC plane.	11D: 11E: 11F: 120:	--89 --00 --00 --00	89h 00h 00h 00h
		The following bytes are factory or user programmable:			
		Bits 32 - 39 = *n* where *n* equals factory programmed groups (low byte). Bits 40 - 47 = *n* where *n* equals factory programmed groups (high byte). Bits 48 - 55 = *n* where 2*n* equals factory programmed bytes/ groups.	121: 122: 123:	--00 --00 --00	0 0 0
		Bits 56 - 63 = *n* where *n* equals user programmed groups (low byte). Bits 64 - 71 = *n* where *n* equals user programmed groups (high byte). Bits 72 - 79 = *n* where *n* equals user programmable bytes/ groups.	124: 125: 126:	--10 --00 --04	16 0 16

Table 58: Burst Read Information

Offset P = 10Ah	Length	Description (Optional flash features and commands)	Address	Hex Code	Value
(P+1D)h	1	Page Mode Read capability: Bits 0 - 7 = n where 2n hex value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	127:	--05 (Non Mux) --00 (A/D Mux	32-byte (Non Mux) 0 (AD Mux)
(P+1E)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	128:	--03	3
(P+1F)h	1	Synchronous mode read capability configuration 1: Bits 3 - 7 = Reserved. Bits 0 - 2 = *n* where 2^{n+1} hex value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This fields's 3-bit value can be written directly to the Read Configuration Register bits 0 - 2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	129:	--02	8
(P+20)h	1	Synchronous mode read capability configuration 2.	12A:	--03	16
(P+21)h	1	Synchronous mode read capability configuration 3.	12B:	--07	Cont

Table 59: Partition and Erase Block Information—Region 1 (Sheet 1 of 2)

Offset P = 10Ah		Description (Optional flash features and commands)	Length	Address	
Bottom	Top			Bottom	Top
(P+22)h	(P+22)h	Number of device hardware partition regions with the device: x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	12C:	12C:
Partition Region 1 Information					
(P+23)h	(P+23)h	Data size of this Partition Region information field: (number of addressable locations, including this field.	2	12D:	12D:
(P+24)h	(P+24)h			12E:	12E:
(P+25)h	(P+25)h	Number of identical partitions within the partition region.	1	12F:	12F:
(P+26)h	(P+26)h			130:	130:
(P+27)h	(P+27)h	Number of Program or Erase operations allowed in a partition: Bits 0 - 3 = Number of simultaneous Program operations. Bits 4 - 7 = Number of simultaneous Erase operations.	1	131:	131:
(P+28)h	(P+28)h	Number of Program or Erase operations allowed in other partitions while a partition in this region is in Program mode: Bits 0 - 3 = Number of simultaneous Program operations. Bits 4 - 7 = Number of simultaneous Erase operations.	1	132:	132:
(P+29)h	(P+29)h	Number of Program or Erase operations allowed in other partitions while a partition in this region is in Erase mode: Bits 0 - 3 = Number of simultaneous Program operations. Bits 4 - 7 = Number of simultaneous Erase operations.	1	133:	133:

Table 59: Partition and Erase Block Information—Region 1 (Sheet 2 of 2)

Offset P = 10Ah		Description (Optional flash features and commands)	Length	Address	
Bottom	Top			Bottom	Top
(P+2A)h	(P+2A)h	Types of erase block regions in this partition region: x = 0: No erase blocking; the partition region erases in bulk. x = Number of erase block regions with contiguous, same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks) x (Type 1 block sizes) + (Type 2 blocks) x (Type 2 block sizes) +...+ (Type n blocks) x (Type n block sizes).	1	134:	134:
(P+2B)h	(P+2B)h	Partition region 1 erase block type 1 information: Bits 0 - 15 = y, y + 1: Number of identical-sized erase blocks in a partition. Bits 16 - 30 = z, where region erase block(s) size is z x 256 bytes.	4	135:	135:
(P+2C)h	(P+2C)h			136:	136:
(P+2D)h	(P+2D)h			137:	137:
(P+2E)h	(P+2E)h			138:	138:
(P+2F)h	(P+2F)h	Partition 1 (Erase Block Type 1): Block erase cycles x 1000	2	139:	139:
(P+30)h	(P+30)h			13A:	13A:
(P+31)h	(P+31)h	Partition 1 (Erase Block Type 1) bits per cell; internal EDAC: Bits 0 - 3 = bits per cell in erase region Bit 4 = internal EDAC used (1=yes, 0=no) Bit 5 - 7 = reserved for future use	1	13B:	13B:
(P+32)h	(P+32)h	Partition 1 (Erase Block Type 1) page mode and synchronous mode capabilities: Bits 0 = page mode host reads permitted (1=yes, 0=no) Bit 1 = synchronous host reads permitted (1=yes, 0=no) Bit 2 = synchronous host writes permitted (1=yes, 0=no) Bit 3 - 7 = reserved for future use	1	13C:	13C:
(P+33)h	(P+33)h	Partition 1 (Erase Block Type 1) programming region information: Bits 0 - 7 = x, 2^x: programming region aligned size (bytes) Bit 8 - 14 = reserved for future use Bit 15 = legacy flash operation; ignore 0:7 Bit 16 - 23 = y: control mode valid size (bytes) Bit 24 - 31 = reserved for future use Bit 32 - 39 = z: control mode invalid size (bytes) Bit 40 - 46 = reserved for future use Bit 47 = legacy flash operation (ignore 23:16 and 39:32)	6	13D:	13D:
(P+34)h	(P+34)h			13E:	13E:
(P+35)h	(P+35)h			13F:	13F:
(P+36)h	(P+36)h			140:	140:
(P+37)h	(P+37)h			141:	141:
(P+38)h	(P+38)h			142:	142:

Table 60: Partition and Erase Block Region Information (Sheet 1 of 2)

Address	128 Mbit		256 Mbit		512 Mbit		1 Gbit	
	B	T	B	T	B	T	B	T
12C:	--01	—	--01	—	--01	—	--01	—
12D:	--16	—	--16	—	--16	—	--16	—
12E:	--00	—	--00	—	--00	—	--00	—
12F:	--08	—	--08	—	--08	—	--08	—
130:	--00	—	--00	—	--00	—	--00	—
131:	--11	—	--11	—	--11	—	--11	—
132:	--00	—	--00	—	--00	—	--00	—
133:	--00	—	--00	—	--00	—	--00	—

Table 60: Partition and Erase Block Region Information (Sheet 2 of 2)

Address	128 Mbit		256 Mbit		512 Mbit		1 Gbit	
	B	T	B	T	B	T	B	T
134:	--01	—	--01	—	--01	—	--01	—
135:	--07	—	--0F	—	--1F	—	--3F	—
136:	--00	—	--00	—	--00	—	--00	—
137:	--00	—	--00	—	--00	—	--00	—
138:	--04	—	--04	—	--04	—	--04	—
139:	--64	—	--64	—	--64	—	--64	—
13A:	--00	—	--00	—	--00	—	--00	—
13B:	--12	—	--12	—	--12	—	--12	—
13C:	--02 Mux --03 Non Mux	—	--02 Mux --03 Non Mux	—	--02 Mux --03 Non Mux	—	--02 Mux --03 Non Mux	—
13D:	--0A	—	--0A	—	--0A	—	--0A	—
13E:	--00	—	--00	—	--00	—	--00	—
13F:	--10	—	--10	—	--10	—	--10	—
140:	--00	—	--00	—	--00	—	--00	—
141:	--10	—	--10	—	--10	—	--10	—
142:	--00	—	--00	—	--00	—	--00	—

13.0 Next State

The Next State Table shows command inputs and the resulting next state of the chip. The Output Next State Table shows command inputs and the resulting output multiplexed next state of the chip.

Table 61: Next State Table (Sheet 1 of 7)

Current Chip State		Command Input and Resulting Chip Next State																		
		Array Read (3)	Word Pgm Setup (4,5,12)	BP Setup (13)	Erase Setup (4,5,12)	BEFP Setup (4,12)	Confirm (9)	Pgm/Ers Suspend	Read Status	Clear SR (6)	Read ID/Query	Lock/RCR/ECR Setup (5)	Blank Check (5)	OTP Setup (5)	Lock Blk Confirm (9)	Lock-down Blk Confirm (9)	Write ECR/RCR Confirm (9)	Block Address Change	Other Commands (2)	WSM Operation Completes
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xxh)	other	
Ready		Ready	Program Setup	BP Setup	Erase Setup	BEFP Setup	Ready					Lock/RCR/ECR Setup	BC Setup	OTP Setup	Ready			N/A	Ready	N/A
Lock/RCR/ECR Setup		Ready (Lock Error [Botch])					Ready (Unlock Block)	Ready (Lock Error [Botch])						Ready (Lock Error [Botch])	Ready (Lock Block)	Ready (Lock down Block)	Ready (Set CR)	N/A	Ready (Lock Error [Botch])	N/A
OTP	Setup	OTP Busy			OTP Busy													N/A	OTP Busy	N/A
	Busy	OTP Busy	IS in OTP Busy	OTP Busy	IS in OTP Busy	OTP Busy					Illegal State in OTP Busy		OTP Busy					N/A	OTP Busy	Ready
	IS in OTP Busy	OTP Busy			OTP Busy															

Table 61: Next State Table (Sheet 2 of 7)

Current Chip State		Command Input and Resulting Chip Next State																	
		Array Read (3)	Word Pgm Setup (4,5,12)	BP Setup (13)	Erase Setup (4,5,12)	BEFP Setup (4,12)	Confirm (9)	Pgm/Ers Suspend	Read Status	Clear SR (6)	Read ID/Query	Lock/RCR/ECR Setup (5)	Blank Check (5)	OTP Setup (5)	Lock Blk Confirm (9)	Lock-down Blk Confirm (9)	Write ECR/RCR Confirm (9)	Block Address Change	Other Commands (2)	WSM Operation Completes
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xxh)	other	
Word Program	Setup	Word Program Busy																N/A	Pgm Busy	N/A
	Busy	Pgm Busy	IS in Pgm Busy	Pgm Busy	IS in Pgm Busy	Pgm Busy	Pgm Susp	Word Pgm Busy			IS in Word Pgm Busy		Word Pgm Busy					N/A	Pgm Busy	Ready
	IS in Pgm Busy	Word Pgm Busy																		
	Suspend	Pgm Susp	IS in Pgm Susp	Pgm Susp end	IS in Pgm Susp	Pgm Busy	Pgm Susp			Pgm Susp (Erbits clear)	Word Pgm Susp	Illegal State in Pgm Suspend		Word Program Suspend				N/A	Word Pgm Susp	N/A
	IS in Pgm Suspend	Word Program Suspend																		

Table 61: Next State Table (Sheet 3 of 7)

Current Chip State		Command Input and Resulting Chip Next State																		
		Array Read (3)	Word Pgm Setup (4,5,12)	BP Setup (13)	Erase Setup (4,5,12)	BEFP Setup (4,12)	Confirm (9)	Pgm/Ers Suspend	Read Status	Clear SR (6)	Read ID/Query	Lock/RCR/ECR Setup (5)	Blank Check (5)	OTP Setup (5)	Lock Blk Confirm (9)	Lock-down Blk Confirm (9)	Write ECR/RCR Confirm (9)	Block Address Change	Other Commands (2)	WSM Operation Completes
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xxh)	other	
Buffer Program (BP)	Setup	BP Load 1																		N/A
	BP Load 1 (10)	BP Load 2 if word count >0, else BP confirm																		
	BP Load 2 (10)	BP Confirm if data load in program buffer is complete, ELSE BP load 2																Ready (Error [Botch])	BP Confirm if data load in program buffer is complete, else BP load 2	
	BP Confirm	Ready (Error [Botch])					BP Busy	Ready (Error [Botch])												
	BP Busy	BP Busy	IS in BP Busy	BP Busy	Illegal State in BP Busy		BP Busy	BP Susp	BP Busy			IS in BP Busy			BP Busy			BP Busy		Ready
	IS in BP Busy	BP Busy																		
	BP Suspend	BP Susp	IS in BP Susp	BP Suspend	Illegal State in BP Busy		BP Busy	BP Suspend		BP Susp (Erbits clear)	BP Susp	IS in BP Susp			BP Suspend			N/A	BP Susp	N/A
	IS in BP Suspend	BP Suspend																		

Table 61: Next State Table (Sheet 4 of 7)

Current Chip State		Command Input and Resulting Chip Next State																	WSM Operation Completes
		Array Read [3]	Word Pgm Setup [4,5,12]	BP Setup [13]	Erase Setup [4,5,12]	BEFP Setup [4,12]	Confirm [9]	Pgm/Ers Suspend	Read Status	Clear SR [6]	Read ID/Query	Lock/RCR/ECR Setup [5]	Blank Check [5]	OTP Setup [5]	Lock Blk Confirm [9]	Lock-down Blk Confirm [9]	Write ECR/RCR Confirm [9]	Block Address Change	Other Commands [2]	
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xxh)	other	
Erase	Setup	Ready (Error [Botch])					Erase Busy	Ready (Error [Botch])										N/A	Ready (Err Botch0])	N/A
	Busy	Erase Busy	IS in Erase Busy	Erase Busy	IS in Erase Busy		Erase Busy	Erase Susp	Erase Busy		IS in Erase Busy				Erase Busy			N/A	Erase Busy	Ready
	IS in Erase Busy	Erase Busy																		
	Suspend	Erase Susp	Word Pgm Setup in Erase Susp	BP Setup in Erase Susp	IS in Erase Suspend		Erase Busy	Erase Suspend	Erase Susp (Erbits clear)	Erase Susp	Lock/RCR/ECR Setup in Erase Susp	Erase Susp		IS in Erase Susp	Erase Suspend			N/A	Erase Susp	N/A
	IS in Erase Susp	Erase Suspend																		
Word Program in Erase Suspend	Setup	Word Pgm busy in Erase Suspend																N/A	Word Pgm Busy in Ers Suspend	N/A
	Busy	Word Pgm busy in Erase Susp	IS in Pgm busy in Ers Susp	Word Pgm busy in Erase Susp	IS in Word Pgm busy in Ers Susp		Word Pgm busy in Erase Susp	Word Pgm Susp in Ers Susp	Word Pgm busy in Erase Susp		IS in Word Pgm busy in Ers Susp				Word Pgm busy in Erase Susp					Erase Susp

Table 61: Next State Table (Sheet 5 of 7)

Current Chip State		Command Input and Resulting Chip Next State																	
		Array Read (3)	Word Pgm Setup (4,5,12)	BP Setup (13)	Erase Setup (4,5,12)	BEFP Setup (4,12)	Confirm (9)	Pgm/Ers Suspend	Read Status	Clear SR (6)	Read ID/Query	Lock/RCR/ECR Setup (5)	Blank Check (5)	OTP Setup (5)	Lock Blk Confirm (9)	Lock-down Blk Confirm (9)	Write ECR/RCR Confirm (9)	Block Address Change	Other Commands (2)	WSM Operation Completes
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xxh)	other	
Word Program in Erase Suspend	Illegal State (IS) in Pgm busy in Erase Suspend	Word Pgm busy in Erase Suspend																N/A	Word Pgm busy in Erase Suspend	IS in Erase Susp
	Suspend	Word Pgm susp in Erase Susp	iS in pgm susp in Erase Susp	Word Pgm susp in Erase Susp	IS in pgm susp in Erase Susp	Word Pgm busy in Erase Susp	Word Pgm susp in Erase Susp	Word Pgm Susp in Erase Susp	Word Pgm Susp in Erase Susp: Error bits clear	Word Pgm Susp in Erase Susp	IS in Word Pgm Susp in Erase Susp	Word Pgm Susp in Erase Susp							Word Pgm Susp in Erase Susp	N/A
	Illegal State in Word Program Suspend in Erase Suspend	Word Pgm Suspend in Erase Suspend																	Word PgmSuspend in Erase Suspend	

Table 61: Next State Table (Sheet 6 of 7)

Current Chip State		Command Input and Resulting Chip Next State																	
		Array Read (3)	Word Pgm Setup (4,5,12)	BP Setup (13)	Erase Setup (4,5,12)	BEFP Setup (4,12)	Confirm (9)	Pgm/Ers Suspend	Read Status	Clear SR (6)	Read ID/Query	Lock/RCR/ECR Setup (5)	Blank Check (5)	OTP Setup (5)	Lock Blk Confirm (9)	Lock-down Blk Confirm (9)	Write ECR/RCR Confirm (9)	Block Address Change	Other Commands (2)	WSM Operation Completes
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xxh)	other	
BP in Erase Suspend	Setup	BP Load 1																		N/A
	BP Load 1 (10)	BP Load 2 if word count >0, else BP confirm																		
	BP Load 2 (10)	BP Confirm if data load in program buffer is complete, ELSE BP load 2																Erase Susp: Error [Botch]	BP Confirm in Erase Suspend when count=0, ELSE BP load 2	
	BP Confirm	Erase Suspend (Error [BotchBP])					BP Busy in Ers Susp	Erase Susp: Error [Botch BP]												
	BP Busy	BP Busy in Erase Susp	IS in BP Busy in Erase Susp	BP Busy in Erase Susp	Illegal State in BP Busy in Erase Susp			BP Susp in Erase Susp	BP Busy in Erase Susp		IS in BP Busy in Erase Suspend		BP Busy in Erase Susp					N/A	BP Busy in Erase Susp	Erase Susp
	IS in BP Busy	BP Busy in Erase Suspend																		IS in Erase Susp
	BP Susp	BP Susp in Erase Susp	IS in BP Susp in Erase Susp	BP Susp in Erase Susp	Illegal State in BP Busy in Erase Susp		BP Busy in Erase Susp	BP Susp in Erase Susp		BP Susp in Erase Susp: Error bits clear	BP Susp in Erase Susp	IS in BP Busy in Erase Suspend			BP Susp in Erase Susp			N/A	BP Susp in Erase Susp	N/A

Table 61: Next State Table (Sheet 7 of 7)

Current Chip State		Command Input and Resulting Chip Next State																	
		Array Read (3)	Word Pgm Setup (4,5,12)	BP Setup (13)	Erase Setup (4,5,12)	BEFP Setup (4,12)	Confirm (9)	Pgm/Ers Suspend	Read Status	Clear SR (6)	Read ID/Query	Lock/RCR/ECR Setup (5)	Blank Check (5)	OTP Setup (5)	Lock Blk Confirm (9)	Lock-down Blk Confirm (9)	Write ECR/RCR Confirm (9)	Block Address Change	Other Commands (2)	WSM Operation Completes
		(FFh)	(41h)	(E9h)	(20h)	(80h)	(D0h)	(B0)	(70h)	(50h)	(90h, 98h)	(60h)	(BCh)	(C0h)	(01h)	(2Fh)	(03h, 04h)	(xh)	other	
Lock/RCR/ECR Setup in Erase Suspend		Erase Suspend: Lock Error [Botch]					Erase Susp: Un-lock Block	Erase Susp: Lock Error [Botch]						Erase Susp: Error [Botch]	Erase Susp Blk Lock	Erase Susp Blk Lk-Down	Erase Susp CR Set	N/A	Erase Susp: Error [Botch]	N/A
Blank Check (BC)	Setup	Ready (Error [Botch])					BC Busy	Ready: Error [Botch]										N/A	Ready: Error [Botch]	N/A
	Blank Check Busy	BC Busy	IS in BC Busy	BC Busy	IS in BC Busy		BC Busy				IS in BC Busy			BC Busy					BC Busy	Ready
	IS in Blank Check Busy	BC Busy																	BC Busy	
BEFP	Setup	Ready: Error [Botch]					BEFP Load Data	Ready: Error [Botch]												N/A
	BEFP Busy	BEFP Program and Verify Busy (if Block Address given matches address given on BEFP Setup command). Commands treated as data. (7)																Ready	BEFP Busy	Ready

Table 62: Output Next State Table

Current Chip State	Command Input to Chip and Resulting Output MUX Next State																		
	Array Read [3] (FFh)	Word Pgm Setup [4,5,12] (41h)	BP Setup [13] (E9h)	Generic Command Setup (EBh)	Erase Setup [4,5,12] (20h)	BEFP Setup [4,12] (80h)	Confirm [9] (D0h)	Pgm/Ers Suspend (B0)	Read Status (70h)	Clear SR [6] (50h)	Read ID/Query (90h, 98h)	Lock/RCR/ECR Setup [5] (60h)	Blank Check [5] (BCh)	OTP Setup [5] (C0h)	Lock Blk Confirm [9] (01h)	Lock-down Blk Confirm [9] (2Fh)	Write ECR/RCR Confirm [9] (03h, 04h)	Block Address Change	Other Commands [2] other	WSM Operation Completes
BEFPSetup, BEFP Pgm & Verify Busy, Erase Setup, OTP Setup, BP Confirm WordPgmSetup, Word Pgm Setup in Erase Susp, BP Confirm in Erase Suspend, Blank Check Setup, Blank Check Busy	Status Read																		Output MUX does not change
Lock/RCR/ECR Setup, Lock/RCR/ECR Setup in Erase Susp	Status Read																Array Read	Status Read	
BP Setup, Load 1, Load 2 BP Setup, Load1, Load 2 - in Erase Susp.	Output MUX will not change																		
BP Busy, BP Busy in Erase Suspend, Word Program Busy, Word Prgm Busy in Erase Suspend, Erase Busy	Array Read	Status Read	Status Read	Status Read	Output MUX does not change	Status Read	Output MUX does not Change	ID/Query Read	Status Read	Output MUX does not change							Array Read	Output MUX does not Change	
Ready, Word Prgm Suspend, BP Suspend, Phase-1 BP Suspend, Erase Suspend, BP Suspend in Erase Suspend			Output MUX does not Change																
OTP Busy			Status Read					SR Read											

Notes:

1. The *Partition Data When Read* field shows what users read from the flash chip after issuing the appropriate command, given the Partition Address is not changed from the address given during the command. Read-while-write functionality gives more flexibility in data output from the device. The data read from the chip depends on the Partition Address applied to the device. Depending on the command issued to the chip, each partition is placed into one of the following three output states during commands: Read Array, Read Status or Read ID/CFI. This partition's output state is retained until a

new command is issued to the chip at that Partition Address. This allows the user to set partition #1's output state to Read Array, and partition #4's output state to Read Status. Each time the partition address is changed to partition #4 (without issuing a new command), the Status will be read from the chip.

2. *Illegal commands* include commands outside of the allowed command set (allowed commands: 41H [pgm], 20H [erase], etc.)
3. All partitions default to Read Array on powerup.
4. If a Read Array is attempted from a busy partition, the result is unreliable data. When the user returns to this partition address later, the output mux will be in the "Read Array" state from its last visit. the Read ID and Read Query commands perform the same function in the device. The ID and Query data are located at different locations in the address map.
5. 1st and 2nd cycles of "2 cycles write commands" must be given to the same partition address, or unexpected results will occur.
6. The Clear Status command clears only the error bits in the status register if the device is not in the following modes: 1) WSM running (Pgm Busy, Erase Busy, Pgm Busy In Erase Suspend, OTP Busy, BEFP modes) 2) Suspend states (Erase Suspend, Pgm Suspend, Pgm Suspend In Erase Suspend).
7. BEFP writes are allowed only when the status register bit #0 = 0 or else the data is ignored.
8. The *current state* is that of the chip and not of the partition. Each partition *remembers* which output (Array, ID/CFI or Status) it was last pointed to on the last instruction to the chip, but the next state of the chip does not depend on where the partition's output mux is presently pointing to.
9. Confirm commands (Lock Block, Unlock Block, Lock-Down Block, Configuration Register and Blank Check) perform the operation and then move to the Ready State.
10. Buffered programming will botch when a different block address (as compared to address given with E9 command) is written during the BP Load1 and BP Load2 states.
11. WA0 refers to the block address latched during the first write cycle of the current operation.
12. All two cycle commands are considered as a contiguous whole during device suspend states. Individual commands are not parsed separately; that is, the 2nd cycle of an erase command issued in program suspend will NOT resume the program operation.
13. The Buffered Program setup command (0xE9) will not change the partition state. The Buffered Program Confirm command (0xD0) will place the partition in read status mode.

Appendix A AADM Mode

A.1 AADM Feature Overview

The following is a list of general requirements for AADM mode. Additional details can be found in subsequent sections.

- **Feature Availability:** AADM mode is available in devices that are configured as A/D MUX. With this configuration, AADM mode is enabled by setting a specific volatile bit in the RCR.
- **High Address Caputure (A[MAX:16]):** When AADM mode is enabled, A[MAX:16] and A[15:0] are captured from the A/DQ[15:0] balls. The selection of A[MAX:16] or A[15:0] is determined by the state of the OE# input, as A[MAX:16] is captured when OE# is at VIL.
- **Read & Write Cycle Support:** In AADM mode, both asynchronous and synchronous Cycles are supported.
- **Customer Requirements:** For AADM operation, the customer is required to ground A16-Amax.
- **Other Characteristics:** For AADM, all other device characteristics (pgm time, erase time, ICCS, etc.) are the same as A/D MUX unless otherwise stated.

A.2 AADM Mode Enable (RCR[4]=1)

Setting RCR.4 to its non-default state ('1b) enables AADM mode:

- The default device configuration upon Reset or Powerup is A/D MUX Mode
- Upon setting RCR[4]=1, the upper Addresses A[max:16] are latched as all 0's by default.

A.3 Bus Cycles and Address Capture

AADM bus operations have one or two address cycles. For two address cycles, the upper address (A[MAX:16]) must be issued first, followed by the lower address (A[15:0]). For bus operations with only one address cycle, only the lower address is issued. The upper address that applies is the one that was most recently latched on a previous bus cycle. For all read cycles, sensing begins when the lower address is latched, regardless of whether there are one or two address cycles.

In bus cycles, the external signal that distinguishes the upper address from the lower address is OE#. When OE# is at VIH, a lower address is captured; when OE# is at VIL, an upper address is captured.

When the bus cycle has only one address cycle, the timing waveform is similar to A/D MUX mode. The lower address is latched when OE# is at VIH, and data is subsequently outputted after the falling edge of OE#.

Note: When the device initially enters AADM mode, the upper address is internally latched as all 0's.

A.3.1 WAIT Behavior

The WAIT behavior in AADM mode functions the same as the legacy M18 non-MUX WAIT behavior (ADMux WAIT behavior is unique). In other words, WAIT will always be driven whenever DQ[15:0] is driven, and WAIT will tri-state whenever DQ[15:0] tri-state. In asynchronous mode (RCR[15] = '1b), WAIT always indicates "valid data" when driven. In synchronous mode (RCR[15] = '0b), WAIT indicates "valid data" only after the latency count has lapsed and the data output data is truly valid.

A.3.2 Asynchronous Read and Write Cycles

For asynchronous read and write cycles, ADV# must be toggled high-low-high a minimum of one time and a maximum of two times during a bus cycle. If ADV# is toggled low twice during a bus cycle, OE# must be held low for the first ADV# rising edge and OE# must be held high for the second ADV# rising edge. The first ADV# rising edge (with OE# low) captures A[MAX:16]. The second ADV# rising edge (with OE# high) captures A[15:0]. Each bus cycle must toggle ADV# high-low-high at least one time in order to capture A[15:0]. For asynchronous reads, sensing begins when the lower address is latched.

During asynchronous cycles, it is optional to capture A[MAX:16]. If these addresses are not captured, then the previously captured A[MAX:16] contents will be used.

A.3.2.1 Asynchronous Read Cycles

For asynchronous read and latching specifications, refer to Table 63, "AADM Aynchronous and Latching Timings" on page 130. For asynchronous read timing diagrams, refer to Figure 61, "AADM Asynchronous Read Cycle (Latching A[MAX:0])" on page 130 and Figure 62, "AADM Asynchronous Read Cycle (Latching A[15:0] only)" on page 131. For AADM, note that asynchronous read access is from the rising edge of ADV# rather than the falling edge. (i.e. TVHQV rather than TVLQV)

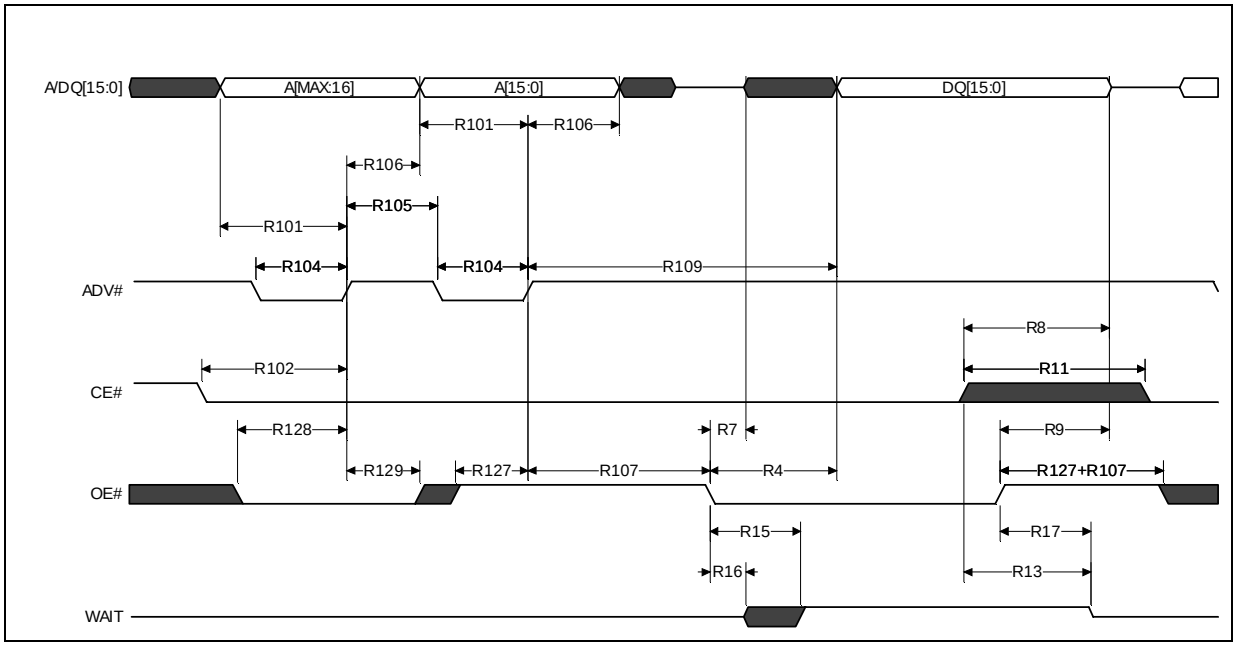
Table 63: AADM Aynchronous and Latching Timings

Num	Sym	Min (nS)	Max (nS)
R4	t_{GLQV}		20
R5	t_{PHQV}		150
R6	t_{ELQX}	0	
R7	t_{GLQX}	0	
R8	t_{EHQZ}		9
R9	t_{GHQZ}		9
R10	t_{OH}	0	
R11	t_{EHEL}	7	
R12	t_{ELTV}		11
R13	t_{EHTZ}		9
R15	t_{GLTV}		7
R16	t_{GLTX}	0	

Num	Sym	Min (nS)	Max (nS)
R17	t_{GHTZ}		9
R101	t_{AVVH}	5	
R102	t_{ELVH}	9	
R104	t_{VLVH}	7	
R105	t_{VHVL}	7	
R106	t_{VHAX}	5	
R107	t_{VHGL}	3	
R109	t_{VHQV}[1]		96
R111	t_{PHVH}	30	
R127	t_{GHVH}	3	
R128	t_{GLVH}	3	
R129	t_{VHGH}	3	

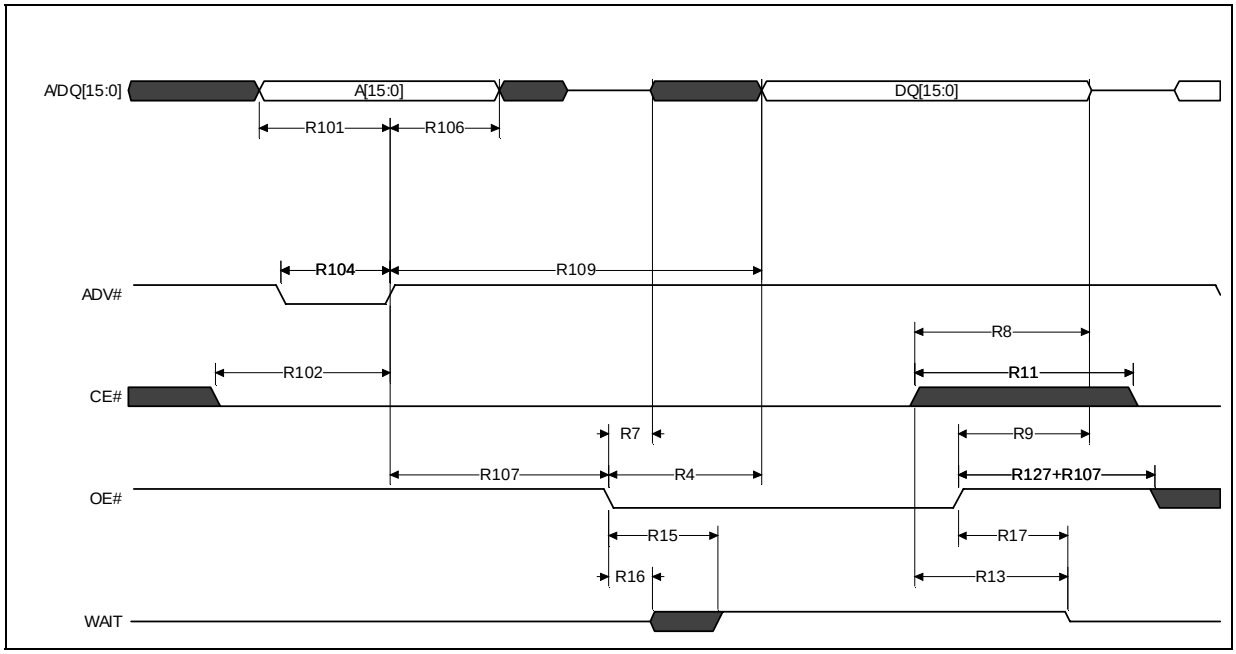
Notes:
1. TVHQV applies to asynchronous read access time.
2. A read cycle may be restarted prior to completing a pending read operation, but this may occur only once before the sense operation is allowed to complete.

Figure 61: AADM Asynchronous Read Cycle (Latching A[MAX:0])



Notes:
1. Diagram shows WAIT as active low (RCR.10=0)

Figure 62: AADM Asynchronous Read Cycle (Latching A[15:0] only)



Notes:
1. Diagram shows WAIT as active low (RCR.10=0).
2. Without latching A[MAX:16] in the Asynchronous Read Cycle, the previously latched A[MAX:16] applies.

A.3.2.2 Asynchronous Write Cycles

For asynchronous write specifications, refer to Table 64, “AADM Write Timings” on page 132. For asynchronous write timing diagrams, refer to Figure 63, “AADM Asynchronous Write Cycle (Latching A[MAX:0])” on page 132 and Figure 64, “AADM Asynchronous Write Cycle (Latching A[15:0] only)” on page 132.

Table 64: AADM Write Timings

Num	Symbol	Min(nS)
W1	t_{PHWL}	150
W2	t_{ELWL}	0
W3	t_{WLWH}	40
W4	t_{DVWH}	40
W6	t_{WHEH}	0
W7	t_{WHDX}	0

Num	Symbol	Min(nS)
W9	t_{WHWL}	20
W10	t_{VPWH}	200
W11	t_{WVVL}	0
W13	t_{BHWH}	200
W14	t_{WHGL}	0
W23	t_{GHWL}	0

Figure 63: AADM Asynchronous Write Cycle (Latching A[MAX:0])

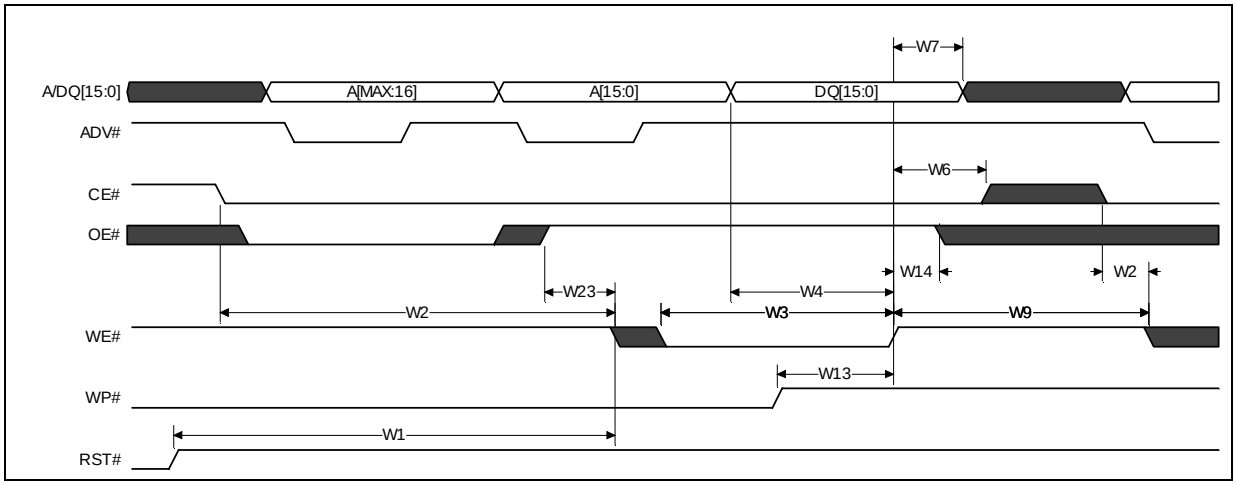
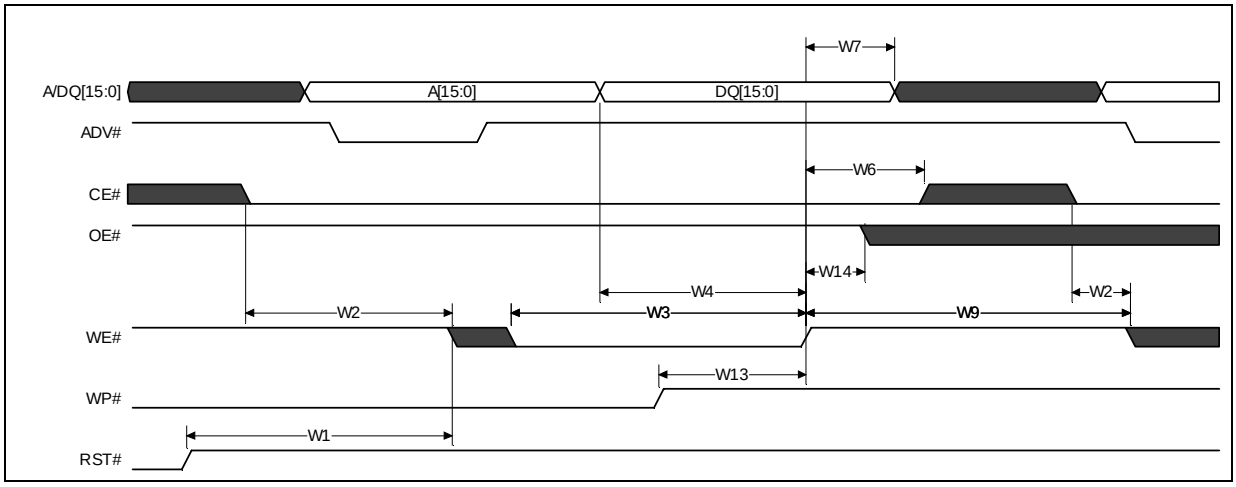


Figure 64: AADM Asynchronous Write Cycle (Latching A[15:0] only)



A.3.3 Synchronous Read and Write Cycles

Just as asynchronous bus cycles, synchronous bus cycles (RCR[15] = '0b) can have one or two address cycles. If the are two address cycles, the upper address must be latched first with OE# at VIL followed by the lower address with OE# at VIH. If there is only one address cycle, only the lower address will be latched and the previously latched upper address applies. For reads, sensing begins when the lower address is latched, but for synchronous reads, addresses are latched on a rising clock CLK instead of a rising ADV# edge.

For synchronous bus cycles with two address cycles, it is not necessary to de-assert ADV# between the two address cycles. This allows both the upper and lower address to be latched in only two clock periods.

A.3.3.1 Synchronous Read Cycles

For synchronous read specifications, refer to Table 65, "AADM Synchronous Timings" on page 133. For synchronous read timing diagrams, refer to the following:

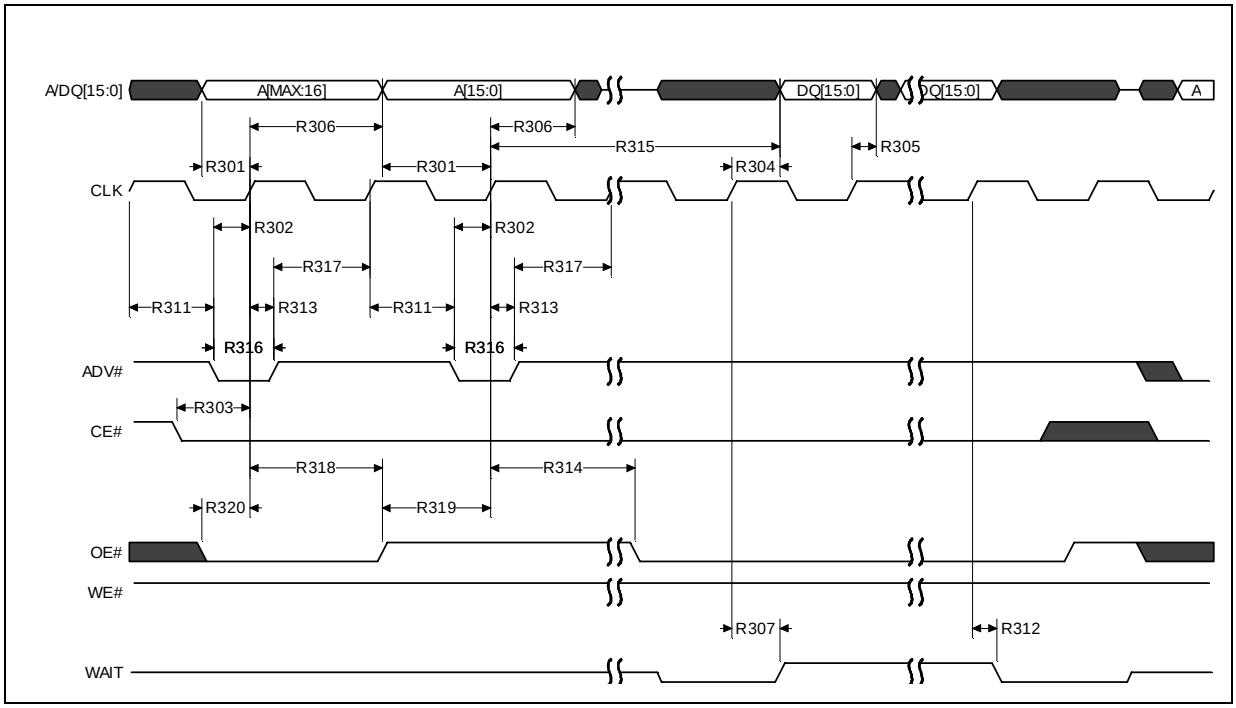
- Figure 65, "AADM Sync Burst Read Cycle (ADV# De-asserted between Address Cycles)" on page 134
- Figure 66, "AADM Sync Burst Read Cycle (ADV# Not De-asserted between Address Cycles)" on page 134
- Figure 67, "AADM Sync Burst Read Cycle (Latching A[15:0] only)" on page 135

Table 65: AADM Synchronous Timings

Num	Sym	Target (104 MHz) (108MHz)		Notes (3)	Num	Sym	Target (104 MHz) (108MHz)		Notes (3)
		Min (nS)	Max (nS)				Min (nS)	Max (nS)	
R201	t_{CLK}	9	See note	1	R311	t_{CHVL}	2.5		
R203	$t_{RISE/FALL}$		1.5	5	R312	t_{CHTX}	2		
R301	t_{AVCH}	3			R313	t_{CHVH}	2		2
R302	t_{VLCH}	3		2	R314	t_{CHGL}	2.5		4
R303	t_{ELCH}	3.5			R316	t_{VLVH}	t_{CLK}	$2*t_{CLK}$	
R304	t_{CHQV}		7		R317	t_{VHCH}	3		
R305	t_{CHQX}	2			R318	t_{CHGH}	2		
R306	t_{CHAX}	5		4	R319	t_{GHCH}	3		
R307	t_{CHTV}		7		R320	t_{GLCH}	3		

Notes:
1. The device must operate down to 9.6MHz in synchronous burst mode.
2. During the address capture phase of a read burst bus cycle, OE# timings relative to CLK shall be identical to those of ADV# relative to CLK.
3. In synchronous burst read cycles, the asynchronous OE# to ADV# setup and hold times must also be met (Tghvh & Tvhgl) to signify that the address capture phase of the bus cycle is complete.
4. To prevent A/D bus contention between the host and the memory device, OE# may only be asserted low after the host has satisfied the ADDR hold spec, Tchax.
5. Rise and fall time specified between Vil & Vih
6. A read cycle may only be terminated (prior to the completion of sensing data) one time before a full bus cycle must be allowed to complete.

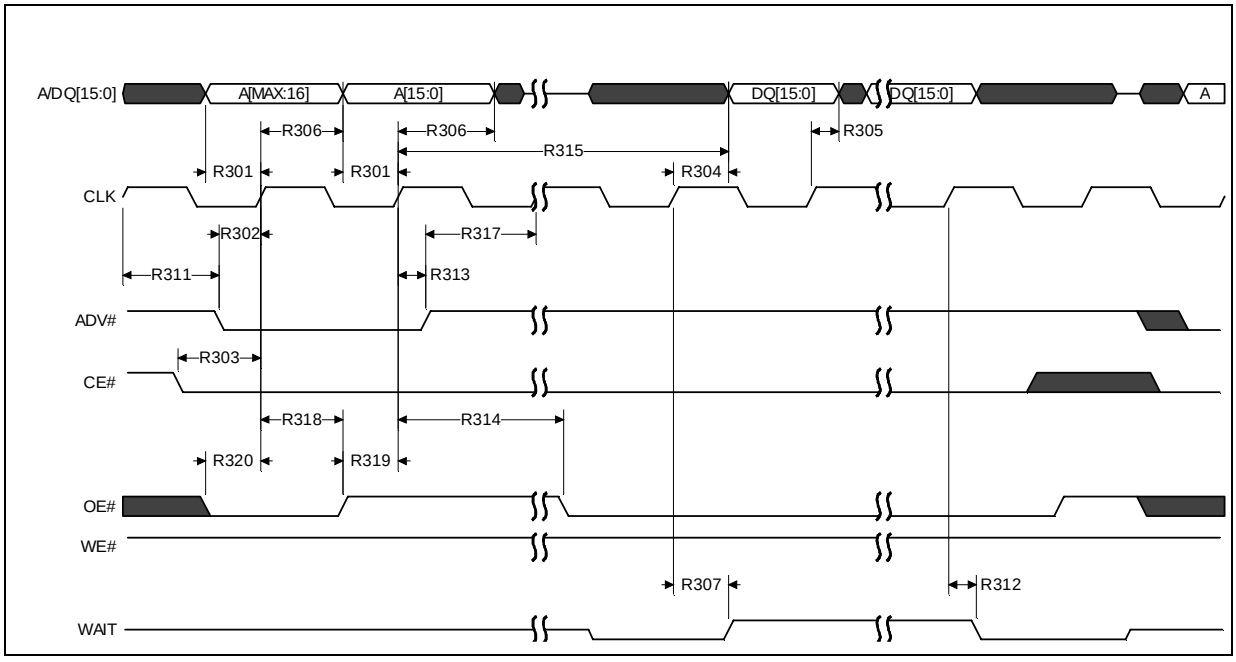
Figure 65: AADM Sync Burst Read Cycle (ADV# De-asserted between Address Cycles)



Notes:

1. Diagram shows WAIT as active low (RCR.10=0) and asserted *with* Data (RCR.8=0).
2. For no-wrap bursts, end-of-wordline WAIT states could occur (not shown in timing diagram).

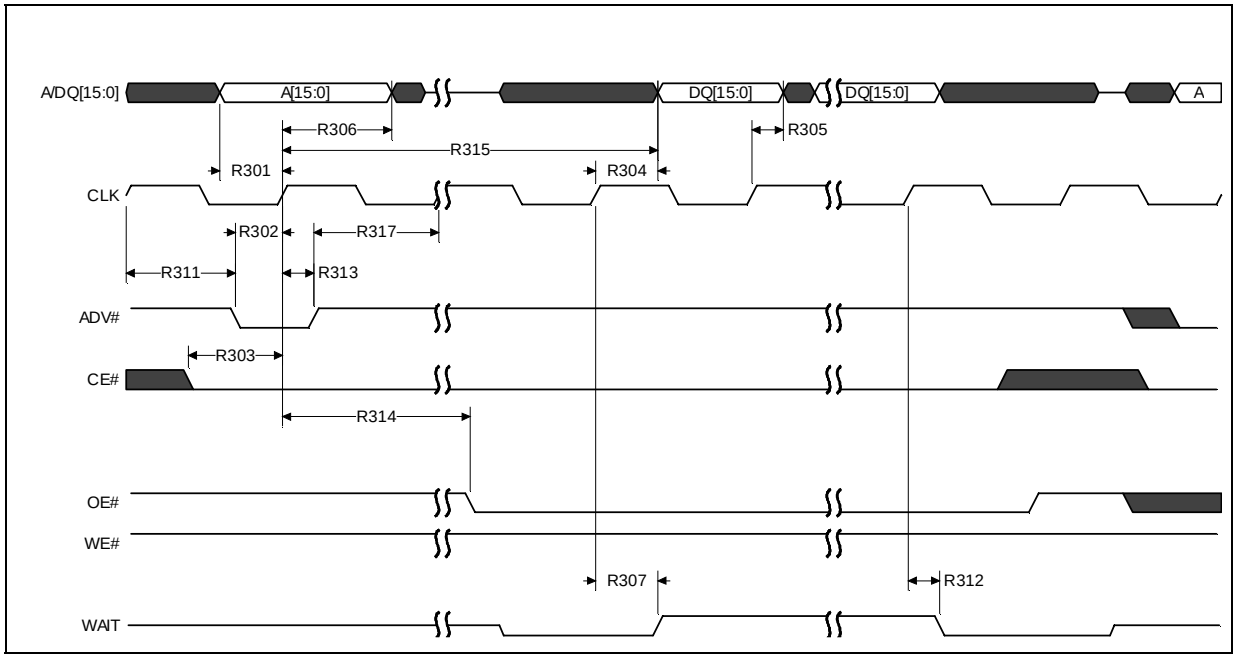
Figure 66: AADM Sync Burst Read Cycle (ADV# Not De-asserted between Address Cycles)



Notes:

1. Diagram shows WAIT as active low (RCR.10=0) and asserted *with* Data (RCR.8=0)

Figure 67: AADM Sync Burst Read Cycle (Latching A[15:0] only)



Notes:
1. Diagram shows WAIT as active low (RCR.10=0) and asserted with Data (RCR.8=0).
2. For no-wrap bursts, end-of-wordline WAIT states could occur (not shown in timing diagram)
3. Without latching A[MAX:16] in the Sync Read Cycle, the previously latched A[MAX:16] applies.

A.3.4 Synchronous Write Cycles

For synchronous writes, only the address latching cycle(s) are synchronous. Synchronous address latching is depicted in the timing diagrams for synchronous read cycles:

- Figure 65, “AADM Sync Burst Read Cycle (ADV# De-asserted between Address Cycles)” on page 134
- Figure 66, “AADM Sync Burst Read Cycle (ADV# Not De-asserted between Address Cycles)” on page 134
- Figure 67, “AADM Sync Burst Read Cycle (Latching A[15:0] only)” on page 135

The actual write operation (rising WE# edge) is asynchronous and is independent of CLK. Asynchronous writes are depicted in the timing diagrams for asynchronous write cycles:

- Figure 63, “AADM Asynchronous Write Cycle (Latching A[MAX:0])” on page 132
- Figure 64, “AADM Asynchronous Write Cycle (Latching A[15:0] only)” on page 132

A.3.5 System Boot

Systems that use the AADM mode will boot from the bottom 128k Bytes of device memory because A[MAX:16] are expected to be grounded in-system. The 128k Byte boot region is sufficient to perform required boot activities before setting RCR[4] to enable AADM mode.

Appendix B Additional Information

Order Number	Document/Tool
315567	Numonyx™ StrataFlash® Cellular Memory (M18) Developer's Manual
307654	Numonyx™ StrataFlash® Cellular Memory (M18 SCSP); 2048-Mbit M18 (Non-Mux and AD-Mux I/O) Family with Synchronous PSRAM Datasheet
310048	Designing with Numonyx™ StrataFlash® Wireless Memory and Pre-enabling Numonyx™ StrataFlash® Cellular Memory, Application Note 822
309311	Numonyx™ StrataFlash® Cellular Memory (M18 SCSP) to ARM® PrimeCell™ Design Guide, Application Note 841
315651	Migration Guide for Numonyx™ StrataFlash® Cellular Memory (M18) 90 nm to 65 nm, Application Note 860
310058	Effect of Program Buffer Size on System Interrupt Latency, Application Note 816

Notes:
4. Visit Numonyx's World Wide Web home page at http://www.numonyx.com for technical documentation and tools or for the most current information on Numonyx flash products.

Appendix C Ordering Information

To order samples, obtain datasheets or inquire about any stack combination, please contact your local Numonyx representative.

Table 66: 38F Type Stacked Components

PF	38F	5070	M0	Y	0	B	0
Package Designator	Product Line Designator	Product Die/ Density Configuration	NOR Flash Prodcut Family	Voltage/NOR Flash CE# Configuration	Parameter / Mux Configuration	Ballout Identifier	Device Details
PF = SCSP, RoHS RD = SCSP, Leaded	Stacked NOR Flash + RAM	Char 1 = Flash die #1 Char 2 = Flash die #2 Char 3 = RAM die #1 Char 4 = RAM die #2 (See Table 68, "38F / 48F Density Decoder" on page 137 for details)	First character applies to Flash die #1 Second character applies to Flash die #2 (See Table 69, "NOR Flash Family Decoder" on page 138 for details)	V = 1.8 V Core and I/O; Separate Chip Enable per die (See Table 70, "Voltage / NOR Flash CE# Configuration Decoder" on page 138 for details)	0 = No parameter blocks; Non-Mux I/O interface (See Table 71, "Parameter / Mux Configuration Decoder" on page 138 for details)	B = x16D Ballout (See Table 72, "Ballout Decoder" on page 139 for details)	0 = Original released version of this product

Table 67: 48F Type Stacked Components

PC	48F	4400	P0	V	B	0	0
Package Designator	Product Line Designator	Product Die/ Density Configuration	NOR Flash Prodcut Family	Voltage/NOR Flash CE# Configuration	Parameter / Mux Configuration	Ballout Identifier	Device Details
PC = Easy BGA, RoHS RC = Easy BGA, Leaded JS = TSOP, RoHS TE = TSOP, Leaded PF = SCSP, RoHS RD = SCSP, Leaded	Stacked NOR Flash only	Char 1 = Flash die #1 Char 2 = Flash die #2 Char 3 = Flash die #3 Char 4 = Flash die #4 (See Table 68, "38F / 48F Density Decoder" on page 137 for details)	First character applies to Flash dies #1 and #2 Second character applies to Flash dies #3 and #4 (See Table 69, "NOR Flash Family Decoder" on page 138 for details)	V = 1.8 V Core and 3 V I/O; Virtual Chip Enable (See Table 70, "Voltage / NOR Flash CE# Configuration Decoder" on page 138 for details)	B = Bottom parameter; Non-Mux I/O interface (See Table 71, "Parameter / Mux Configuration Decoder" on page 138 for details)	0 = Discrete Ballout (See Table 72 "Ballout Decoder" on page 139 for details)	0 = Original released version of this product

Table 68: 38F / 48F Density Decoder

Code	Flash Density	RAM Density
0	No Die	No Die
1	32-Mbit	4-Mbit
2	64-Mbit	8-Mbit
3	128-Mbit	16-Mbit
4	256-Mbit	32-Mbit
5	512-Mbit	64-Mbit
6	1-Gbit	128-Mbit
7	2-Gbit	256-Mbit
8	4-Gbit	512-Mbit
9	8-Gbit	1-Gbit
A	16-Gbit	2-Gbit
B	32-Gbit	4-Gbit
C	64-Gbit	8-Gbit
D	128-Gbit	16-Gbit
E	256-Gbit	32-Gbit
F	512-Gbit	64-Gbit

Table 69: NOR Flash Family Decoder

Code	Family	Marketing Name
C	C3	Numonyx™ Advanced+ Boot Block Flash Memory
J	J3v.D	Numonyx™ Embedded Flash Memory
L	L18 / L30	Numonyx™ StrataFlash® Wireless Memory
M	M18	Numonyx™ StrataFlash® Cellular Memory
P	P30 / P33	Numonyx™ StrataFalsh® Embedded Memory
W	W18 / W30	Numonyx™ Wireless Flash Memory
0(zero)	-	No Die

Table 70: Voltage / NOR Flash CE# Configuration Decoder

Code	I/O Voltage (Volt)	Core Voltage (Volt)	CE# Configuration
Z	3.0	1.8	Seperate Chip Enable per die
Y	1.8	1.8	Seperate Chip Enable per die
X	3.0	3.0	Seperate Chip Enable per die
V	3.0	1.8	Virtual Chip Enable
U	1.8	1.8	Virtual Chip Enable
T	3.0	1.8	Virtual Chip Enable
R	3.0	1.8	Virtual Address
Q	1.8	1.8	Virtual Address
P	3.0	3.0	Virtual Address

Table 71: Parameter / Mux Configuration Decoder (Sheet 1 of 2)

Code, Mux Identification	Number of Flash Die	Bus Width	Flash Die 1	Flash Die 2	Flash Die 3	Flash Die 4
0 = Non Mux 1 = AD Mux 3 = "Full" AD Mux	Any	NA	Notation used for stacks that contain no parameter blocks			
B = Non Mux C = AD Mux F = "Full" Ad Mux	1	X16	Bottom	-	-	-
	2		Bottom	Top	-	-
	3		Bottom	Bottom	Top	-
	4		Bottom	Top	Bottom	Top
	2	X32	Bottom	Bottom	-	-
	4		Bottom	Bottom	Top	Top

Table 71: Parameter / Mux Configuration Decoder (Sheet 2 of 2)

Code, Mux Identification	Number of Flash Die	Bus Width	Flash Die 1	Flash Die 2	Flash Die 3	Flash Die 4
T = Non Mux U = AD Mux W = "Full" Ad Mux	1	X16	Top	-	-	-
	2		Top	Bottom	-	-
	3		Top	Top	Bottom	-
	4		Top	Bottom	Top	Bottom
	2	X32	Top	Top	-	-
	4		Top	Top	Bottom	Bottom

Table 72: Ballout Decoder

Code	Ballout Definition
0 (Zero)	SDiscrete ballout (Easay BGA and TSOP)
B	x16D ballout, 105 ball (x16 NOR + NAND + DRAM Share Bus)
C	x16C ballout, 107 ball (x16 NOR + NAND + PSRAM Share Bus)
Q	QUAD/+ ballout, 88 ball (x16 NOR + PSRAM Share Bus)
U	x32SH ballout, 106 ball (x32 NOR only Share Bus)
V	x16SB ballout, 165 ball (x16 NOR / NAND + x16 DRAM Split Bus
W	x48D ballout, 165 ball (x16/x32 NOR + NAND + DRAM Split Bus