National Semiconductor

DS90CF363 +3.3V LVDS Transmitter 18-Bit Flat Panel Display (FPD) Link—65 MHz

General Description

The DS90CF363 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughputs is 170 Mbytes/sec.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- 20 to 65 MHz shift clock support
- Single 3.3V supply
- Chipset (Tx + Rx) power consumption < 250 mW (typ)
- Power-down mode (< 0.5 mW total)</p>
- Single pixel per clock XGA (1024x768) ready
- Supports VGA, SVGA, XGA and higher addressability.
- Up to 170 Megabytes/sec bandwidth
- Up to 1.3 Gbps throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Falling edge data strobe Transmitter
- Compatible with TIA/EIA-644 LVDS standard
- ESD rating > 7 kV
- Operating Temperature: -40°C to +85°C





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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V _{CC})	-0.3V to +4V				
CMOS/TTL Input Voltage	-0.3V to (V _{CC} + 0.3V)				
LVDS Driver Output Voltage	-0.3V to (V _{CC} + 0.3V)				
LVDS Output Short Circuit Duration	Continuous				
Junction Temperature	+150°C				
Storage Temperature	–65°C to +150°C				
Lead Temperature (Soldering, 4 sec)	+260°C				
Maximum Package Power Dissipation Capacity @ 25°C					
MTD48 (TSSOP) Package: DS90CF363	1.98 W				

Package Derating: DS90CF363	16 mW/°C above +25°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	> 7 kV

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V _{CC})	3.0	3.3	3.6	V
Operating Free Air				
Temperature (T _A)	-40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V _{CC})			100	$\mathrm{mV}_{\mathrm{PP}}$

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditio	ns	Min	Тур	Max	Units
CMOS/T	TL DC SPECIFICATIONS	·					
V _{IH}	High Level Input Voltage			2.0		V _{CC}	V
VIL	Low Level Input Voltage			GND		0.8	V
V _{OH}	High Level Output Voltage	I _{OH} = -0.4 mA		2.7	3.3		V
V _{OL}	Low Level Output Voltage	I _{OL} = 2 mA			0.1	0.3	V
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA			-0.79	-1.5	V
I _{IN}	Input Current	$V_{IN} = V_{CC}$, GND, 2.5V c	or 0.4V		±5.1	±10	μΑ
Ios	Output Short Circuit Current	V _{OUT} = 0V			-60	-120	mA
LVDS DO	SPECIFICATIONS			•			
V _{OD}	Differential Output Voltage	R _L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V _{OD} between complimentary output states					35	mV
Vos	Offset Voltage (Note 4)			1.125	1.25	1.375	V
ΔV_{OS}	Change in V _{OS} between complimentary output states				35	mV	
los	Output Short Circuit Current	$V_{OUT} = 0V, R_L = 100\Omega$	$V_{OUT} = 0V, R_1 = 100\Omega$		-3.5	-5	mA
I _{oz}	Output TRI-STATE® Current	$\overline{Power Down} = 0V,$ $V_{OUT} = 0V \text{ or } V_{CC}$			±1	±10	μA
V _{TH}	Differential Input High Threshold	V _{CM} = +1.2V				+100	mV
V _{TL}	Differential Input Low Threshold	1		-100			mV
I _{IN}	Input Current	$V_{IN} = +2.4V, V_{CC} = 3.6V$	$V_{IN} = +2.4V, V_{CC} = 3.6V$ $V_{IN} = 0V, V_{CC} = 3.6V$			±10	μA
		$V_{IN} = 0V, V_{CC} = 3.6V$				±10	μΑ
TRANSM	ITTER SUPPLY CURRENT						
ICCTW	Transmitter Supply Current	R _L = 100Ω,	f = 32.5 MHz		31	45	mA
	Worst Case	$C_L = 5 \text{ pF},$	f = 37.5 MHz		32	50	mA
		(Figures 1, 3)	f = 65 MHz		42	55	mA
ICCTG	Transmitter Supply Current	R _L = 100Ω,	f = 32.5 MHz		23	35	mA
	16 Grayscale	$C_L = 5 \text{ pF},$ 16 Gravesale Pattern	f = 37.5 MHz		28	40	mA
	(Figures 2, 3)	(Figures 2, 3)	f = 65 MHz		31	45	mA
ICCTZ	Transmitter Supply Current Power Down	Power Down = Low Driver Outputs in TRI-STATE® under Power Down Mode			10	55	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Electrical Characteristics (Continued)

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and Δ V _{OD}).

Note 4: V_{OS} previously referred as V_{CM} .

Transmitter Switching Characteristics Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Тур	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 3)			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 3)			0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 4)				5	ns
TCCS	TxOUT Channel-to-Channel Skew (Figure 5)			250		ps
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)	f = 65 MHz	-0.4	0	0.3	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		10.6	11.0	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period (Figure 6)			Т	50	ns
TCIH	TxCLK IN High Time (Figure 6)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 6)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (Figure 6)	f = 65 MHz	2.5			ns
THTC	TxIN Hold to TxCLK IN (Figure 6)		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay 25°C, V _{CC} = 3.3V (Figure 7)		3		5.5	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 8)				10	ms
TPDD	Transmitter Power Down Delay (Figure 11)				100	ns

AC Timing Diagrams



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Applications Information

The DS90CF363 and DS90CF364 are backward compatible with the existing 5V FPD Link transmitter/receiver pair (DS90CF563 and DS90CF564). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC} of both the transmitter

and receiver devices. This change may enable the removal of a 5V supply from the system, and power may be supplied from an existing 3V power source.

2. The DS90CF363 transmitter input and control inputs accept 3.3V TTL/CMOS levels. They are not 5V tolerant.





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