National Semiconductor

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CLC-CAPT-PCASM Data Capture Board User's Guide

Section I. Introduction

The CLC3790093 Data Capture Board enables simple evaluation of National Semiconductor's High Speed Analog to Digital Converters (ADCs) and the Diversity Receiver Chip Set (DRCS). The Data Capture Board interfaces the outputs of these devices to the standard serial port available on the back of most Personal Computers (PCs). We have provided PC software to control the data capture function and Matlab® scripts for data analysis.

A block diagram of the evaluation test bed is shown below.

The Data Capture Board contains a field-programmable gate array (FPGA) that controls its operation. An EPROM configures the FPGA after power is applied. The serial interface is provided by a UART (Universal Asynchronous Receiver/Transmitter), an oscillator, and a level translator IC. The captured data is stored in either three 32K x 8 static RAMs (organized into 24-bit words) or in a FIFO containing 32K 18-bit words. LEDs provide a visual indication of activity. DIP switches and a jumper configure several capture functions.

Section II. Capturing Data from ADC Evaluation Boards

Getting Started

To use the Data Capture board to capture data from a National Semiconductor Analog to Digital converter, you will need the following hardware, software, and documentation.

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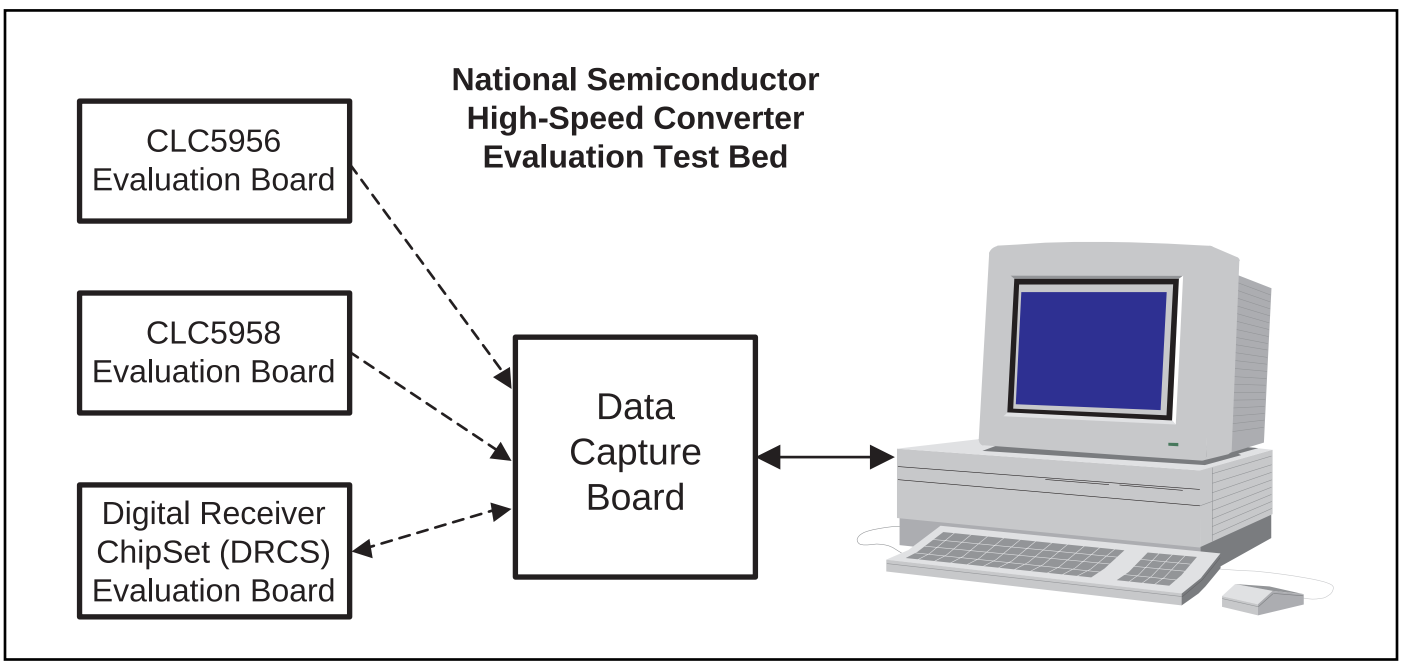
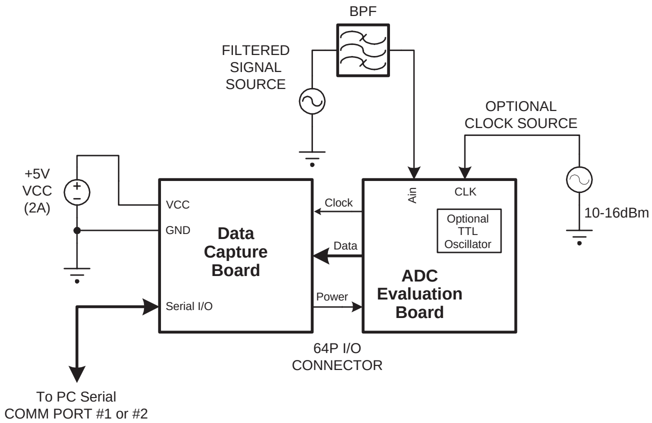




Hardware

1. CLC3790093 Data Capture Board (CLC-CAPT-PCASM)
2. CLC Evaluation Board. Several ADC products can be evaluated with this system. Currently, the choices are the CLC5956 (12-bit 65MSPS ADC), or the CLC5958 (14-bit 52MSPS ADC). Each product has a unique evaluation board (CLC5956PCASM or CLC5958PCASM) which plugs into the data capture board.
3. Personal Computer. An IBM-Compatible PC running Windows® 95, Windows® 98, or Windows® NT. The PC should have an available serial port capable of operating at 115,200 baud. These ports are usually labeled and referred to as COM1 and COM2. The captured data is stored in a file on the PC to allow custom analysis.
4. Serial Cable. A standard serial interface cable is provided. This cable connects the data capture board to the PC.
5. Power Supply. The data capture board requires a single +5V supply. This power is applied at connector J3. A 2-amp supply will provide enough current for the evaluation board and the data capture board. Note that the power for the evaluation board is provided from the data capture board through the 64-pin connector J1.
6. Input signal. You can provide any type of input signal that you feel is appropriate to your system testing. The data analysis software provided with the data capture board is oriented toward analysis of single tone sinewave inputs. Our recommendation for high purity, low phase noise reference signal sources is the Hewlett Packard HP8644B synthesizer. It provides an excellent input stimulus for evaluating ADC performance.
7. Bandpass or lowpass filter. Even with a good sinewave source, you will need to filter out the harmonics of the signal source. A bandpass filter also enables filtering of the wideband noise of the reference source. As an example, Allen Avionics (Mineola, NY) passive filters are used for most of our converter testing.
8. Clock Source. If you wish to test the ADC with a fixed clock frequency, you may install a standard TTL oscillator in the socket provided on the evaluation board. Otherwise, you will need to provide a low phase noise sinewave or square wave clock source at the appropriate SMA connector on the evaluation board. An amplitude of 10 to 16dBm is recommended. Here, again, the HP 8644B is a good choice.

Software

1. National Semiconductor Software. All of the required software is provided on a CD-ROM. To install the software now, insert the CD-ROM into your computer and follow the directions. The default installation copies all of the files to a directory called "c:\nsc". The data capture software is called "capture.exe".
2. Matlab. A copy of Matlab version 5.1 or later is required to operate the analysis routines. If you simply wish to capture data to a file on your PC and process the data with your own analysis software, then you will not need Matlab. For more information about Matlab, please see their website at http:// www.mathworks.com.
3. Matlab script files. The Matlab script files for data analysis are located in the "c:\nsc\mfiles" directory. These script files are run from the Matlab command prompt.

Documentation

The CD-ROM includes all of the following documentation, with the most current versions available on our website at http:// www.national.com:

1. CLC5956 data sheet
2. CLC5958 data sheet
3. Data Capture Board User's guide (this document).

Additional information is included on other products and their evaluation boards. If you are evaluating the Diversity Receiver Chip Set, please refer to Section III of this manual.

Operation of Data Capture Board

When evaluating the performance of an ADC, the data capture board has two main modes of operation. In the first mode, data is captured from the evaluation board under test at the full sample rate of the ADC. A contiguous set of 32k data samples is captured into a FIFO memory on the board, and then this data is moved over to the PC at a slower rate. The data set is stored in a file on the hard drive for later analysis. The data is stored in an ASCII file in exactly the format that it is output from the converter. For the CLC5956, the two's complement 12-Bit data is stored as numbers ranging from 0 to 4095. In the case of the 14-bit ADC5958, the two's complement data ranges from 0 to 16383. Each value is terminated with a carriage return, hexadecimal 0D. Note that the two's complement number can be converted to offset binary by inverting the MSB. This is the first step in the Matlab routine for FFT analysis.

CLC5956 Data				
Analog Input	Condition	Offset Binary Number	Two's Complement	ASCII Value Stored
Ain- >> Ain	- Full Scale	0000 0000 0000	1000 0000 0000	2048
Ain- > Ain	- Mid Scale	0111 1111 1111	1111 1111 1111	4095
Ain > Ain-	+ Mid Scale	1000 0000 0000	0000 0000 0000	0
Ain >> Ain-	+ Full Scale	1111 1111 1111	1111 1111 1111	2047
CLC5958 Data				
Analog Input	Condition	Offset Binary Number	Two's Complement	ASCII Value Stored
Ain- >> Ain	- Full Scale	00 0000 0000 0000	10 0000 0000 0000	8192
Ain- > Ain	- Mid Scale	01 0111 1111 1111	11 1111 1111 1111	16383
Ain > Ain-	+ Mid Scale	10 0000 0000 0000	00 0000 0000 0000	0
Ain >> Ain-	+ Full Scale	11 1111 1111 1111	01 1111 1111 1111	8191

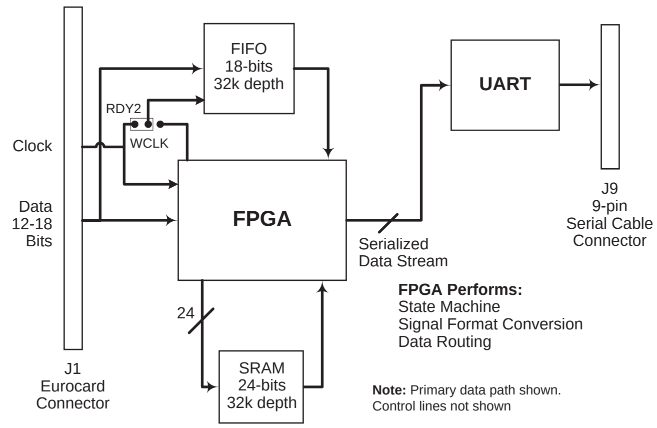
Histogram Mode

In the second mode of operation, the “Histogram” mode, the data capture board operates as a hardware histogrammer. The board does not collect a contiguous record from the ADC; instead, it compiles statistical information by counting the number of times that the ADC outputs each code. The most significant 15 bits of the converter define 32K histogram bins. The MSB of the data is inverted before being stored (all data is treated as offset binary format). ADC data is aligned to the least significant bit, and unused higher bits are set to 0s. Each bin is cleared initially. The ADC output code is used as the address for the SRAM on the board, and as each code is read by the Data Capture board, the data at that location in the SRAM is read, incremented and written back to the SRAM. This counting requires multiple clock cycles, so the data is not counted in real time. In fact, 11 samples of data are missed for each sample that is counted. The histogram capture terminates when a bin reaches the count specified by DIP switches 4 and 5. The 32K histogram bin counts are then returned via the serial port. If the input signal to the ADC is a pure sinusoid, then the histogram information can be compared to the theoretical probability density of a sinusoid and the linearity of the ADC can be calculated. The supplied Matlab script DNL_INL uses this method. Please refer to the IEEE Standard for Digitizing Waveform Recorders (IEEE Std 1057-1994) for more information about this technique.

Hardware Configuration

Jumpers

The data capture board has 3 jumpers that must be configured before use. The first jumper, VCORE, sets the core voltage used by the FPGA. This jumper is always set to 5V. (A voltage regulator on the board reduces the supplied +5V to +3.3V for the FPGA I/O and other components on the board.) The second jumper, WCLK, selects the clock source for the FIFO. When capturing data from an ADC evaluation board, **WCLK should always be set to RDY2**. This selects the DR (Data Ready) clock line from the ADC evaluation board pin 20B. The third jumper block, J2, is unused.



Data Capture Board Block Diagram

DIP Switches

Five of the eight DIP switches are used to configure several capture functions as follows.

DIP switch 1: This DIP switch specifies whether a Diversity Receiver Evaluation Board or an ADC Evaluation Board is attached to the Data Capture Board.

ON → ADC Evaluation Board is attached. Captured data is aligned to the least significant bit with unused higher bits set to 0s.

DIP switches 2 and 3: When DIP switch 1 is ON to indicate that an ADC Evaluation Board is attached, DIP switches 2 and 3 specify the width of the ADC data so it can be aligned to the least significant bit and unused higher bits can be set to 0s.

Switch:	2	3	Number of Bits in ADC
	OFF	OFF	18
	OFF	ON	16
	ON	OFF	14
	ON	ON	12

DIP switches 4 and 5: These DIP switches specify the maximum histogram bin count. The histogram capture terminates when any bin reaches the count specified by these switches.

Switch:	4	5	Maximum Count
	OFF	OFF	16384
	OFF	ON	8192
	ON	OFF	4096
	ON	ON	2048

A maximum count of 16384 corresponds to approximately 2.5 million total samples for a 12-Bit ADC. The capture is very fast (on the order of 1 second for a 52 MSPS clock rate) so there is not much advantage in setting the switches for a lower maximum count. The other settings are more useful for the DRCS evaluations because the effective clock rate can become very low with certain output formats and decimation ratios.

SMA Connectors

The output clock SMA connector provides a signal that can be used to phase lock a signal source. The frequency is that of the input clock signal divided by 2. For example, with an attached CLC5958 ADC evaluation board at 52MSPS the clock output signal will be a 26MHz square wave. The second SMA connector is currently unused.

Serial Port

The serial port is configured at 115,200 baud with one stop bit, no parity, and 8-bits per character. Although the DSR, CTS, and RTS control signals are connected, they are not used. XON/XOFF flow control is supported. The flow of returned data pauses after an XOFF character (DC3, ctrl-S, hexadecimal 13) has been received. The flow of returned data resumes after an XON character (DC1, ctrl-Q, hexadecimal 11) has been received. The Data Capture Board initializes as if an XON character had been received.

Power Up the System

Once the WCLK jumper and the DIP switches have been set, (for example, for the CLC5956 we have set WCLK at RDY2 and DIP switches 1,2,3,4,5 as ON,ON,ON,OFF,OFF) connect the evaluation board to the data capture board, apply power, clock, and signal to the boards, and connect the serial cable to the PC. Some PCs will need to be rebooted at this point, but it may not be necessary with your PC. In the software configuration section, next, we will check the communication between the PC and the data capture board.

Light Emitting Diode (LED) Status Monitors

3 of the 6 LEDs are used to provide status indications.

LED 1: This LED is connected to an address line of the static RAM ICs. While the static RAM is being written or read, it blinks. After the Data Capture Board is powered up and the FPGA is initialized, it is on to indicate that the board is ready. After all the SRAM data has been output, it is off.

LED 2: This LED is on when captured data is available to be output to the serial port. After all the data has been output, it is off.

LED 6: This LED is connected to the clock signal selected by DIP switch 1. When the clock is toggling, it will be on at less than full intensity.

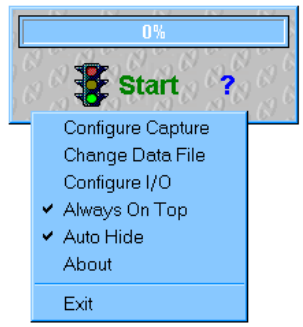
So, at this point in your setup, you should have LED 1 on at full intensity and LED 6 on at reduced intensity. You are now ready to configure the software for data capture.

Software Configuration

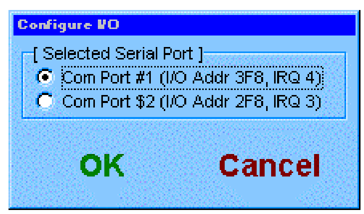
Run the program ***"capture.exe"***. It is located in the directory that you chose during the CD-ROM installation. The default directory is ***"c:\nsc\"***. You can also use the start menu: start → programs → nsc → capture.

When you run ***capture.exe***, you will see the following window pop up onto your PC:

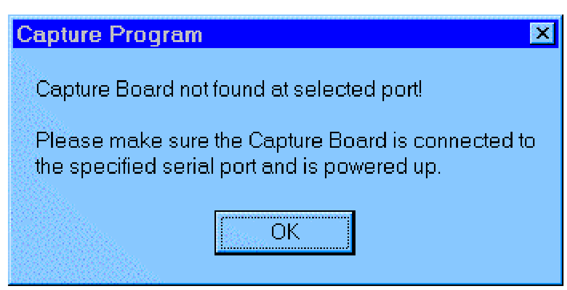
This is the data capture control panel. It is small to conserve monitor area for other programs. The main function of the panel is to initiate data capture. Before we capture data we must configure the computer and the board. By clicking on the ***control panel*** with the RIGHT mouse button (right click), we bring up the following configuration menu:



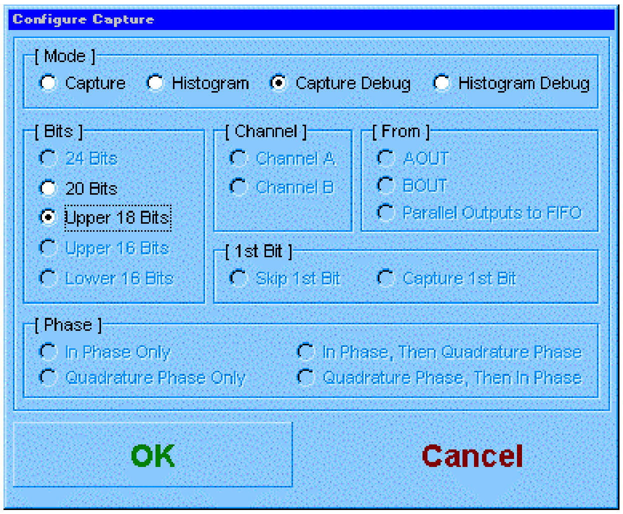
The first thing to configure is the COM port on the computer, so move the mouse to ***"Configure I/O"*** and click with the LEFT mouse button. This will bring up the following menu:



Select the COM port that you have attached to the data capture board, and press ***"OK"***. The computer will then send a command to the data capture board. If the data capture board responds and the COM port interface is operating correctly, the ***"Configure I/O"*** menu will disappear, and the Data Capture control panel will return. If there is a problem with the COM port interface, you will get the following message:

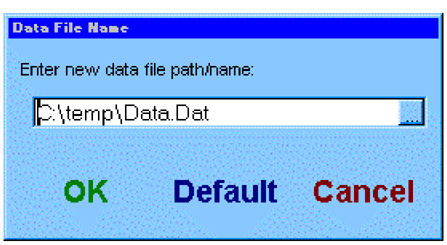


Verify the connections and, if necessary, try the other COM port. (Note that you must have a clock applied to the ADC Evaluation board during this communication verification stage. Check to make sure that either an external clock or the TTL oscillator is installed, and that LED6 is on at reduced intensity.) Once you get a proper exit from this step, you are ready to configure the capture board. Right click on the capture control panel, then left click on ***"Configure Capture."*** You will see the following screen:



To configure the capture board for direct capture of a contiguous 32k point record of ADC output codes, click on the selections shown above. Left click on ***"Capture Debug"*** and select ***"Upper 18 Bits."*** The names of these selections may seem rather cryptic when you are simply capturing ADC data. The label names are derived from functions in the DRCS and CLC5902, so they might seem out of context for ADC capture uses. Don't worry about the label names, just make sure you have selected the modes as shown above. Then click on ***"OK."***

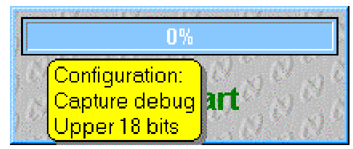
One final configuration remains. You need to tell the program where to store your data. Right click on the capture control panel, then left click on ***"Change Data File."*** You will see the following menu:



By left clicking on the little box to the right of the text entry window, you can select any disk, directory, and file name that suits you. However, we recommend that you start with the default file name and location shown. Click on ***"Default"*** and then on ***"OK"***. If you do not have a C:\temp directory, please make one. The reason for this is that the Matlab script files for data analysis look automatically for the file ***C:\temp\data.dat***. If you wish to store the data elsewhere, you will need to modify the Matlab m-files to look for your data file in a different location. Obviously, if you are using your own software for data analysis this is not a concern.

Capture Data!

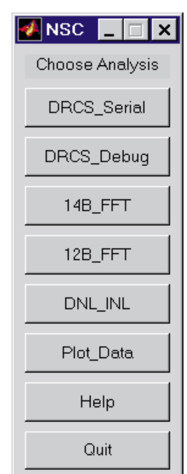
We are finally ready to capture data from the ADC. As a final check, you can move the mouse until it is on top of the progress bar (the big bar on the data capture control panel that now reads (0%). You should see a little yellow box appear that confirms your capture settings.



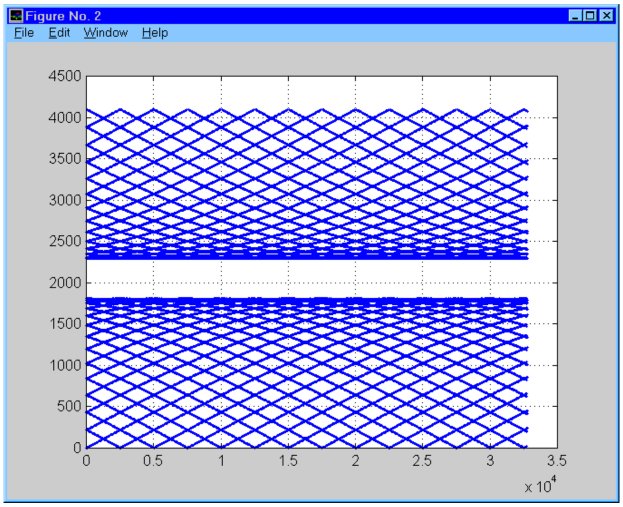
Now, simply left-click on the ***"Start"*** button on the capture control panel to start the process. You will see LED 2 light up on the board, and the bar at the top of the capture control panel will show the progress of the data transfer. At 52MSPS, the 32768 samples are collected in only 630 microseconds; the rest of the time is the serial port transfer. Typical times for this transfer are on the order of 10 to 15 seconds. To analyze the data using the Matlab Mfiles that we have provided, please start Matlab at this time. To include the provided script files in your Matlab path, type the following command at the Matlab command prompt:

>> path(path,'c:\nsc\mfiles')

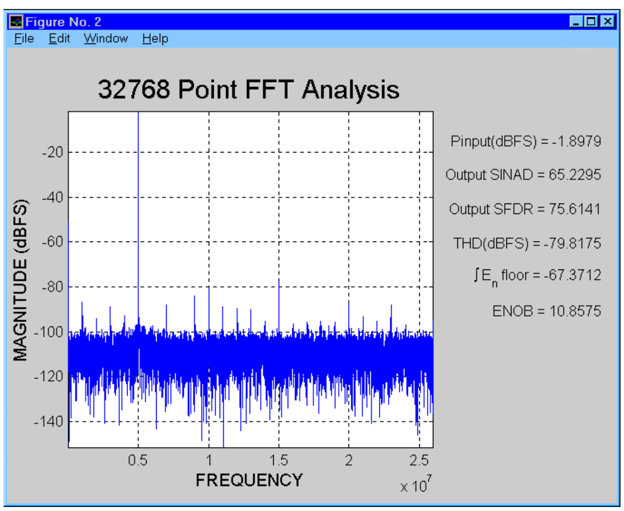
Alternatively, you can change directories at the Matlab prompt until this is the current directory. From the Matlab command prompt, type ***"analysis_menu"***. This will bring up the following menu:



To look at the data that you have just captured, left click on the "Plot_Data" button. If you have collected data with a 12-bit ADC at 52MSPS and a -2dBFS sinewave input at 5MHz, you will see two's complement data that looks like this:



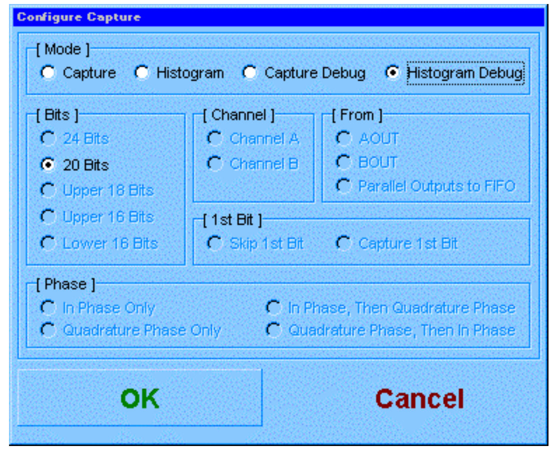
Next, left click on the 12B_FFT button, and you will see the following FFT plot and performance summary. (Note that if you are testing a 14-bit ADC you should set SW1 accordingly and click on the 14B_FFT button instead.)



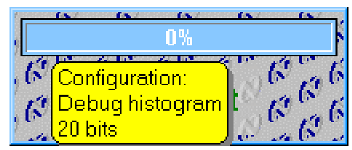
For more information on the Matlab routines, please refer to section IV of this manual or the "analysis.txt" file in the Mfiles directory.

Configuring for Histogram Capture (DNL and INL Analysis)

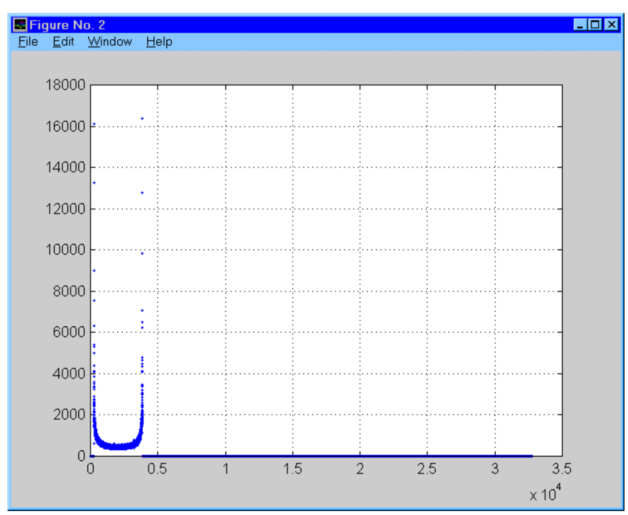
To configure the board for histogram capture, right click on the capture control panel, then left click on "Configure Capture." You will see the capture configuration menu:



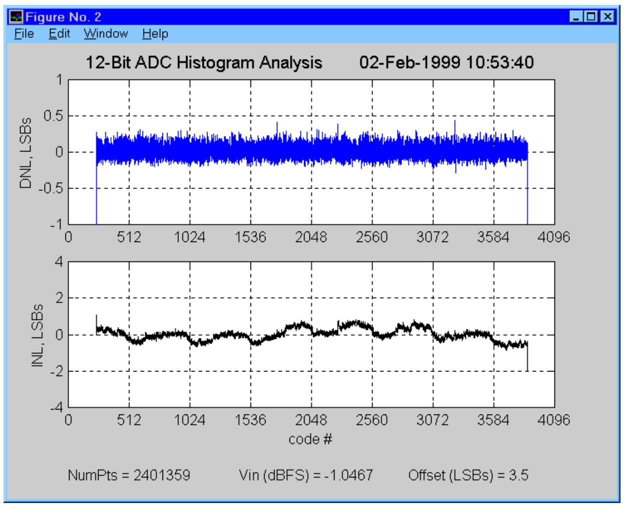
Select ***"Histogram Debug"***, as shown above, and click on ***"OK".*** When the data capture control panel returns, you can verify your capture settings by positioning the mouse over the progress bar. You will see the following display:



When you press Start now, the SRAM will be cleared and then the board will count the number of times each code is output. When any count reaches the number that you set with DIP switches 4 and 5, the counting will stop and the data will be transferred. At 52 MSPS and a maximum count of 16384, the counting takes about 1 second. You will see LED1 flash as data is written to and read from the SRAM. LED2 will again light for about 10-15 seconds as the data is transferred to the PC and stored in the file that you have selected. To use the included m-files to analyze the histogram data and extract the DNL and INL of the ADC, start Matlab and run ***"analysis_menu"***. If you still have the Matlab analysis menu visible you can again click on ***"Plot_Data"*** to see the histogram information:

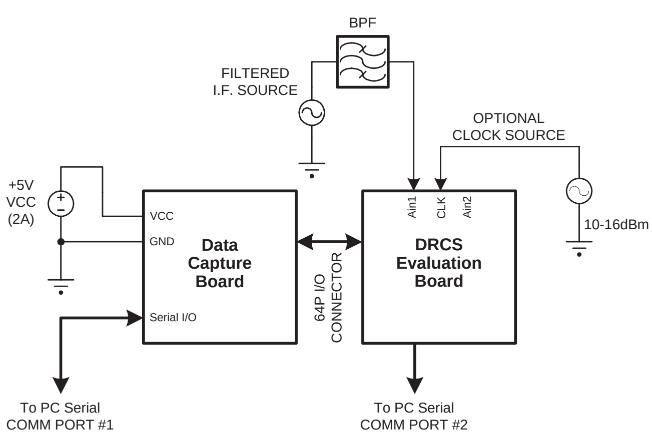


In this example, we have captured data from a 12-Bit ADC. Remember that the data that we are plotting is the bin count information. The ADC output codes that were exercised ranged from code 236 to code 3865. The maximum count was set to 16384 (with DIP switches 4 and 5 OFF) and for this particular data record the maximum count was reached at the ADC output code of 3864. To analyze the converter's linearity, you can left click on the ***"DNL_INL"*** button, and you will see the following analysis window:



For more information about this analysis technique, please refer to Section IV of this document, the comments in the DNL_INL script file, or the IEEE Standard for Digitizing Waveform Recorders (IEEE Std 1057-1994).

Section III. Capturing Data from the Diversity Receiver Chipset (DRCS) Evaluation Board



Diversity Receiver Chipset Evaluation Setup

Getting Started

To use the Data Capture board to capture data from National's DRCS Evaluation Board, you will need the following hardware, software, and documentation. Several analysis tools are provided in the form of Matlab scripts. It will prove helpful if the user has some familiarity with the CLC5902 data sheet and the Diversity Receiver Evaluation Board User Manual document.

Hardware

1. CLC730093 Data Capture Board. (CLC-CAPT-PCASM)
2. CLC730090 DRCS Evaluation Board. (CLC-DRCS-PCASM)
3. DC Power Supply - The DRCS Evaluation and Capture Board combination require +5V at >1A.
4. An IBM-Compatible Personal Computer running Windows 95, Windows 98, or Windows NT with a serial port capable of 115,200 baud.
5. Serial data cable to connect the data capture board to the PC.
6. Low noise, filtered, IF Signal source for analog input to DRCS.
7. OPTIONAL - Low jitter clock source (10 - 16dBm sinewave) if DRCS crystal oscillator is removed.

Software

1. "Capture.exe" - Contained in the provided CDROM.
2. Data storage space on PC hard drive (default path & name = "c:\temp\data.dat").
3. Matlab (version 5.1 or higher) to run analysis routines.

Documentation

The following applicable documents can be found on the provided CDROM, with the most current versions available on our website at http:// www.national.com:

1. CLC5526 - Data sheet for the Digitally controlled Variable Gain Amplifier (DVGA).
2. CLC5956 - Data sheet for the 12-bit, 65MSPS, IF sampled ADC.
3. CLC5902 - Data sheet for the Dual Digital Tuner/ AGC (DDC/AGC).
4. Diversity Receiver ChipSet Evaluation Board User's Manual (for CLC-DRCS-PCASM).

General Description and Program Options

Data from the Diversity Receiver ChipSet (DRCS) Evaluation Board can be captured from either of its two serial outputs, its parallel outputs, or its debug outputs. The serial in-phase and quadrature-phase data can also be captured simultaneously for quadrature data analyses. The Data Capture Board always returns 32,768

24-bit words via the serial port as 96K bytes. Each word is interpreted as a 24-bit two's complement integer and stored as 32K ASCII words in a user defined file. Each value is terminated with a carriage return (hexadecimal 0D). When a Diversity Receiver Evaluation Board is attached to the Data Capture Board, data narrower than 24 bits is aligned to the most significant bit with unused lower bits set to 0s. Serial data is always 24-bits wide. Because of the various DRCS data output formats, care must be exercised to ensure that configuration conflicts do not occur between the Data Capture board and the DRCS board. Such conflicts usually lead to unpredictable data formats. The default DRCS settings, ***"I/Q_Packed, Mux_Mode",*** are compatible with the Data Capture Board's 24-bit serial and 16-bit parallel formats.

The "CLK" SMA connector provides a buffered output of the DRCS Serial Clock (SCLK) divided by 2. The CLC5902 ***"RATE"*** register can be used to further divide this clock. This clock output is intended for phase locking a signal source to the DRCS XTAL oscillator. Because of the FPGA speed limitations, DRCS Serial Clock "RATE" settings <2 are not recommended. The default DRCS settings and XTAL oscillator yield a 13MHz output from this SMA jack.

Serial data from the CLC5902 (DDC/AGC) can be configured for ***"I/Q_Packed, Mux_Mode"*** in the majority of evaluations (refer to the CLC5902 data sheet or the DRCS Evaluation Board User Manual). For proper operation, a decimation of at least 192 in the DDC is required to complete the transfer of the whole 96-bit word (24-bits each of CHA I & Q phase and CHB I & Q phase). The Data Capture board de-serializes the DRCS data stream, registers the selected channel and phase, stores the data in SRAM, then reads and formats the SRAM data to a 24-bit word for transmission to the PC via its serial communications port.

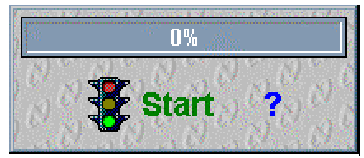
Parallel and Debug port data can be written directly to the 18-bit by 32K FIFO or to the 24-bit by 32K SRAM. Because the FIFO has its own address counter, it is capable of contiguous block capture up to 75MSPS and is the recommended means of data capture for Fourier Analysis of high speed data. The SRAM address and write is controlled by the FPGA, which requires about 6 clock strobes per write cycle resulting in data decimation. The SRAM is useful for displaying time records of data or collecting contiguous blocks of slower data that have been decimated by the CLC5902 DDC. The SRAM is the memory element used for the board's hardwired histogram data generation.

Capture Board Hardware Configuration Options for DRCS data capture

Place the ***WCLK*** (FIFO write clock) jumper in the ***"PIN 120"*** position, the ***VCORE*** should be in the ***"5V"*** position and the eight ***SW1*** switches in their ***"OFF"*** position.

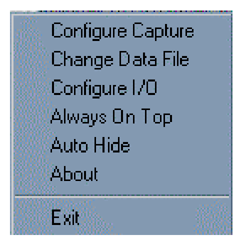
Using the DATA CAPTURE Control Panel

The Data Capture Program, ***"capture.exe"***, must be copied into a directory on the user's PC. The setup/install program on the CDROM automatically places this program in a default directory (c:\nsc\). The program generates a user *.ini file within this same directory. The file is used to store the user options and is updated each time the user changes the options and runs the program. When the Data Capture Program is started, a graphical user interface (GUI) Control Panel is placed on the PC desktop.



The **left mouse button** can be used to drag the control panel to the desired position on the desktop. The Data Capture control panel should not be placed on top of the Windows task bar, otherwise the software may behave erratically. A left click on the ***?*** button will open an informational text file. The program configuration variables must be setup prior to running the program using the ***"Start"*** button. Clicking the ***right mouse button*** within the control panel brings up the user configuration options menu. The left mouse button is again used to select the desired menu option.

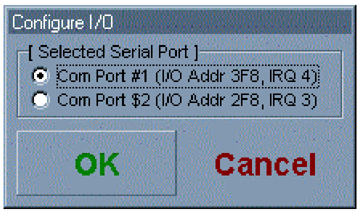
The following discusses the function of the various menu options:



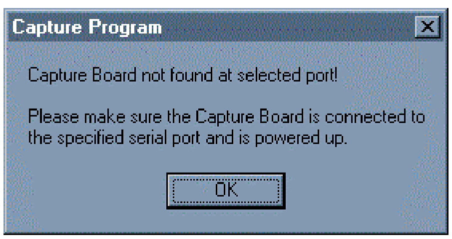
The ***"Exit"*** button terminates the Data Capture Program. The ***"About"*** button opens a window that displays the version of the Data Capture Program as well as the firmware revision of the FPGA on the Data Capture Board. Clicking the left mouse button on the ***"SysInfo"*** button in the About window replaces it with the System Information window that displays some details about your PC. Clicking the left mouse button on the ***"OK"*** button in the System Information window closes it and returns you to the About window. Clicking the left mouse button on the ***"Visit our web page"*** text will open National Semiconductor's web page using your internet browser. Clicking the left mouse button on the ***"OK"*** button in the ***"About"*** window will close it.

The ***"Auto Hide"*** and ***"Always on Top"*** selections enable and disable these functions. A check mark to the left of each selection indicates when it is enabled.

The ***"Configure I/O"*** button opens the user port option menu window. Clicking the left mouse button selects the desired port (the default Windows address and IRQ is assumed). Clicking the ***"OK"*** button sends an identification command out the selected port and listens for the Capture board to echo back the command. This function requires that DC power and data clock is present. If the hardware is functional and the proper PC port connected, the Configure I/O window will then close and return back to the user Control Panel. Capture Board LED#6 will be lit if the data clock is present.

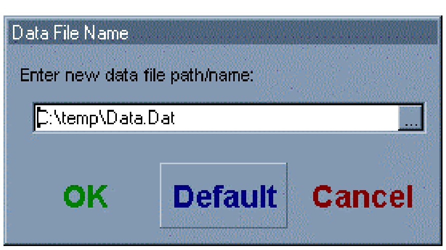


If the incorrect serial port is selected or if the hardware is dysfunctional (i.e. missing power or clock) the program will return an error-warning window.



Click the ***"OK"*** button to clear the warning and then try the other PC serial port in the ***"I/O Configuration"*** window or correct the hardware problem.

The ***"Change Data File"*** button enables a dialog window where the user can direct the location of the captured data file. The desired file name and path can be typed into the box. Clicking the left mouse on the button on the right side of the file name box opens a standard browser window to search for an appropriate file name. The ***"Default"*** button restores the default directory and file name. The attached Matlab script analysis routines (*.m files) assume that the data is located at this location; however, the user can edit the routines to load from the appropriate location. Clicking the ***"OK"*** button updates the Capture program's *.ini file and returns to the Capture Control Panel.



The ***"Configure Capture"*** button invokes the user dialog window for the remainder of the configuration options. After selecting the desired options, a left mouse click on ***"OK"*** stores the configuration variables and returns to the Control Panel. Positioning the mouse pointer over the Progress Bar inside the Control Panel pops up a text bubble which displays the configuration variables used when the Capture Program is started. Next is a discussion of the Mode functions and the related sub-functions:

MODES

There are four primary modes in which to run the data capture system, each with its own associated options:

1. ***Capture*** mode configures the Capture Board for data reception from the DRCS evaluation board. Both serial and the parallel output ports can be used as the source data path.

a) The ***24-Bits*** option captures serial DRCS data ***FROM*** either of the two serial data ports. The ***Capture 1st*** Bit option should be selected for this mode of data capture. With CLC5902 DDC in ***"packed"*** and ***"mux_mode"***, the ***AOUT*** data source contains both phases of both DDC channels. The two ***Channel*** buttons select the desired DDC channel to be stored in the SRAM. The four ***Phase*** buttons select either I or Q phase or the ordering of alternating I/Q phases. In this latter case, the 32K RAM space is shared. Therefore, only 16K points of each phase are collected. If the ***BOUT*** data source is selected, the CLC5902 DDC must be instructed accordingly (i.e. "packed" and "mux_mode" off). With the DDC in its default output format, the ***BOUT*** serial port is disabled.

b) The ***Upper 16-Bits*** and ***Lower 16-Bits*** options enable the CLC5902 DDC's parallel outputs. In this configuration the DDC parallel output mux is controlled by the FPGA through the 64 pin Euro connector (be sure that the DRCS board SW1 ***"POUT"*** switches are OFF/OPEN). The user selects ***Channel*** and ***Phase*** and the FPGA instructs the DDC which channel, phase, and which half of the 32-bit output word to send out its parallel data bus. This configuration uses the FIFO for temporary data storage.

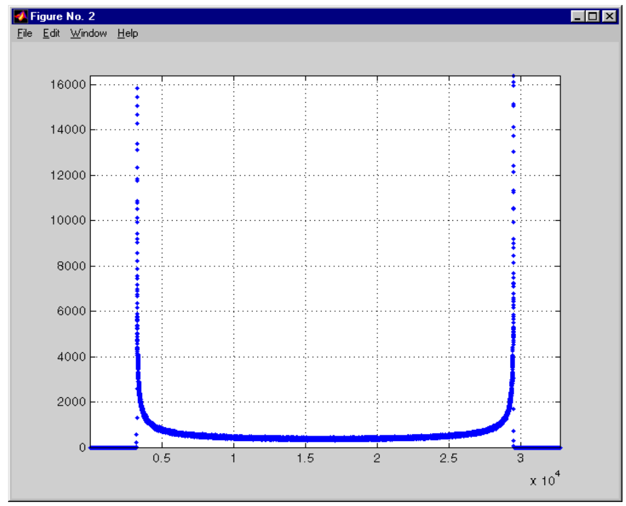
2. ***Histogram*** mode returns the Capture Board to the 24-bit serial data mode. As before, with the CLC5902 DDC in "packed" and "mux_mode", the ***AOUT*** data source contains both phases of both DDC channels. A DDC change is required to enable the ***BOUT***. The ***Capture 1st Bit*** option should be selected as before. In the ***Histogram*** configuration, the program ***Start*** button first sets every SRAM location value to zero. The hardware then samples the data, reads the value at that memory location, increments the value, and writes back the updated value. The process continues until one of the memory values reach the target value set by SW1

#4 & #5 as indicated in the Histogram Max Target table. Due to a high data resolution and relatively slow data rate, **a relatively long period of time is required for generating histogram data from the DRCS with high decimation values in the DDC.** Under some circumstances, the serial PC interface will time out. The program detects this condition and queries the user to continue. Click ***"Yes"*** to continue and wait for the Progress Bar to run to completion. Be patient, it could take several minutes depending on the input amplitude and DDC decimation value and Histogram Target Value. The last mode description, ***Debug Histogram***, provides further description of the output file generated by the hardwired histogram generator.

Histogram Target Table

SW1; #4	SW1; #5	Histogram Target Value
0	0	16K
0	1	8K
1	0	4K
1	1	2K

3. ***Capture Debug*** mode configures the Capture Board to collect data from the DRCS evaluation board's 20-bit parallel debug data bus. Because the FIFO memory is limited to 18 bits, the user is given the option to collect the full data width in the SRAM by selecting the ***20 Bits*** menu button. As previously mentioned, parallel data which runs at the full clock speed (i.e. ***Mixer Out*** at Debug port) gets decimated by 6 due to the fact that the FPGA requires multiple clock strobes to address and write data into the SRAM. Choosing the ***Upper 18 Bits*** option will use the high speed FIFO for the memory element and collect a contiguous 32K block of data. The ***Debug*** data port provides users access to nodes internal to the CLC5902 DDC. Refer to the DRCS Evaluation Board User Manual and CLC5902 data sheet for more detailed information.
4. ***Histogram Debug*** mode configures the Capture Board to generate a histogram file using the parallel data as the source. The hardware requires multiple clock strobes to increment each SRAM value. Even though the data used is not a contiguous block, the probability density information is retained. The SRAM depth (32K) is used to store the data bin values; therefore, the histogram generator is limited to 15-bits of resolution (there are only 32,767 bins). The values of all 32K bins will be read out of the SRAM and sent out to the users PC regardless of the resolution of the data source. The DRCS ***Debug*** data will be displayed at the 15-bit resolution limit (this is also the case for the DRCS 24-bit Serial Out data) and the histogram will be centered about 16,384 assuming there is no intentional DC offset. The following figure displays the sine wave histogram data of the DRCS output generated by the Capture Board at an input frequency of 150MHz and 16dBm in amplitude using all the default DRCS settings. The data source was the DDC serial output (***Capture Histogram*** mode was used where Fsample is 270KHz) and therefore took several minutes to collect. In this scenario the 24-bit data source resolution is truncated to the 15-bits (32K) of available SRAM. The histogram peak target was set to 16K which required over 16 million data points be processed for the input level of -2dB below full scale. The number of data points is proportional to the Max Target and the amplitude range of the data (the X-axis). The "Plot Data" menu function of the analysis tools was used to generate the actual Matlab plot figure.



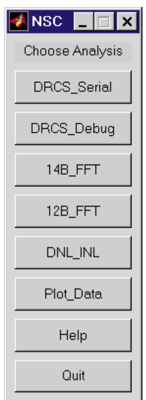
DRCS Evaluation Setup Sanity Check

The following discussion is to confirm the DRCS evaluation setup. The example uses a Fourier analysis of a simple, single tone, sinusoidal IF input to the DRCS. It is assumed that Setup.exe on the evaluation kit's CDROM has installed the necessary files in the user's PC and the DRCS and Data Capture hardware is configured as shown in the diagram at the front of ***Section III***. It is also assumed that Matlab (version 5.1 or higher) is available. Reconfiguration of the DRCS through its Control Panel software is not required for these two tests. The DRCS default values contained within the micro-controller with SW2:1-8 = OFF (on DRCS board) will configure the CLC5902 with the proper values. If the power has been applied while in another state or if the user has ***RESET*** the micro-controller with a different switch setting, then set the SW2 switches to OFF and press the ***RESET*** button on the DRCS Evaluation board.

** ***Apply an IF input signal*** to the AIN1 jack on the DRCS Evaluation board at 150MHz and 0dBm. The DDC mixer is set to -5.97MHz which brings the aliased (Fclk ADC = 52MHz; 3rd alias = 156MHz) signal down to +30KHz. The DDC then filters and decimates the data and sends it out the serial port (***AOUT***) in the "packed", "muxed_mode" format.

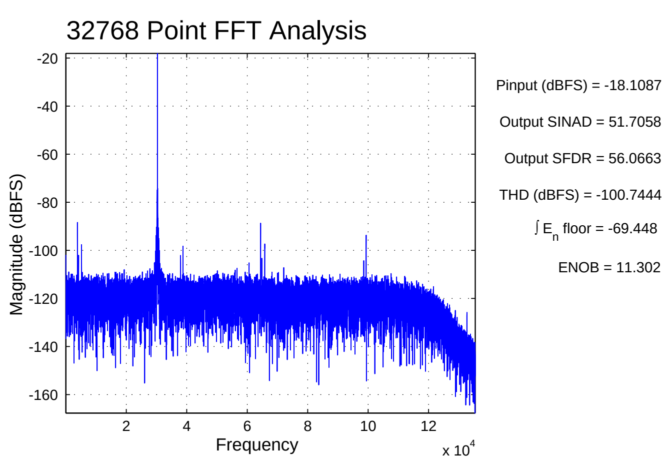
** From the Windows Start Programs menu, ***launch the Capture program*** (it's inside the ***C:\nsc*** folder). Right click inside the Control Panel and select ***Configure I/O*** and click the appropriate PC COM port button. Next, right click inside the Control Panel and select ***Configure Capture***. Select the following options: ***Mode = Capture; Bits =24; Channel = A; From = AOUT; 1st Bit = Capture 1st Bit; Phase = In Phase Only.*** Click ***"OK"*** and then click the ***Start*** button in the Control Panel to start the data capture. The progress bar should conclude in about 10 seconds.

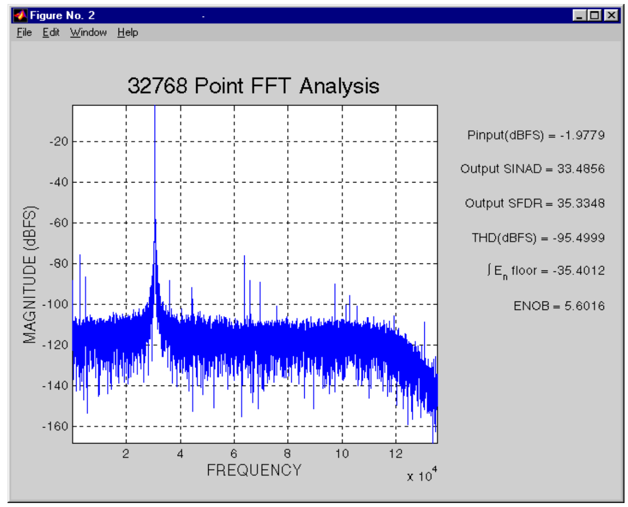
** Launch Matlab. Use the Matlab path browser to include the analysis Mfiles. The installed default path is: "c:\nsc\mfiles". Add this to the Matlab paths, save the directory file and exit the path browser. At the Matlab command line enter "analysis_menu". A GUI will appear. Left click on the ***DRCS_Serial*** button to perform an FFT on the captured data.



The menu disappears while the analysis routine is running. The process takes 4 - 5 seconds on a 133MHz PC and plots the results when finished.

The FFT should report an input power of about -18dBFS.





The FFT plot above and the analysis results highlight several setup issues. The poor SINAD (and corresponding ENOB) is due to phase jitter (spec'd as SSB Phase Noise) of the IF signal source (an HP8656 was used here). A better choice of signal synthesizer is the HP8644B, which yields a SINAD of about 60dB under the same conditions. The main portion of the noise power is contained in the carrier's immediate sidebands (±5KHz).

Another point of interest is that there are several spectral lines about -75dBFS and 25KHz on either side of the fundamental. These have been traced to the ground loop created by the PC serial interface. Both serial interface cables were connected while this data was being collected. Removing the cable to the DRCS will reduce the amplitude of these spurs. Some of the ground loop remains because of the required Capture Board's serial interface to the PC.

Section IV. Data Analysis Tools

The Matlab scripts contained on the Evaluation Kit CDROM provide a convenient toolset for evaluation of National's Diversity Receiver ChipSet (DRCS) and high speed ADCs like the CLC595x family. There are 4 FFT routines and 1 Sine Histogram routine which can be called from a user interface menu, "analysis_menu". **Set the Matlab path and working directory to that of the "Mfiles" provided on the Evaluation Kit CDROM. Run "analysis_menu" from the Matlab command window** to open a graphical user interface. Each of the called FFT routines has its appropriate variables set prior to the data analysis. These variables are explained in the adjacent text and can be easily edited to adjust for a particular application from Matlab's script editor. There are also comments within the routines that highlight various analysis blocks.

** ***DRCS_Serial*** “DRCS_ser_fft.m” is the script intended for analysis of the DRCS 24-bit serial output data. Fsample is set to a default of 52e6/192 which is the GSM standard output rate of 270.833KS/s. The “search’ option is enabled; therefore, excluding the DC bins, the peak FFT bin is assumed to be the input fundamental. A default 4-term data window is used.

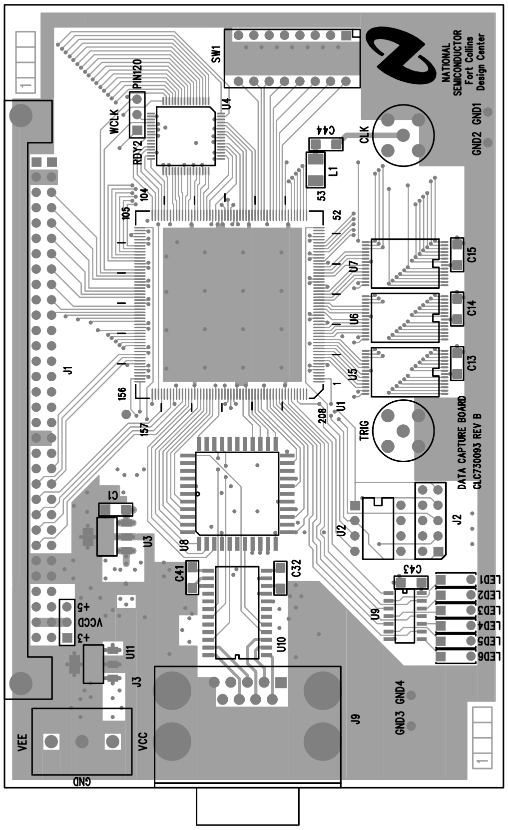
** ***DRCS_Debug*** “DRCS_par_fft.m” is the script intended for analysis of the DRCS 16-20 bit parallel debug data. The hardware setting will determine the actual Fsample variable needed. The data is always placed within a 24-bit word with MSB justification. The default Fsample is set to the assumed clock frequency of 52MHz with no decimation. If a debug port is selected which has decimated data, the Fsample variable will require an appropriate adjustment. Carefully edit and save the new value into the script file. The original file can be recovered from the CDROM.

** ***14-bit FFT*** “b14_FFT.m” is the script intended for data analysis in conjunction with the CLC5958 Evaluation Board. All the FFT routines can be run with a rectangular window by setting the variable to “0”. Setting the “Dither” variable excludes a lower portion of the spectrum from the FFT analysis and is intended to be used in conjunction with a base-band dither signal being present at the ADC analog input.

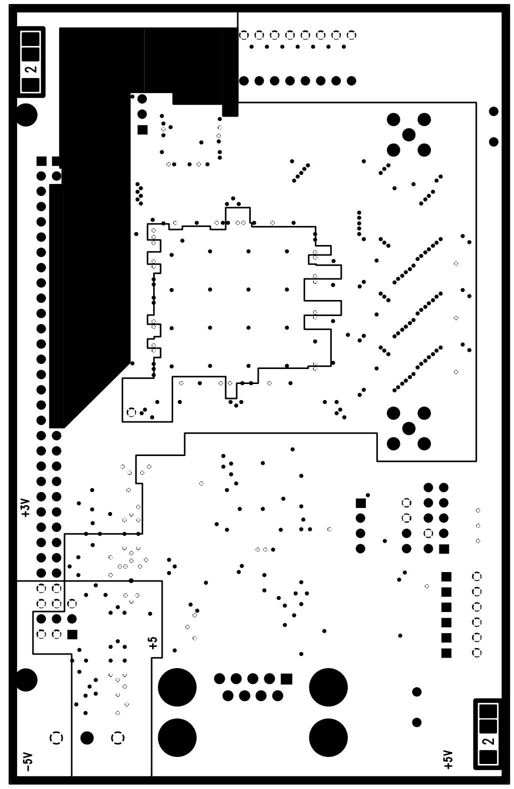
** ***12-bit FFT*** “b12_FFT.m” is the script intended for data analysis in conjunction with the CLC5956 Evaluation Boards.

** ***DNL_INL*** “dnl_inl.m” - is the script intended for data analysis of the histogram data file generated by the Data Capture Board. The data file has a fixed 2^15 length (i.e. the number of histogram bins). SW1 on the Capture Board is set to LSB justify the ADC data within the 2^15 bins. 12-18 bit histograms are supported. This Matlab script automatically scales to the data source. In addition to the graphic plots, the routine gives the number of samples, input amplitude (dBFS of ADC), and data DC offset (in LSBs). See the Data Capture Board User Manual for more info.

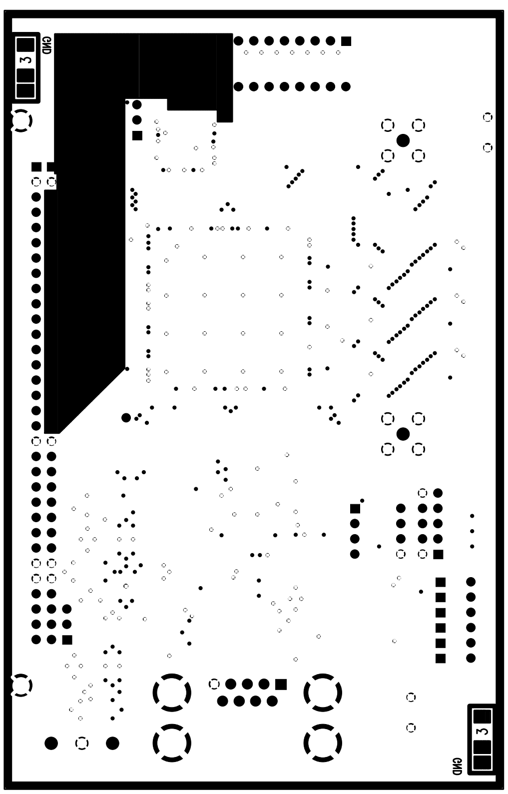
** ***Plot_Data*** this script is contained within “analysis_menu.m”. It simply clears the figure, loads the data file from the default location, and plots the new data. ***No data manipulation*** occurs. If the user wishes to view offset binary formatted data which has been normalized to ±1, he should first run the appropriate FFT analysis, then clear the plot figure (use ***“clf“***at Matlab command line) and plot the variable ***“u”*** (use ***“plot(u,’.’)”*** at Matlab command line).



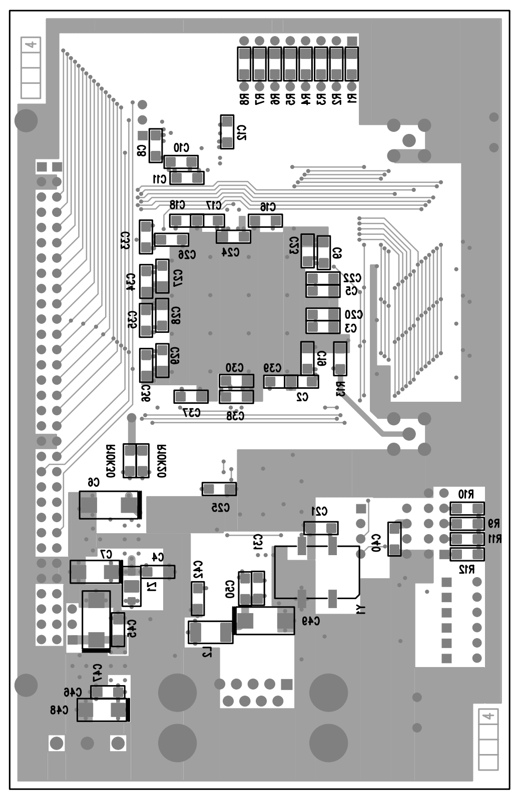
CLC-CAPT-PCASM Evaluation Board - Layer 1



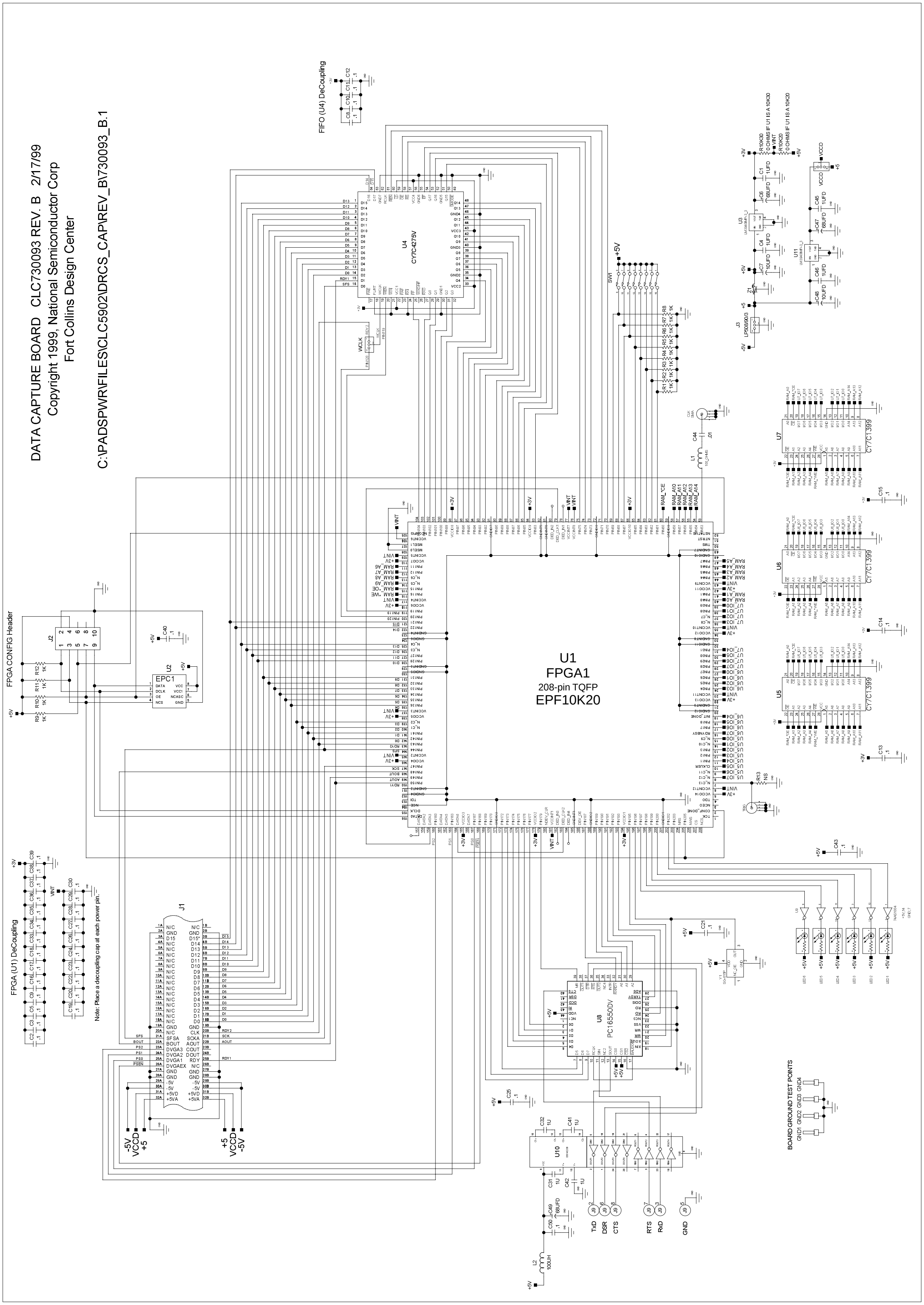
CLC-CAPT-PCASM Evaluation Board - Layer 2



CLC-CAPT-PCASM Evaluation Board - Layer 3



CLC-CAPT-PCASM Evaluation Board - Layer 4



CLC-CAPT-PCASM Schematic Diagram

CLC-CAPT-PCASM
Data Capture Board User's Guide

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408