

February 1988

CD4009M/CD4009C Hex Buffers (Inverting) CD4010M/CD4010C Hex Buffers (Non-Inverting)

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3V to 15V providing $V_{CC} \leq V_{DD}$.

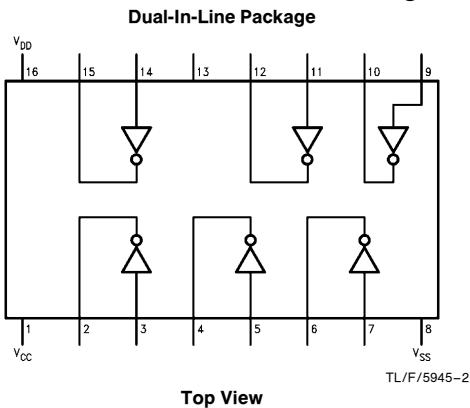
Features

- Wide supply voltage range3.0V to 15V
- Low power100 nW (typ.)
- High noise immunity0.45 V_{DD} (typ.)
- High current sinking capability8 mA (min.) at $V_O = 0.5V$ and $V_{DD} = 10V$

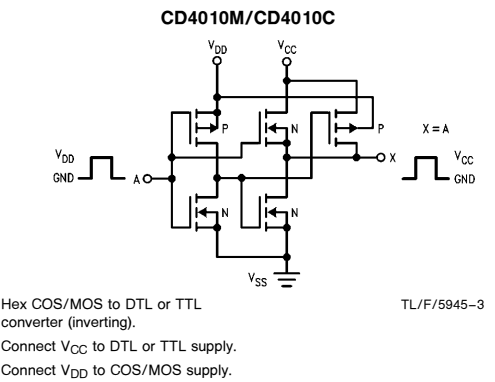
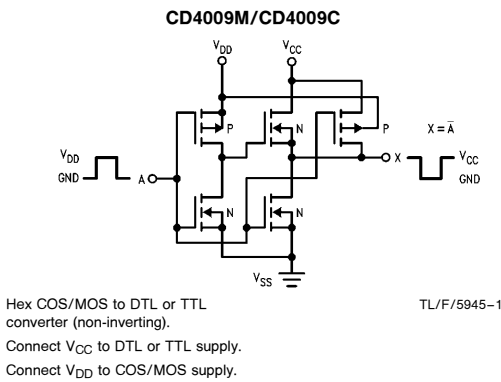
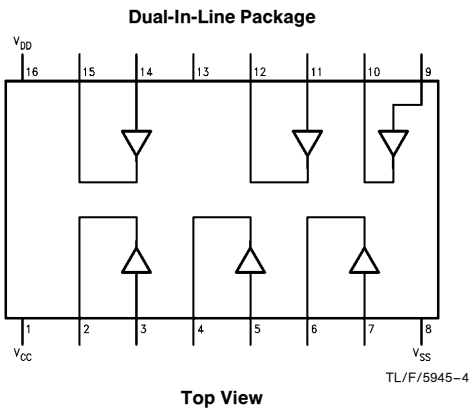
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Schematic and Connection Diagrams



Order Number CD4009 or CD4010



CD4009M/CD4009C Hex Buffers (Inverting)
CD4010M/CD4010C Hex Buffers (Non-Inverting)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1) $V_{SS} - 0.3V$ to $V_{SS} + 15.5V$

Operating Temperature Range

CD40XXM $-55^{\circ}C$ to $+125^{\circ}C$

CD40XXC $-45^{\circ}C$ to $+85^{\circ}C$

Storage Temperature Range (T_S)

$-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)

Dual-In-Line

700 mW

Small Outline

500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds)

260°C

Operating Range (V_{DD})

$V_{SS} + 3V$ to $V_{SS} + 15V$

DC Electrical Characteristics

Symbol	Characteristics	Test Conditions (Volts)		Limits														Units
				CD40XXM						CD40XXC								
				− 55°C		+ 25°C		+ 125°C		− 40°C		+ 25°C		+ 85°C				
		V _O	V _{DD}	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
I _{CC}	Quiescent Device Current		5 10		0.3 0.5		0.01 0.01	0.3 0.5		20 30		3 5		0.03 0.05	3 5		42 70	μA μA
P _D	Quiescent Device Dissipation/Package		5 10		1.5 5		0.05 0.1	1.5 5		100 300		15 50		0.15 0.5	15 50		210 700	μW μW
V _{OL}	Output Voltage Low Level		5 10		0.01 0.01		0 0	0.01 0.01		0.05 0.05		0.01 0.01		0 0	0.01 0.01		0.05 0.05	V V
V _{OH}	High Level		5 10	4.99 9.99		4.99 9.99	5 10		4.95 9.95		4.99 9.99		4.99 9.99	5 10		4.95 9.95		V V
V _{NL}	Noise Immunity (All Inputs)																	
	CD4009M	$\left\{ \begin{array}{l} V_O \geq 4.0 \\ V_O \geq 8.0 \end{array} \right.$	5 10	1 2		1 2	2.25 4.5		0.9 1.9		1 2		1 2	2.25 4.5		0.9 1.9		V V
V _{NL}	CD4010M	$\left\{ \begin{array}{l} V_O \geq 1.5 \\ V_O \geq 3.0 \end{array} \right.$	5 10	1.6 3.2		1.5 3	2.25 4.5		1.4 2.9		1.6 3.2		1.5 3	2.25 4.5		1.4 2.9		V V
V _{NH}		$\left\{ \begin{array}{l} V_O \geq 3.5 \\ V_O \geq 7.0 \end{array} \right.$	5 10	1.4 2.9		1.5 3	2.25 4.5		1.5 3		1.4 2.9		1.5 3	2.25 4.5		1.5 3		V V
I _{DN}	Output Drive Current N-Channel (Note 2)	0.4 0.5	5 10	3.75 10		3 8	4 10		2.1 5.6		3.6 9.6		3 8			2.4 6.4		mA mA
I _{DP}	P-Channel (Note 2)	2.5 9.5	5 10	−1.85 −0.9		−1.25 −0.6	−1.75 −0.8		−0.9 −0.4		−1.5 −0.72		−1.25 −0.6			−1 −0.48		mA mA
I _{IN}	Input Current						10							10				pA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

Note 2: I_{DN} and I_{DP} are tested one output at a time.

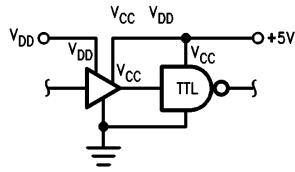
AC Electrical Characteristics*

$T_A = 25^{\circ}C$, $C_L = 15$ pF, unless otherwise noted. Typical Temperature coefficient for all values of $V_{DD} = 0.3\%/^{\circ}C$

Characteristics	Test Conditions		Limits						Units
			CD40XXM			CD40XXC			
	V _{DD} (Volts)	Min	Typ	Max	Min	Typ	Max		
Propagation Delay Time: High-to-Low Level (t _{PHL})	V _{CC} = V _{DD}	5 10	— —	15 10	55 30	— —	15 10	70 40	ns
Low-to-High Level (t _{PLH})	V _{DD} = 10V V _{CC} = 5V		—	10	25	—	10	35	
	V _{CC} = V _{DD}	5 10	— —	50 25	80 55	— —	50 25	100 70	
	V _{DD} = 10V V _{CC} = 5V		—	15	30	—	15	40	
									ns
Transition Time: High-to-Low Level (t _{THL})	V _{CC} = V _{DD}	5 10	— —	20 16	45 40	— —	20 16	60 50	ns
Low-to-High Level (t _{TLH})	V _{CC} = V _{DD}	5 10	— —	80 50	125 100	— —	80 50	160 120	ns
Input Capacitance (C _i)	Any Input		—	5	—	—	5	—	pF

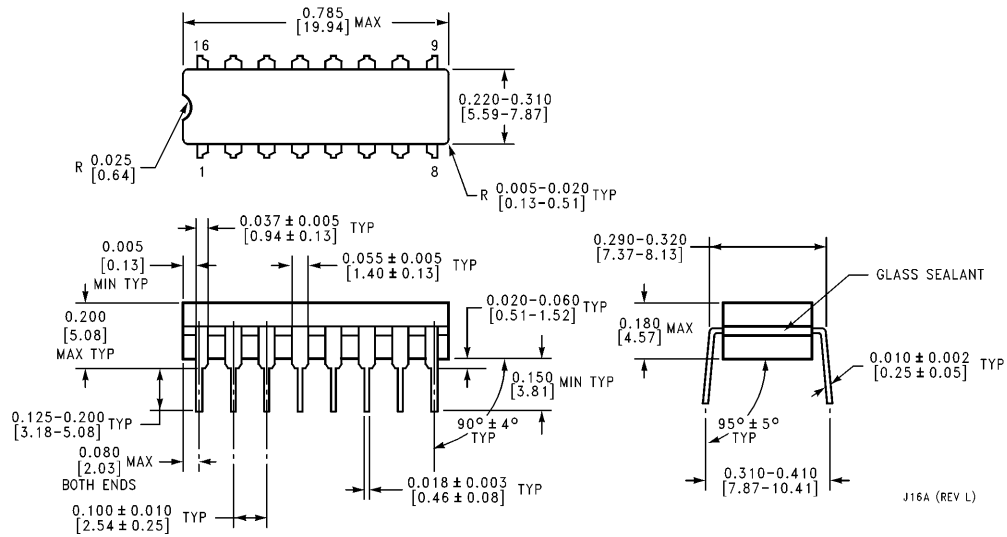
*AC Parameters are guaranteed by DC correlated testing.

Typical Application



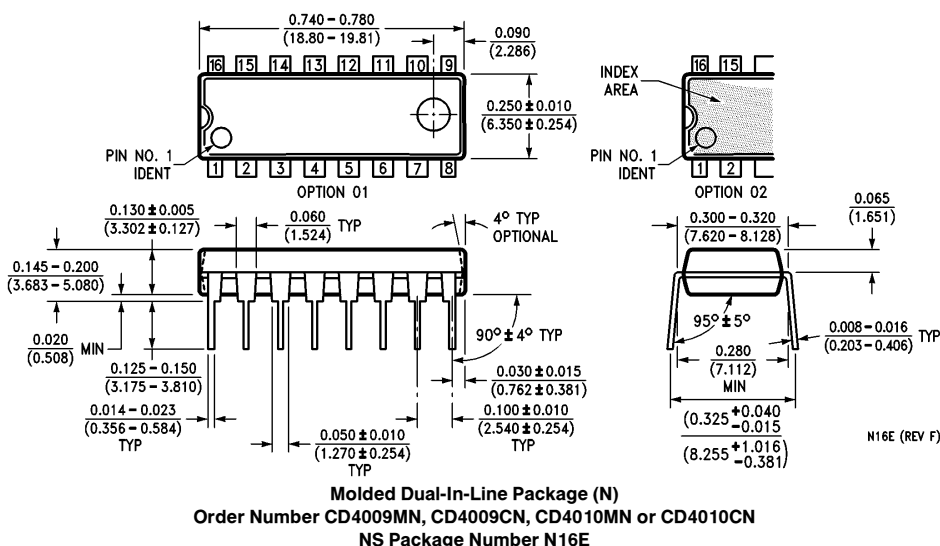
TL/F/5945-5

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4009MJ, CD4009CJ, CD4010MJ or CD4010CJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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