

May 1995

54F/74F322 Octal Serial/Parallel Register with Sign Extend

General Description

The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with TRI-STATE® parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register.

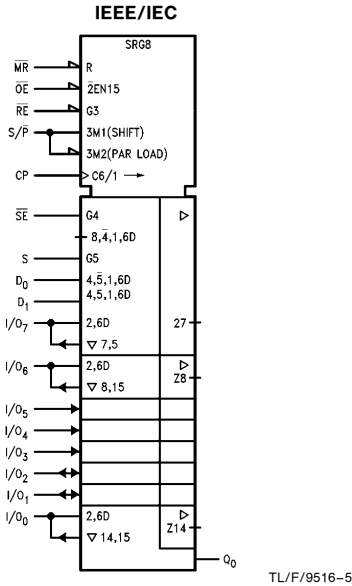
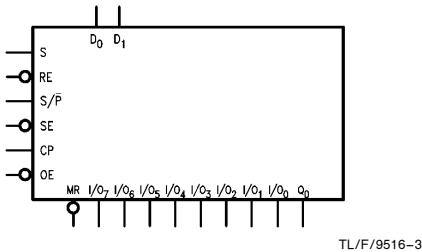
Features

- Multiplexed parallel I/O ports
- Separate serial input and output
- Sign extend function
- TRI-STATE outputs for bus applications

Commercial	Military	Package Number	Package Description
74F322PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F322DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F322SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F322FM (Note 2)	W20A	20-Lead Cerpack
	54F322LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SJX.
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

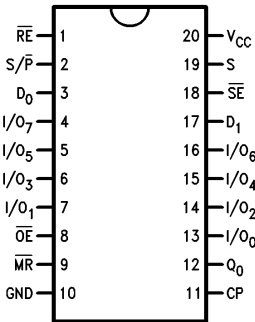
Logic Symbols



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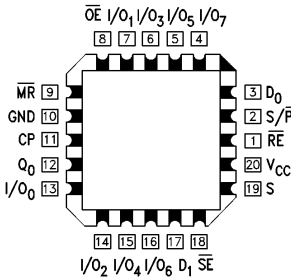
Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak



TL/F/9516-1

Pin Assignment
for LCC



TL/F/9516-2

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{RE}$	Register Enable Input (Active LOW)	1.0/1.0	20 μ A/ –0.6 mA
S/ $\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	1.0/1.0	20 μ A/ –0.6 mA
$\overline{SE}$	Sign Extend Input (Active LOW)	1.0/3.0	20 μ A/ –1.8 mA
S	Serial Data Select Input	1.0/2.0	20 μ A/ –1.2 mA
D ₀ , D ₁	Serial Data Inputs	1.0/1.0	20 μ A/ –0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/ –0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μ A/ –0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μ A/ –0.6 mA
Q ₀	Bi-State Serial Output	50/33.3	–1 mA/ –20 mA
I/O ₀ –I/O ₇	Multiplexed Parallel Data Inputs or TRI-STATE Parallel Data Outputs	3.5/1.083 150/40 (33.3)	70 μ A/ –0.65 mA –3 mA/24 mA (20 mA)

Functional Description

The 'F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on S/ $\overline{P}$ enables shift right, while a LOW signal disables the TRI-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal

on $\overline{SE}$ enables serial entry from either D₀ or D₁, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q₇ reloads its contents, thus performing the sign extend function required for the 'F384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the TRI-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Select Table

Mode	Inputs							Outputs								Q ₀
	$\overline{MR}$	$\overline{RE}$	S/ $\overline{P}$	$\overline{SE}$	S	$\overline{OE}^*$	CP	I/O ₇	I/O ₆	I/O ₅	I/O ₄	I/O ₃	I/O ₂	I/O ₁	I/O ₀	
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀	I ₀
Shift Right	H	L	H	H	L	L		D ₀	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₁
	H	L	H	H	H	L		D ₁	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₁
Sign Extend	H	L	H	L	X	L		O ₇	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₁
Hold	H	H	X	X	X	L		NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH all I/O_n terminals are at the high impedance state; sequential operation or clearing of the register is not affected.

Note 1: I₇–I₀ = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q₀) are isolated from the I/O terminal.

Note 2: D₀, D₁ = The level of the steady-state inputs to the serial multiplexer input.

Note 3: O₇–O₀ = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

H = HIGH Voltage Level

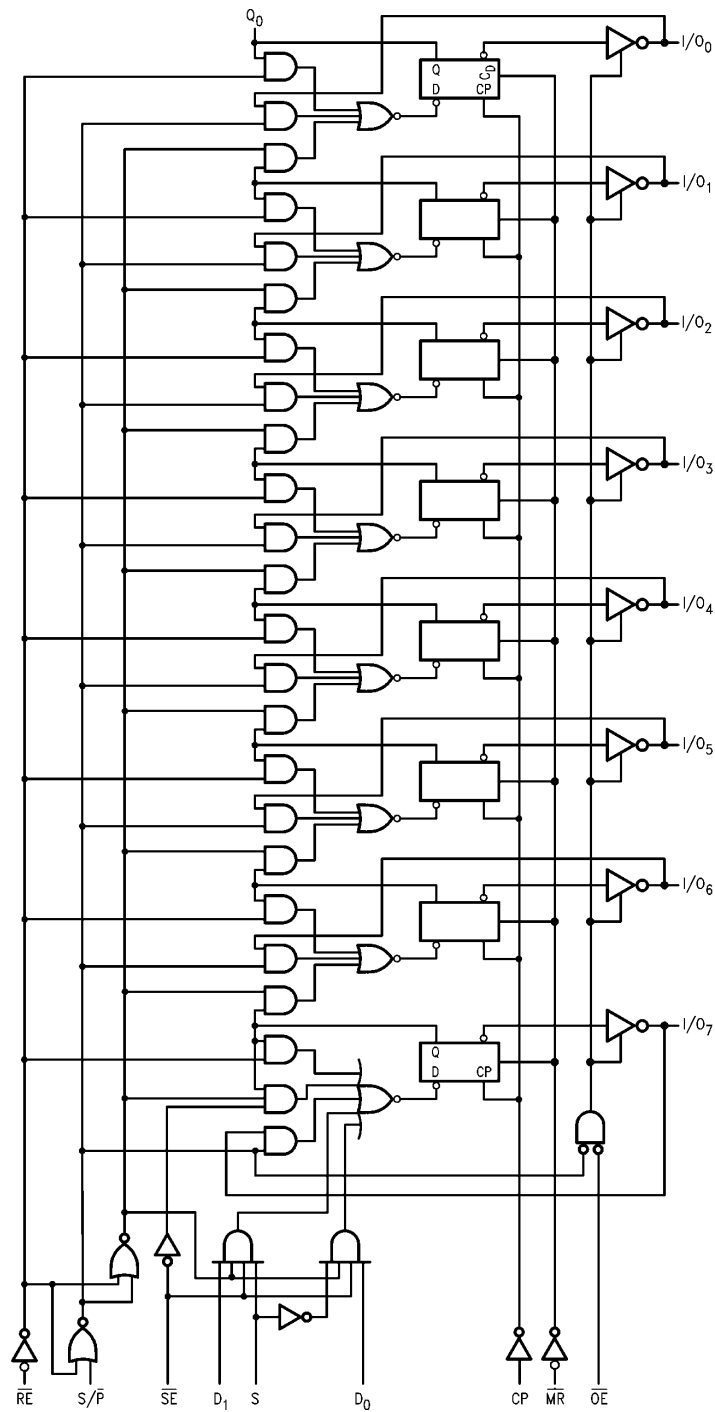
L = LOW Voltage Level

Z = High Impedance Output State

 = LOW-to-HIGH Transition

NC = No Change

Logic Diagram



TL/F/9516-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output
in HIGH State (with V_{CC} = 0V)
Standard Output
TRI-STATE Output

−0.5V to V_{CC}
−0.5V to +5.5V

Current Applied to Output
in LOW State (Max) twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature

−55°C to +125°C
0°C to +70°C

Military
Commercial

Supply Voltage

+4.5V to +5.5V
+4.5V to +5.5V

Military
Commercial

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = −1 mA (Q ₀ , I/O _n)
		54F 10% V _{CC}	2.4				I _{OH} = −3 mA (I/O _n)
		74F 10% V _{CC}	2.5				I _{OH} = −1 mA (Q ₀ , I/O _n)
		74F 10% V _{CC}	2.4				I _{OH} = −3 mA (I/O _n)
		74F 5% V _{CC}	2.7				I _{OH} = −1 mA (Q ₀ , I/O _n)
		74F 5% V _{CC}	2.7				I _{OH} = −3 mA (I/O _n)
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA (Q ₀ , I/O _n)
		74F 10% V _{CC}		0.5			I _{OL} = 20 mA (Q ₀)
		74F 10% V _{CC}		0.5			I _{OL} = 24 mA (I/O _n)
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V (Non-I/O Inputs)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)	54F 74F		1.0 0.5	mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V (RE, S/P, D _n , CP, MR, OE)
				−1.2	mA	Max	V _{IN} = 0.5V (S)
				−1.8	mA	Max	V _{IN} = 0.5V (SE)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{I/O} = 2.7V (I/O _n)
I _{IL} + I _{OZL}	Output Leakage Current			−650	μA	Max	V _{I/O} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CC}	Power Supply Current		60	90	mA	Max	

AC Electrical Characteristics

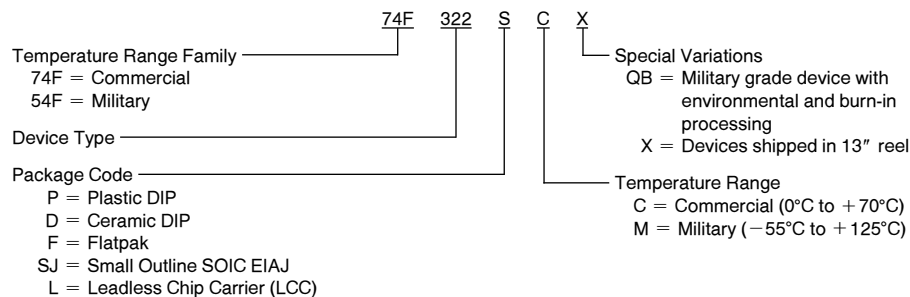
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	70	90		50		70		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O _n	3.5 5.0	7.0 8.5	7.5 11.0	3.5 3.5	9.5 10.0	3.5 5.0	8.5 12.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q ₀	3.5 3.5	7.0 7.0	9.0 8.0	3.5 3.5	11.0 10.0	3.5 3.5	10.0 9.0	
t_{PHL}	Propagation Delay MR to I/O _n	6.0	10.0	13.0	6.0	15.0	6.0	14.0	ns
t_{PHL}	Propagation Delay MR to Q ₀	5.5	7.5	12.0	5.5	14.0	5.5	13.0	ns
t_{PZH} t_{PZL}	Output Enable Time OE to I/O _n	3.0 4.0	6.5 8.5	9.0 11.0	3.0 4.0	12.5 14.5	3.0 4.0	10.0 12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time OE to I/O _n	2.0 2.0	4.5 5.0	6.0 7.0	2.0 2.0	8.0 10.0	2.0 2.0	7.0 8.0	
t_{PZH} t_{PZL}	Output Enable Time S/P to I/O _n	4.5 5.5	8.0 10.0	10.5 14.0	4.5 5.5	13.5 17.0	4.5 5.5	11.5 15.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time S/P to I/O _n	5.0 6.0	9.0 12.0	11.5 15.5	5.0 6.0	16.5 19.5	5.0 6.0	12.5 16.5	

AC Operating Requirements

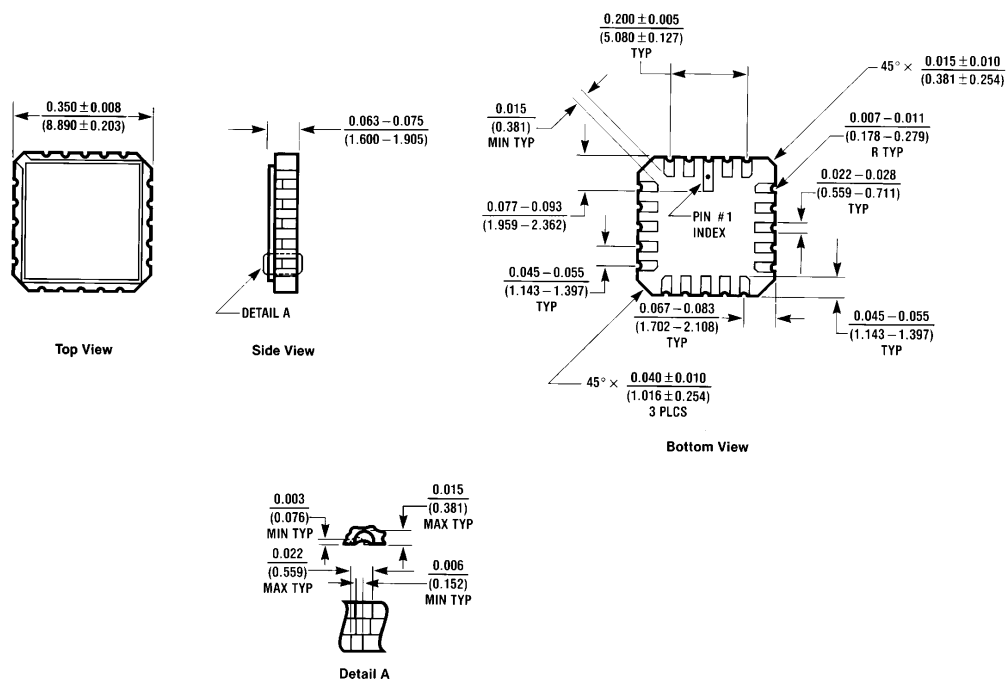
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{RE}}$ to CP	6.0 14.0		14.0 18.0		7.0 16.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{RE}}$ to CP	0 0		0 0		0 0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW D_0, D_1 or I/O_n to CP	6.5 6.5		8.5 8.5		7.5 7.5		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW D_0, D_1 or I/O_n to CP	2.0 2.0		3.0 3.0		3.0 3.0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{SE}}$ to CP	7.0 2.5		9.0 11.0		8.0 3.5		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{SE}}$ to CP	2.0 0.0		2.0 1.0		2.0 0.0		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $S/\overline{\text{P}}$ to CP	11.0 13.5		13.0 21.0		12.0 15.5		ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW S to CP	6.5 9.0		8.5 11.0		7.5 10.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW S or $S/\overline{\text{P}}$ to CP	0 0		1.0 0		0 0		ns
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width, HIGH or LOW	7.0		8.0		7.0		ns
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.5		7.5		6.5		
t_{rec}	Recovery Time $\overline{\text{MR}}$ to CP	8.0		12.0		8.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



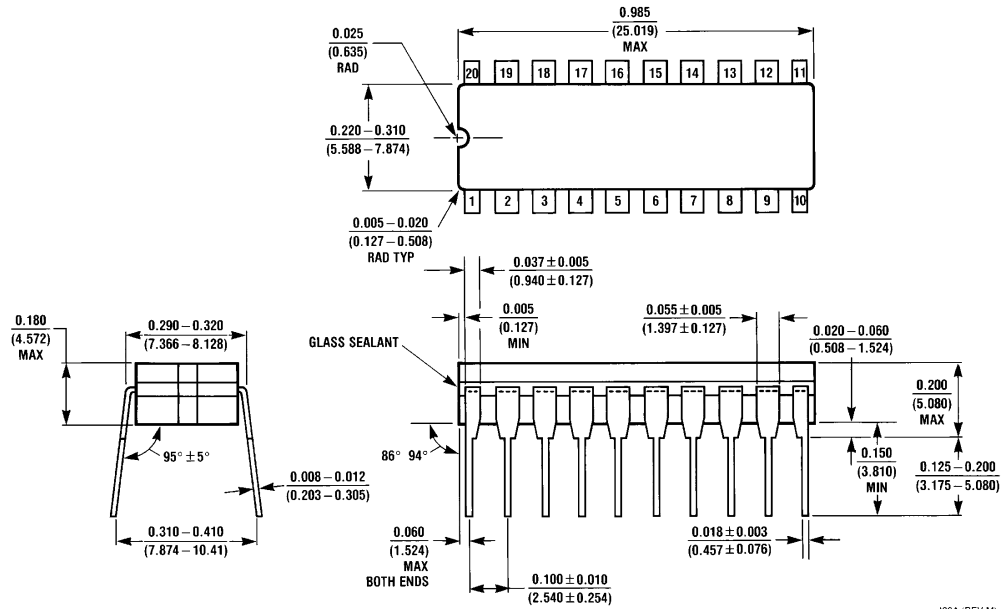
Physical Dimensions inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

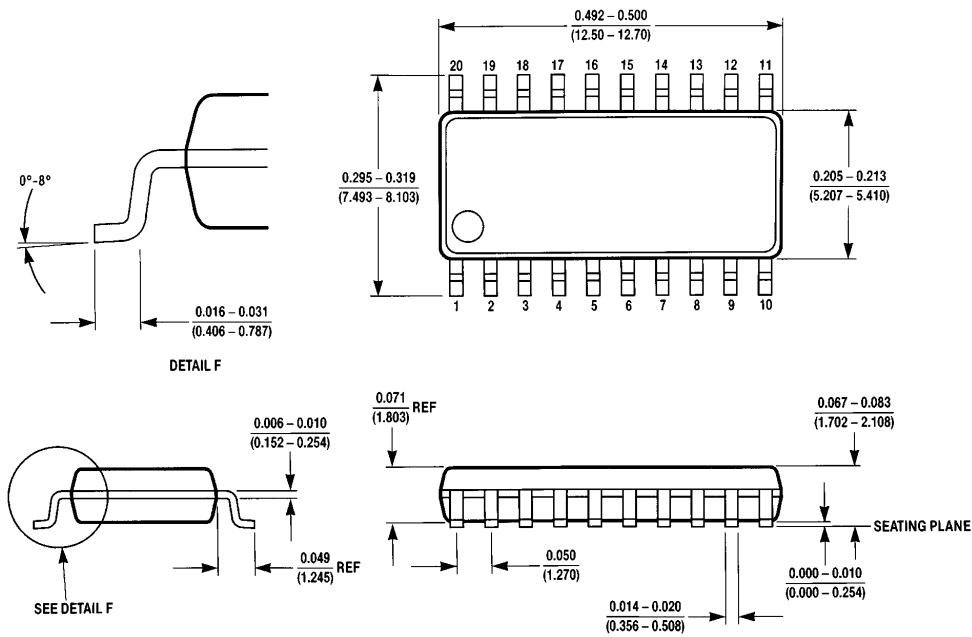
E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)



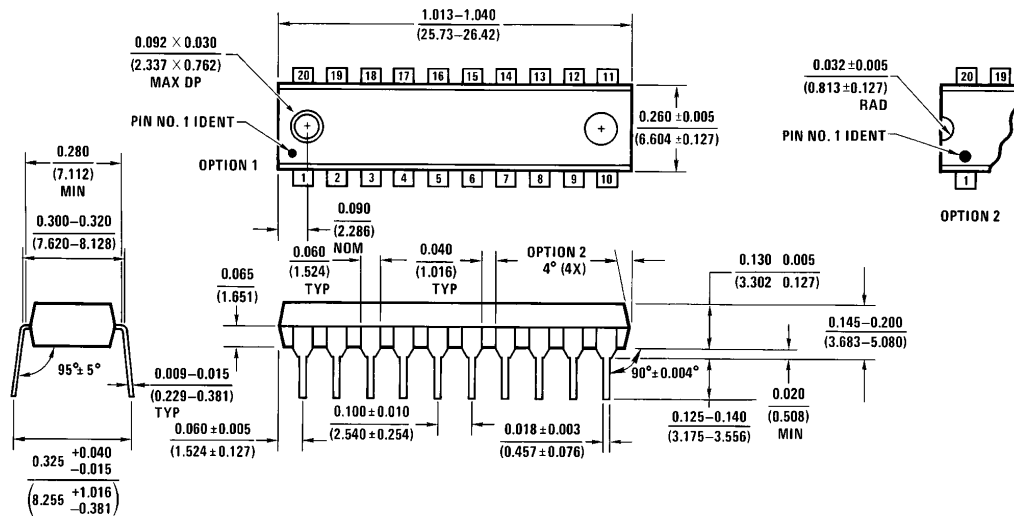
**20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A**

Physical Dimensions inches (millimeters) (Continued)



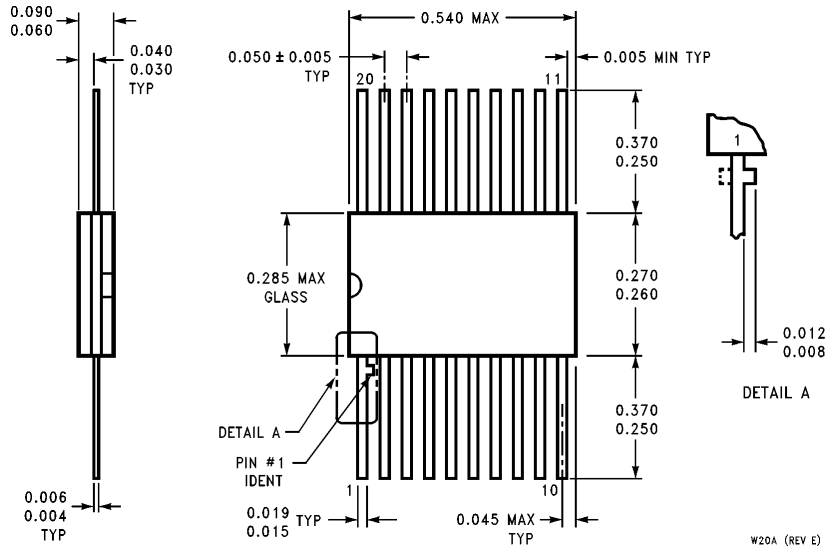
M20D (REV A)

**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D**



N20A (REV G)

**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A**

Physical Dimensions inches (millimeters) (Continued)

20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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