

August 1998

# 100331

## Low Power Triple D Flip-Flop

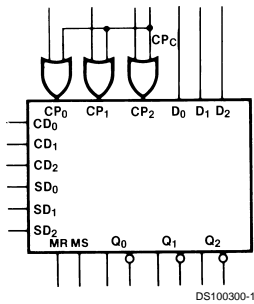
### General Description

The 100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock ( $CP_C$ ), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock ( $CP_n$ ), Direct Set ( $SD_n$ ) and Direct Clear ( $CD_n$ ) inputs. Data enters a master when both  $CP_n$  and  $CP_C$  are LOW and transfers to a slave when  $CP_n$  or  $CP_C$  (or both) go HIGH. The Master Set, Master Reset and individual  $CD_n$  and  $SD_n$  inputs override the Clock inputs. All inputs have 50 k $\Omega$  pull-down resistors.

### Features

- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/function compatible with 100131
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to Standard Microcircuit Drawing (SMD) 5962-9153601

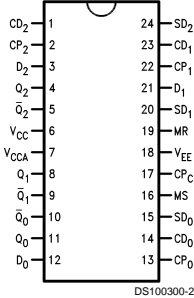
### Logic Symbol



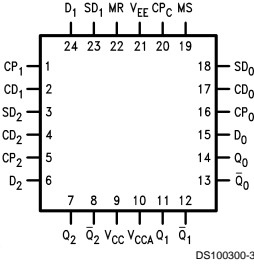
Pin Names	Description
$CP_0$ – $CP_2$	Individual Clock Inputs
$CP_C$	Common Clock Input
$D_0$ – $D_2$	Data Inputs
$CD_0$ – $CD_2$	Individual Direct Clear Inputs
$SD_n$	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
$Q_0$ – $Q_2$	Data Outputs
$\overline{Q_0}$ – $\overline{Q_2}$	Complementary Data Outputs

### Connection Diagrams

24-Pin DIP

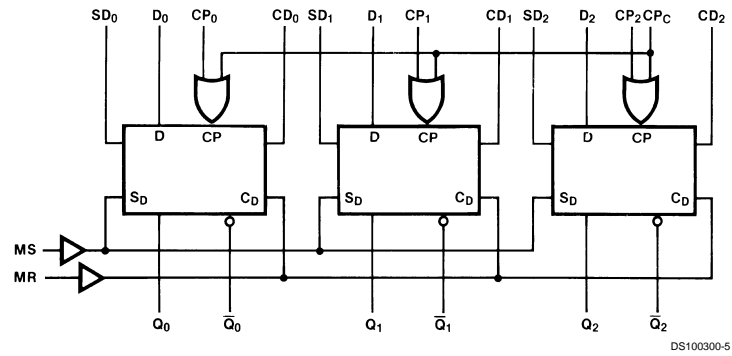


24-Pin Quad Cerpak



100331 Low Power Triple D Flip-Flop

## Logic Diagram



## Truth Tables

### Synchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D <sub>n</sub>	CP <sub>n</sub>	CP <sub>C</sub>	MS SD <sub>n</sub>	MR CD <sub>n</sub>	Q <sub>n</sub> (t + 1)
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	Q <sub>n</sub> (t)
X	H	X	L	L	Q <sub>n</sub> (t)
X	X	H	L	L	Q <sub>n</sub> (t)

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 U = Undefined  
 t = Time before CP Positive Transition  
 t + 1 = Time after CP Positive Transition  
 ↗ = LOW to HIGH Transition

### Asynchronous Operation

(Each Flip-Flop)

Inputs					Outputs
D <sub>n</sub>	CP <sub>n</sub>	CP <sub>C</sub>	MS SD <sub>n</sub>	MR CD <sub>n</sub>	Q <sub>n</sub> (t + 1)
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Maximum Junction Temperature ( $T_J$ )

Ceramic  $+175^{\circ}\text{C}$

Pin Potential to

Ground Pin ( $V_{EE}$ )  $-7.0\text{V}$  to  $+0.5\text{V}$

Input Voltage (DC)

$V_{EE}$  to  $+0.5\text{V}$

Output Current

(DC Output HIGH)

$-50\text{ mA}$

ESD (Note 2)

$\leq 2000\text{V}$

## Recommended Operating Conditions

Case Temperature ( $T_C$ )

Military

$-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Supply Voltage ( $V_{EE}$ )

$-5.7\text{V}$  to  $-4.2\text{V}$

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

## Military Version

### DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$  to  $-5.7\text{V}$ ,  $V_{CC} = V_{CCA} = \text{GND}$ ,  $T_C = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Symbol	Parameter	Min	Max	Units	T <sub>C</sub>	Conditions		Notes
V <sub>OH</sub>	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085	−870	mV	−55°C			
V <sub>OL</sub>	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
V <sub>OHC</sub>	Output HIGH Voltage	−1035		mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to −2.0V	(Notes 3, 4, 5)
		−1085		mV	−55°C			
V <sub>OLC</sub>	Output LOW Voltage	−1610		mV	0°C to +125°C			
		−1555		mV	−55°C			
V <sub>IH</sub>	Input HIGH Voltage	−1165	−870	mV	−55°C to +125°C	Guaranteed HIGH Signal for all Inputs		(Notes 3, 4, 5, 6)
V <sub>IL</sub>	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for all Inputs		(Notes 3, 4, 5, 6)
I <sub>IL</sub>	Input LOW Current	0.50		μA	−55°C to +125°C	V <sub>EE</sub> = −4.2V V <sub>IN</sub> = V <sub>IL</sub> (Min)		(Notes 3, 4, 5)
I <sub>IH</sub>	Input HIGH Current		240	μA	0°C to +125°C	V <sub>EE</sub> = −5.7V V <sub>IN</sub> = V <sub>IH</sub> (Max)		(Notes 3, 4, 5)
			340	μA	−55°C			
I <sub>EE</sub>	Power Supply Current	−130	−50	mA	−55°C to +125°C	Inputs Open		(Notes 3, 4, 5)

**Note 3:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^{\circ}\text{C}$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 4:** Screen tested 100% on each device at  $-55^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+125^{\circ}\text{C}$ , Subgroups, 1, 2, 3, 7 and 8.

**Note 5:** Sampled tested (Method 5005, Table I) on each manufactured lot at  $-55^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$ , and  $+125^{\circ}\text{C}$ , Subgroups A1, 2, 3, 7 and 8.

**Note 6:** Guaranteed by applying specified input condition and testing  $V_{OH}/V_{OL}$ .

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	T <sub>C</sub> = −55°C		T <sub>C</sub> = +25°C		T <sub>C</sub> = +125°C		Units	Conditions		Notes
		Min	Max	Min	Max	Min	Max				
f <sub>max</sub>	Toggle Frequency	400		400		400		MHz	Figures 2, 3		(Note 10)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP <sub>C</sub> to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	Figures 1, 3		(Notes 7, 8, 9)
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP <sub>n</sub> to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CD <sub>n</sub> , SD <sub>n</sub> to Output	0.50	2.20	0.60	2.00	0.50	2.40	ns	CP <sub>n</sub> , CP <sub>C</sub> = L	Figures 1, 4	
t <sub>PLH</sub> t <sub>PHL</sub>		0.50	2.40	0.60	2.10	0.50	2.50		CP <sub>n</sub> , CP <sub>C</sub> = H		
t <sub>PLH</sub> t <sub>PHL</sub>		0.70	2.70	0.80	2.60	0.80	2.90		CP <sub>n</sub> , CP <sub>C</sub> = L		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay MS, MR to Output	0.70	2.90	0.80	2.80	0.80	3.10	ns	CP <sub>n</sub> , CP <sub>C</sub> = H		
t <sub>TLH</sub> t <sub>THL</sub>		Transition Time 20% to 80%, 80% to 20%	0.20	1.40	0.20	1.40	0.20		1.40	ns	
t <sub>s</sub>	Setup Time								Figure 5		(Note 10)
	D <sub>n</sub>	1.00		0.80		0.90		ns			
	CD <sub>n</sub> , SD <sub>n</sub> (Release Time)	1.50		1.30		1.60			Figure 4		
	MS, MR (Release Time)	2.50		2.30		2.50					
t <sub>h</sub>	Hold Time D <sub>n</sub>	1.50		1.30		1.60		ns	Figure 5		
t <sub>pw(H)</sub>	Pulse Width HIGH										
	CP <sub>n</sub> , CP <sub>C</sub> , CD <sub>n</sub> , SD <sub>n</sub> , MR, MS	2.00		2.00		2.00		ns	Figures 3, 4		

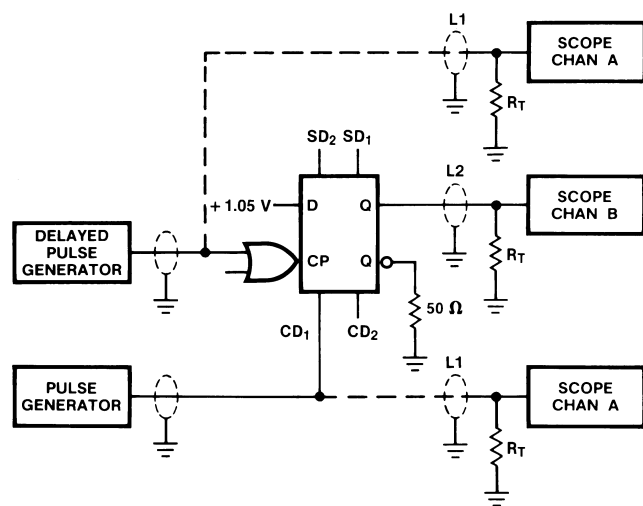
**Note 7:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 8:** Screen tested 100% on each device at  $+25^\circ C$ . Temperature only, Subgroup A9.

**Note 9:** Sample tested (Method 5005, Table I) on each Mfg. lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$ , and  $-55^\circ C$  Temp., Subgroups A10 and A11.

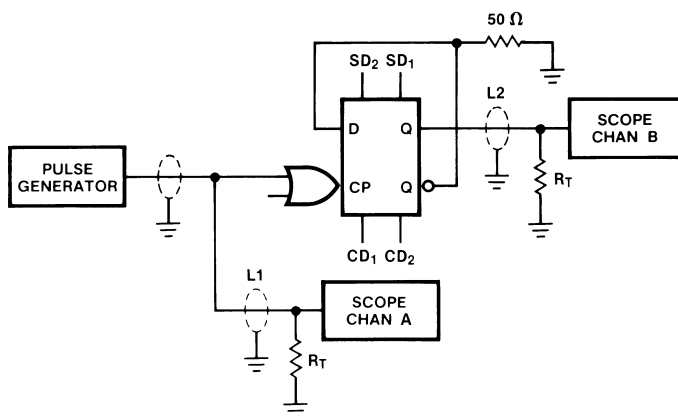
**Note 10:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$  and  $-55^\circ C$  Temperature (design characterization data).

## Test Circuits



DS100300-6

FIGURE 1. AC Test Circuit



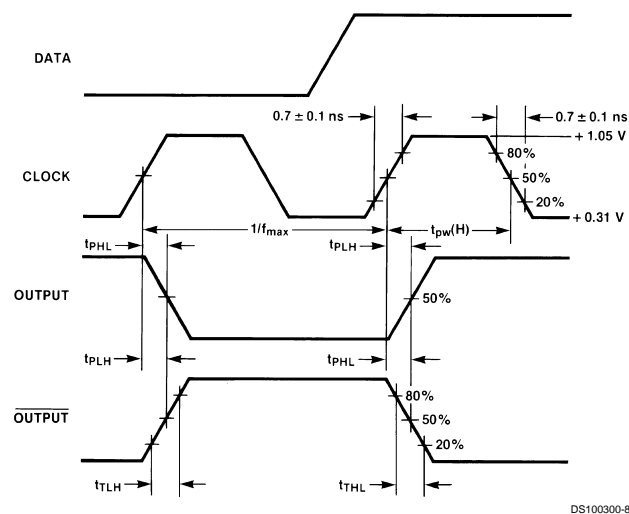
DS100300-7

### Notes:

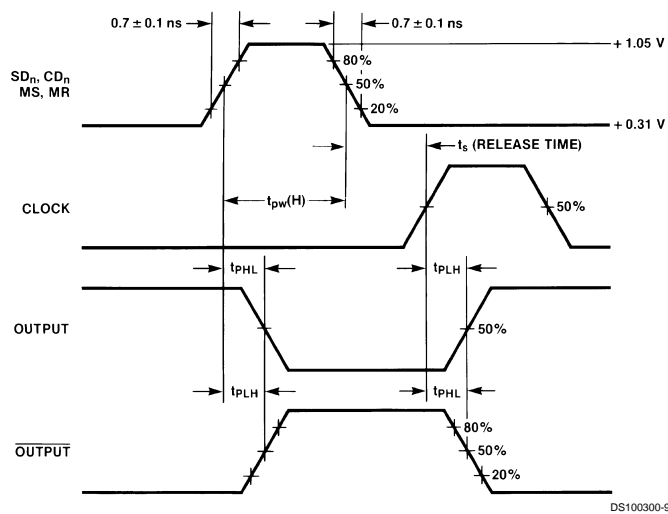
$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$   
 $L1$  and  $L2$  = Equal length  $50\Omega$  impedance lines  
 $R_T = 50\Omega$  terminator internal to scope  
 Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$   
 All unused outputs are loaded with  $50\Omega$  to GND  
 $C_L$  = Fixture and stray capacitance  $\leq 3 pF$

FIGURE 2. Toggle Frequency Test Circuit

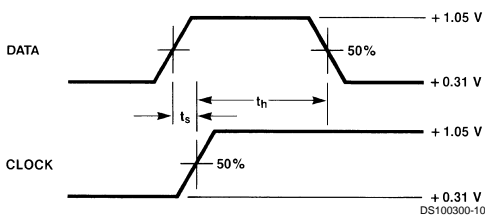
## Switching Waveforms



**FIGURE 3. Propagation Delay (Clock) and Transition Times**



**FIGURE 4. Propagation Delay (Resets)**



**FIGURE 5. Data Setup and Hold Time**

**Note 11:**  $t_s$  is the minimum time before the transition of the clock that information must be present at the data input.

**Note 12:**  $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

inches (millimeters) unless otherwise noted



**24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)**  
**NS Package Number J24E**



**24-Lead Quad Cerpak (F)**  
**NS Package Number W24B**

#### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

[www.national.com](http://www.national.com)

**National Semiconductor Europe**

Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**

Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**

Tel: 81-3-5620-6175  
Fax: 81-3-5620-6179