

# LP3931 Dual RGB LED Driver with High Current Boost DC-DC Converter

## **General Description**

The LP3931 is a RGB LED driver with high current boost DC-DC converter designed for portable wireless applications. It contains 2 sets of RGB LED drivers that are PWMdriven with programmable color, intensity and blinking patterns. They additionally feature a FLASH function to support picture taking with camera-enabled cellular phones.

An efficient magnetic boost DC/DC converter provides the required bias, operating from a single Li-Ion battery. The DC/DC converter output voltage is user programmable for adapting to different LED types and for efficiency optimization.

All functions are software controllable through the SPI interface and internal registers.

## **Features**

- High Efficiency Programmable 300 mA Magnetic Boost DC-DC converter
- 2 separately controlled PWM RGB LED drivers with programmable color, brightness, turn on/off slopes and blinking patterns
- FLASH function with up to 6 outputs, each up to 120 mA
- Functions software controlled through SPI interface
- Additional LED on/off and dimming hardware control
- Programmable low current Standby mode
- Low voltage digital interface down to 1.8V
- Space efficient 24-pin LLP package

# Applications

- GSM Cellular Phones
- WCDMA, CDMA and CDMA2000 Phones
- PHS and PDC Cellular Phone



August 2004



**Note:** The actual physical placement of the package marking will vary from part to part. The package marking "XY" designates the date code. "UZ" and "TT" are NSC internal codes for die manufacturing and assembly traceability. Both will vary considerably.

## **Ordering Information**

Order Number	Package Marking	Supplied As
LP3931ISQ	LP3931ISQ	1000 units, Tape-and-Reel
LP3931ISQX	LP3931ISQ	2500 units, Tape-and-Reel

Pin De	escription			
Pin #	Name	Туре	Description	
1	G2	Output	Open Drain, Green LED2	
2	R2	Output	Open Drain, Red LED2	
3	GND_RGB	Ground	RGB Driver Ground	
4	R1	Output	Open Drain, Red LED1	
5	G1	Output	Open Drain, Green LED1	
6	B1	Output	Open Drain, Blue LED1	
7	GND_BOOST	Ground	Power Switch Ground	
8	SW	Output	Open Drain, Boost Converter Power Switch	
9	V <sub>DD2</sub>	Power	Supply Voltage for Internal Digital Circuits	
10	GND2	Ground	Ground	
11	FB	Input	Boost Converter Feedback	
12	V <sub>REF</sub>	Output	Internal Reference Bypass Capacitor	
13	SO	Logic Output	SPI Serial Data Out	
14	SI	Logic Input	SPI Serial Data Input	
15	SS	Logic Input	SPI Slave Select	
16	SCK	Logic Input	SPI Clock	
17	PWM_LED	Input	LED Control for On/Off or PWM Dimming	
18	NRST	Logic Input	Low Active Reset Input	
19	V <sub>DDIO</sub>	Power	Supply Voltage for Logic IO Signals	
20	RT	Input	Oscillator Resistor	
21	GND3	Ground	Ground	
22	V <sub>DD1</sub>	Power	Supply Voltage for Internal Analog Circuits	
23	GND1	Ground	Ground	
24	B2	Output	Open Drain, Blue LED2	

## Absolute Maximum Ratings (Notes 1,

#### 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V (SW, FB, R1- 2, G1-2, B1-2) pins:	
Voltage to GND (Notes 3, 4)	-0.3V to +7.2V
$V_{DD1}, V_{DD2}, V_{DD_{IO}}$	-0.3V to +6.0V
Voltage on Logic Pins	$-0.3V$ to $V_{DD_{IO}}$
	+0.3V, with 6.0V max
I (R1, G1, B1, R2, G2, B2)	
(Note 5)	150 mA
I (V <sub>REF</sub> )	10 µA
Continuous Power Dissipation	
(Note 6)	Internally Limited
Junction Temperature (T <sub>J-MAX</sub> )	125°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature	
(Reflow soldering, 3 times)	
(Note 7)	240°C

ESD Rating (Note 8)	
Human Body Model:	2 kV
Machine Model:	200V

### Operating Ratings (Notes 1, 2)

V (SW, FB, R1-2, G1-2, B1-2)	3.0V to 6.0V
V <sub>DD1</sub> , V <sub>DD2</sub> (Note 4)	2.65V to 2.9V
V <sub>DD_IO</sub>	1.8V to $V_{DD1,2}$
Recommended Load Current	0 mA to 300 mA
Junction Temperature (T <sub>J</sub> ) Range	-40°C to +125°C
Ambient Temperature (T <sub>A</sub> ) Range	
(Note 9)	–40°C to +85°C

## **Thermal Properties**

Junction-to-Ambient Thermal Resistance $(\theta_{JA})$ ,	
SQA24A Package (Note 10)	39°C/W

### Electrical Characteristics (Notes 2, 11)

Limits in standard typeface are for  $T_J = 25$ °C. Limits in **boldface** type apply over the operating ambient temperature range (-40°C  $\leq T_J \leq +85$ °C). Unless otherwise noted, specifications apply to the LP3931 Typical Application Circuit (pg. 1) with:  $V_{DD1} = V_{DD2} = V_{DD10} = 2.775V$ ,  $C_{VDD1} = C_{VDD2} = C_{VDD10} = 0.1 \mu$ F,  $C_{OUT} = C_{IN} = 10 \mu$ F,  $C_{VREF} = 0.1 \mu$ F,  $L_1 = 10 \mu$ H,  $R_T = 82k$  (Note 12).

Symbol	Parameter	Condition	Min	Тур	Мах	Units
I <sub>DD</sub>	Standby Supply Current	NSTBY = L (register)		-	E	
	$(V_{DD1} \text{ and } V_{DD2} \text{ current})$	SCK, SS, SI, NRST = H		1	5	μΑ
	No-Load Supply Current	NSTBY = H (reg.)				
	$(V_{DD1} \text{ and } V_{DD2} \text{ current, boost off})$	EN_BOOST = L (reg.)		170	250	μA
		SCK, SS, SI, NRST = H				
	Full Load Supply Current	NSTBY = H (reg.)				
	$(V_{DD1} \text{ and } V_{DD2} \text{ current, boost on})$	EN_BOOST = H (reg.)		4		m۸
		SCK, SS, SI, NRST = H		1		
		All Outputs Active				
I <sub>DD_IO</sub>	V <sub>DD_IO</sub> Standby Supply Current	NSTBY = L (reg.)		4		
		SCK, SS, SI, NRST = H		1		μΑ
	V <sub>DD IO</sub> Supply Current	1 MHz SCK Frequency		00		
		$C_L = 50 \text{ pF}$ at SO Pin		20		μΑ
V <sub>REF</sub>	Reference Voltage (Note 13)	$I(V_{REF}) \le 1 \text{ nA},$	1.205	1.23	1.255	V
		Test Purposes Only	-2		+2	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins (GND1-3, GND\_BOOST, GND\_RGB).

Note 3: Battery/Charger voltage should be above 6V no more than 10% of the operational lifetime.

**Note 4:** Voltage tolerance of LP3931 above 6.0V relies on fact that  $V_{DD1}$  and  $V_{DD2}$  (2.775V) are available (ON) at all conditions. If  $V_{DD1}$  and  $V_{DD2}$  are not available (ON) at all conditions, National Semiconductor does not guarantee any parameters or reliability for this device.

Note 5: The total load current of the boost converter should be limited to 300 mA.

Note 6: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at  $T_J = 160^{\circ}C$  (typ.) and disengages at  $T_J = 140^{\circ}C$  (typ.).

Note 7: For detailed package and soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Leadframe Package (LLP).

Note 8: The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7.

### Electrical Characteristics (Notes 2, 11) (Continued)

**Note 9:** In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ( $T_{A-MAX}$ ) is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125$ °C), the maximum power dissipation of the device in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the part/package in the application ( $\theta_{JA}$ ), as given by the following equation:  $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$ .

Note 10: Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 11: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 12: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

Note 13: V<sub>REF</sub> pin (Bandgap reference output) is for internal use only. A capacitor should always be placed between V<sub>REF</sub> and GND1.

# **Block Diagram**





## Modes of Operation

**RESET:** In the RESET mode all the internal registers are reset to the default values (Boost output register 3Fh (5.0V), all other registers 00h). Reset is entered always if input NRST is LOW or internal Power On Reset is active.

**STANDBY:** The STANDBY mode is entered if the register bit NSTBY is LOW and Reset is not active. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after power up.

**STARTUP:** INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (V<sub>REF</sub>, Bias, Oscillator etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. Thermal shutdown (THSD) disables the chip operation and Startup mode is entered until *no* thermal shutdown event is present.

**BOOST STARTUP:** Soft start for boost output is generated in the BOOST STARTUP mode. In this mode the boost output is raised in PFM mode during the 10 ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN\_BOOST is HIGH or from Normal mode when EN\_BOOST is written HIGH.

# **NORMAL:** During NORMAL mode the user controls the chip using the *Control Registers*. The registers can be written in any sequence and any number of bits can be altered in a register in one write.



# **Logic Interface Characteristics**

 $(1.8V \le V_{DD\_IO} \le V_{DD1,2})$ 

Symbol	Parameter	Conditions	Min	Тур	Max	Units
LOGIC INPL	JTS SS, SI, SCK, PWM_I	ED				
V <sub>IL</sub>	Input Low Level				0.5	V
V <sub>IH</sub>	Input High Level		V <sub>DD_IO</sub> – 0.5			V
l <sub>l</sub>	Logic Input Current		-1.0		1.0	μA
f <sub>scк</sub>	Clock Frequency	V <sub>DD_IO</sub> = 2.775V			13	MHz
LOGIC INPL	JT NRST					
V <sub>IL</sub>	Input Low Level				0.5	V
V <sub>IH</sub>	Input High Level		1.5			V
l <sub>i</sub>	Logic Input Current		-1.0		1.0	μA
t <sub>NRST</sub>	Reset Pulse Width		10			μs
LOGIC OUT	PUT SO				-	
V <sub>OL</sub>	Output Low Level	I <sub>SO</sub> = 3 mA		0.3	0.5	V
V <sub>OH</sub>	Output High Level	I <sub>SO</sub> = – 3 mA	V <sub>DD_IO</sub> – 0.5	V <sub>DD_IO</sub> – 0.3		V

## **SPI Interface**

LP3931 is compatible with the SPI serial bus specification and it operates as a slave. The transmission consists of 16-bit Write and Read Cycles. One cycle consists of 7 Address bits, 1 Read/Write (R/W) bit and 8 Data bits. R/W bit high state defines a Write Cycle and low defines a Read Cycle. SO output is normally in high-impedance state and it is active only when Data is sent out during a Read Cycle. A pull-up or pull-down resistor may be needed in SO line if a floating logic signal can cause unintended current consumption in the input where SO is connected. The Address and Data are transmitted MSB first. The Slave Select signal SS must be low during the Cycle transmission. SS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the SCK clock signal, while data is clocked out on the falling edge of SCK.





# **SPI Timing Parameters**

 $V_{DD1,2} = V_{DD_{-10}} = 2.775V$ 

Symbol	Dexemptor	Li	Unito		
Symbol	Parameter	Min	Max	Units	
1	Cycle Time	70		ns	
2	Enable Lead Time	35		ns	
3	Enable Lag Time	35		ns	
4	Clock High Time	35		ns	
5	Clock Low Time	35		ns	
6	Data Setup Time	0		ns	
7	Data Hold Time	20		ns	
8	Data Access Time	0	20	ns	
9	Disable Time		10	ns	
10	Data Valid		20	ns	
11	Data Hold Time	0		ns	
12	SS Inactive Time	10		ns	
late: Data guaranteed by simulation					

Note: Data guaranteed by simulation.

# Magnetic Boost DC/DC Converter

The LP3931 Boost DC/DC Converter generates a 4.1V–5.3V supply voltage for the LEDs from single Li-Ion battery (3V...4.5V). The output voltage is controlled with an 8-bit register in 9 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter switching frequency is 1 MHz when timing resistor RT is 82 k $\Omega$ .

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The control changes the resistor divider in the feedback loop.

The following figure shows the boost topology with the protection circuitry. Three different protection schemes are implemented:

- 1. Over voltage protection, limits the maximum output voltage
  - Keeps the output below breakdown voltage.
  - Prevents boost operation if battery voltage is much higher than desired output.
- 2. Over current protection, limits the maximum inductor current
  - Voltage over switching NMOS is monitored; too high voltages turn the switch off.
- 3. Duty cycle limiting, done with digital control.

#### Magnetic Boost DC/DC Converter (Continued) **Boost Converter Topology** 1MHz clock Duty control VOUT V<sub>IN</sub> m ፓፓር የ ᡗ᠋᠋ᡘ SW FΒ OVPCOMP R S R RESETCOMP R R ≶ ERRORAMP LOOPC ΛΛΛ SLOPER **OLPCOMP** 20117310

# Magnetic Boost DC/DC Converter Electrical Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Units
I <sub>LOAD</sub>	Load Current	$\begin{array}{l} 3.0V \leq V_{\text{IN}} \leq 4.5V \\ V_{\text{OUT}} \ (\text{FB}) = 5V \end{array}$	0		300	mA
V <sub>FB</sub>	Voltage Accuracy at FB Pin (Boost Converter Output Voltage Accuracy)	$\begin{array}{l} 1 \mbox{ mA} \leq I_{SW} \leq 300 \mbox{ mA} \\ 3.0V \leq V_{IN} \leq V \mbox{ (FB)} - 0.5 \\ V \mbox{ (FB)} = 5V \end{array}$	-5		+5	%
	Voltage at FB Pin (Boost Converter Output Voltage)	$\begin{array}{l} 1 \mbox{ mA} \leq I_{SW} \leq 300 \mbox{ mA} \\ 3.0V < V_{IN} < 5V + \\ V_{(SCHOTTKY)} \end{array}$		5		v
		$1 \text{ mA} \leq I_{SW} \leq 300 \text{ mA}$ $V_{IN} > 5V + V_{(SCHOTTKY)}$		$V_{IN} - V_{(SCHOTTKY)}$		V
RDS <sub>ON</sub>	Switch ON Resistance	V <sub>DD1,2</sub> = 2.775V, I <sub>SW</sub> = 0.5A		0.4	0.7	Ω
f <sub>PWF</sub>	PWM Mode Switching Frequency	RT = 82 kΩ		1		MHz
	Frequency Accuracy	$\begin{array}{l} 2.65 \leq V_{\text{DD1,2}} \leq 2.9 \\ \text{RT} = 82 \; k\Omega \end{array}$	-6 <b>-9</b>	±3	+6 <b>+9</b>	%
t <sub>startup</sub>	Startup Time	From NSTBY and EN_BOOST 0 -> 1 transition		25		ms
I <sub>CL_OUT</sub>	SW Pin Current Limit		670 <b>530</b>	800	915 <b>995</b>	mA

# **Boost Standby Mode**

User can set the Boost Converter to STANDBY mode by writing the register bit EN\_BOOST low. When EN\_BOOST is written high, the converter waits for 10 ms for the internal voltages and currents to stabilize and then starts for 10 ms in PFM mode and then goes to PWM mode.

# **Boost Output Voltage Control**

User can control the boost output voltage by 8-bit boost output register as follows:

Register 0DH Boost Output [7:0]	BOOST Output Voltage (typical)
0000 0000	4.15
0000 0001	4.30
0000 0011	4.40
0000 0111	4.55
0000 1111	4.70
0001 1111	4.85
0011 1111	5.00 Default
0111 1111	5.15
1111 1111	5.30





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# **Boost Converter Typical Performance Characteristics** $V_{IN} = 3.6V$ , $V_{OUT} = 5.0V$ if not otherwise stated.





Boost Frequency vs RT Resistor



# **Boost Converter Typical Performance Characteristics** $V_{IN} = 3.6V$ , $V_{OUT} = 5.0V$ if not otherwise stated. (Continued)



TIME (500 µs/DIV)

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Boost Typical Waveforms at 100 mA Load







## Multiple RGB LED Drivers

The RGB driver has six outputs that can independently drive 2 separate RGB LEDs or six LEDs of any kind. User has control over the following parameters separately for each LED:

- ON and OFF (start and stop time in blinking cycle)
- **DUTY** (PWM brightness control)
- SLOPE (dimming slope)
- ENABLE (output enable control)

The main blinking cycle is controlled with 2-bit CYCLE control (0.25 / 0.5 / 1.0 / 2.0s).



RGB\_START is the master enable control for the whole RGB function. The internal PWM and blinking control can be disabled by setting the RGB\_PWM control LOW. In this case the individual enable controls can be used to switch outputs on and off. PWM\_LED input can be used for external hardware PWM control.

In the normal PWM mode the R, G and B switches are controlled in 3 phases (one phase per driver). During each phase the peak current set by the external ballast resistor is driven through the LED for the time defined by DUTY setting (0  $\mu$ s-50  $\mu$ s). As a time averaged current this means 0%-33% of the peak current. The PWM period is 150  $\mu$ s and the pulse frequency is 6.67 kHz in normal mode.



In the FLASH mode all the outputs are controlled in one phase and the PWM period is 50  $\mu$ s. The time averaged FLASH mode current is three times the normal mode current at the same DUTY value.

Blinking can be controlled separately for each output.

ON and OFF times define, when a LED turns on and off within the blinking cycle. When both ON and OFF are 0, the LED is on and doesn't blink. If ON equals OFF but is not 0, the LED is turned off.



Application Note AN1291 describes in detail the RGB driver functionality of LP3933. The RGB driver in LP3931 is identical with LP3933.

### **RGB Driver Electrical Characteristics** (R1, G1, B1, R2, G2, B2 outputs)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
R <sub>DS-ON</sub>	ON Resistance			3.5	6	Ω
ILEAKAGE	Off State Leakage Current	$V_{FB} = 5V$ , LED driver off		0.03	1	μΑ
I <sub>MAX</sub>	Maximum Sink Current	(Note 5)			120	mA
T <sub>SMAX</sub>	Maximum Slope Period	At Maximum Duty Setting		0.93		s
T <sub>SMIN</sub>	Minimum Slope Period	At Maximum Duty Setting		31		ms
T <sub>SRES</sub>	Slope Resolution	At Maximum Duty Setting		62		ms
T <sub>START/STOP</sub>	Start/Stop Resolution	Cycle 1s		1/16		s
Duty	Duty Step Size			1/16		
T <sub>BLINK</sub>	Blinking Cycle Accuracy		-6	±3	+6	%
D <sub>CYCF</sub>	Duty Cycle Range	EN_FLASH = 1	0		99.6	%
D <sub>CYC</sub>	Duty Cycle Range	EN_FLASH = 0	0		33.2	%
D <sub>RESF</sub>	Duty Resolution	EN_FLASH = 1 (4-bit)		6.64		%
D <sub>RES</sub>	Duty Resolution	EN_FLASH = 0 (4-bit)		2.21		%
F <sub>PWMF</sub>	PWM Frequency	EN_FLASH = 1		20		kHz
F <sub>PWM</sub>	PWM Frequency	EN_FLASH = 0		6.67		kHz

# RGB LED PWM Control (Note 14)

R1DUTY[3:0] G1DUTY[3:0] B1DUTY[3:0] B2DUTY[2:0]	DUTY sets the brightness of the LED by adjusting the duty cycle of the PWM driver. The minimum DUTY cycle is 0% [0000] and the maximum in the Flash mode is ~ 100% [1111] of peak pulse current. The peak pulse current is determined by the external resistor, LED forward voltage drop and the boost voltage. In normal mode the maximum duty cycle is 23%
G2DUTY[3:0] B2DUTY[3:0]	volage. In normal mode the maximum duty cycle is 35 %.
R1SLOPE[3:0]	SLOPE sets the turn-on and turn-off slopes. Fastest slope is set by [0000] and slowest by [1111]. SLOPE
G1SLOPE[3:0]	changes the duty cycle at constant, programmable rate. For each slope setting the maximum slope time
B1SLOPE[3:0]	appears at maximum DUTY setting. When DUTY is reduced, the slope time decreases proportionally. For
R2SLOPE[3:0]	example, in case of maximum DUTY, the sloping time can be adjusted from 31 ms [0000] to 930 ms
G2SLOPE[3:0]	[1111]. For 50% DUTY [0111] the sloping time is 14 ms [0000] to 434 ms [1111]. The blinking cycle has
B2SLOPE[3:0]	no effect on SLOPE.
R1ON[3:0]	ON sets the beginning time of the turn-on slope. The on-time is relative to the selected blinking cycle
G1ON[3:0]	length. On-setting N (N = 0 $-$ 15) sets the on-time to N/16 * cycle length.
B1ON[3:0]	
R2ON[3:0]	
G2ON[3:0]	
B2ON[3:0]	
R1OFF[3:0]	OFF sets the beginning time of the turn-off slope. Off-time is relative to the blinking cycle length in the
G1OFF[3:0]	same way as the on-time.
B1OFF[3:0]	
R2OFF[3:0]	
G2OFF[3:0]	
B2OFF[3:0]	
	If ON = 0, OFF = 0 and RGB_PWM = 1, then the RGB outputs are continuously on (no blinking), the
	DUTY setting controls the brightness and the SLOPE control is ignored.
	If ON and OFF are the same, but not 0, the RGB outputs are turned off.
CYCLE[1:0]	CYCLE sets the blinking cycle: [00] for 0.25s, [01] for 0.5s, [10] for 1s and [11] for 2s. CYCLE effects to all RGB LEDs.

RGB LED PWM Control (Note 14) (Continued)				
RSW1	Enable for R1 switch			
GSW1	Enable for G1 switch			
BSW1	Enable for B1 switch			
RSW2	Enable for R2 switch			
GSW2	Enable for G2 switch			
BSW2	Enable for B2 switch			
RGB_START	Master Switch:			
	$RGB\_START = 0 \rightarrow RGB OFF$			
	RGB_START = 1 $\rightarrow$ RGB ON, starts the new cycle from t = 0			
RGB_PWM	RGB_PWM = $0 \rightarrow$ RSW, GWS and BSW control directly the RGB outputs (on/off control only)			
	RGB_PWM = 1 $\rightarrow$ Normal PWM RGB functionality (duty, slope, on/off times, cycle)			
EN_FLASH1	Flash Mode enable controls for RGB1 and RGB2. In Flash mode (EN_FLASH = 1) RGB outputs are			
EN_FLASH2	PWM controlled simultaneously, not in 3-phase system as in the Normal Mode.			
R1_PWM	XX_PWM = 0 $\rightarrow$ External PWM control from PWM_LED pin is disabled			
G1_PWM	XX_PWM = 1 $\rightarrow$ External PWM control from PWM_LED pin is enabled			
B1_PWM	Internal PWM control (DUTY) can be used independently of external PWM control. External PWM has			
R2_PWM	the same effect on all enabled outputs.			
G2_PWM				
B2_PWM				

PWM\_LED input can be used as a direct on/off or PWM brightness control for selected White LED or RGB outputs. For example it can trigger the Flash using a Flash signal from the camera. If PWM\_LED input is not used, it must be tied to V<sub>DD\_IO</sub>.

Note 14: Application Note 1291, "Driving RGB LEDs Using LP3933 Lighting Management System" contains a thorough description of the RGB driver functionality including programming examples. It applies to LP3931, too.

# Recommended External Components

#### OUTPUT CAPACITOR, COUT

The output capacitor  $C_{OUT}$  directly affects the magnitude of the output ripple voltage so  $C_{OUT}$  should be carefully selected. In general, the higher the value of  $C_{OUT}$ , the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower  $V_{OUT}$  ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower  $V_{OUT}$  ripple magnitude than the tantalums of the same value. However, the dv/dt of the  $V_{OUT}$  ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

#### INPUT CAPACITOR, C<sub>IN</sub>

The input capacitor  $C_{\rm IN}$  directly affects the magnitude of the input ripple voltage and to a lesser degree the  $V_{\rm OUT}$  ripple. A higher value  $C_{\rm IN}$  will give a lower  $V_{\rm IN}$  ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

#### OUTPUT DIODE, DOUT

A Schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode should be larger than the peak inductor current (1A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

#### INDUCTOR, L

The LP3931's high switching frequency enables the use of the small surface mount inductor. A 10  $\mu$ H shielded inductor is suggested. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation (~1A). Less than 100 m $\Omega$  ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the OUT pin as close to the IC as possible. Examples of suitable inductors are TDK types LLF4017T-100MR90C and VLF4012AT-100MR79 and Coilcraft type DO3314T-103 (unshielded).

# Recommended External Components (Continued)

List of External Components								
Symbol	Symbol Explanation	Value	Unit	Recommended Type				
C <sub>VDD1</sub>	V <sub>DD1</sub> Bypass Capacitor	100	nF	Ceramic, X7R				
C <sub>VDD2</sub>	V <sub>DD2</sub> Bypass Capacitor	100	nF	Ceramic, X7R				
C <sub>OUT</sub>	Output Capacitor from FB to GND	10	μF	Ceramic, X7R/Y5V				
C <sub>IN</sub>	Input Capacitor from Battery Voltage to GND	10	μF	Ceramic, X7R/Y5V				
C <sub>VDDIO</sub>	V <sub>DD_IO</sub> Bypass Capacitor	100	nF	Ceramic, X7R				
RT	Oscillator Frequency Bias Resistor	82	kΩ	1% (Note 15)				
RSO	SO Output Pull-up Resistor	100	kΩ					
C <sub>VREF</sub>	Reference Voltage Capacitor, between $V_{\text{REF}}$ and GND	100	nF	Ceramic, X7R				
L <sub>BOOST</sub>	Boost Converter Inductor	10	μH	Shielded, Low ESR, I <sub>SAT</sub> ~1A				
D <sub>OUT</sub>	Rectifying Diode, V <sub>F</sub> @ Maxload	0.3	V	Schottky Diode				
RGB1	RGB LED1							
RGB2	RGB LED2			Llear Defined				
$R_{R1}, R_{G1}, R_{B1}$	Current Limit Resistor	- User Defined - (See Application Note AN-1291 for resistor size calculation						
$R_{R2}, R_{G2}, R_{B2}$	Current Limit Resistor							
LEDs	White LEDs	]						

Note 15: Resistor RT accuracy specification change from  $1\% \rightarrow 5\%$  will be seen on timing accuracy of RGB block. Also the boost converter's switching frequency will be affected.

# **Control Registers**

Control registers and register bits are shown in the following table.

ADDR	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
00H	RGB Control register1	rgb pwm	rgb start	rsw1	gsw1	bsw1	rsw2	gsw2	bsw2
01H	red1_on_off	r1_on[3]	r1_on[2]	r1_on[1]	r1_on[0]	r1_off[3]	r1_off[2]	r1_off[1]	r1_off[0]
02H	green1_on_off	g1_on[3]	g1_on[2]	g1_on[1]	g1_on[0]	g1_off[3]	g1_off[2]	g1_off[1]	g1_off[0]
03H	blue1_on_off	b1_on[3]	b1_on[2]	b1_on[1]	b1_on[0]	b1_off[3]	b1_off[2]	b1_off[1]	b1_off[0]
04H	r1slope, r1duty	r1slope[3]	r1slope[2]	r1slope[1]	r1slope[0]	r1duty[3]	r1duty[2]	r1duty[1]	r1duty[0]
05H	g1slope, g1duty	g1slope[3]	g1slope[2]	g1slope[1]	g1slope[0]	g1duty[3]	g1duty[2]	g1duty[1]	g1duty[0]
06H	b1slope, b1duty	b1slope[3]	b1slope[2]	b1slope[1]	b1slope[0]	b1duty[3]	b1duty[2]	b1duty[1]	b1duty[0]
07H	RGB Control register2	cycle[1]	cycle[0]	r1_pwm	g1_pwm	b1_pwm	r2_pwm	g2_pwm	b2_pwm
0BH	enables		nstby	en_boost	en_flash1	en_flash2			
0DH	boost output	boost[7]	boost[6]	boost[5]	boost[4]	boost[3]	boost[2]	boost[1]	boost[0]
2AH	red2_on_off	r2_on[3]	r2_on[2]	r2_on[1]	r2_on[0]	r2_off[3]	r2_off[2]	r2_off[1]	r2_off[0]
2BH	green2_on_off	g2_on[3]	g2_on[2]	g2_on[1]	g2_on[0]	g2_off[3]	g2_off[2]	g2_off[1]	g2_off[0]
2CH	blue2_on_off	b2_on[3]	b2_on[2]	b2_on[1]	b2_on[0]	b2_off[3]	b2_off[2]	b2_off[1]	b2_off[0]
2DH	r2slope, r2duty	r2slope[3]	r2slope[2]	r2slope[1]	r2slope[0]	r2duty[3]	r2duty[2]	r2duty[1]	r2duty[0]
2EH	g2slope, g2duty	g2slope[3]	g2slope[2]	g2slope[1]	g2slope[0]	g2duty[3]	g2duty[2]	g2duty[1]	g2duty[0]
2FH	b2slope, b2duty	b2slope[3]	b2slope[2]	b2slope[1]	b2slope[0]	b2duty[3]	b2duty[2]	b2duty[1]	b2duty[0]

Default value of each register is 0000 0000 except boost output which is 0011 1111 (5V).





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