

LMX2525 PLLatinum[™] Dual Frequency Synthesizer System with Integrated VCOs **General Description**

LMX2525 is a highly integrated, high performance, low power frequency synthesizer system optimized for dualband Japan PDC mobile handsets. Using a proprietary digital phase locked loop technique. LMX2525 generates verv stable, low noise local oscillator signals for up and down conversion in wireless communications devices.

LMX2525 includes dual voltage controlled oscillators (VCOs) for the upper and lower Japan PDC frequency bands, a loop filter, and a fractional-N RF PLL based on a delta sigma modulator. In concert, these blocks form a closed loop RF synthesizer system. The RF synthesizer system supports two frequency bands: PDC1500 and PDC800.

Serial data is transferred to the device via a three-wire MICROWIRE interface (DATA, LE, CLK).

Operating supply voltage ranges from 2.5 V to 3.3 V. LMX2525 features low current consumption: 10 mA at 2.8 V when operating in the PDC800 mode.

LMX2525 is available in a 24-pin leadless leadframe package (LLP).

Features

- Small Size
 - 5.0 mm X 4.0 mm X 0.75 mm 24-Pin LLP Package
 - **RF** Synthesizer System Two Integrated VCOs Integrated Loop Filter Low Spurious, Low Phase Noise Fractional-N RF PLL Based on 10-Bit Delta Sigma Modulator Frequency Resolution Down to 20 kHz
 - Supports Various Reference Frequencies 12.6 MHz, 14.4 MHz, 25.2MHz, and 26.0 MHz
 - Fast Lock Time: 300 µs
 - Low Current Consumption 10 mA at 2.8 V in PDC800 Mode
 - 2.5 V to 3.3 V Operation
 - Digital Filtered Lock Detect Output
 - Hardware and Software Power Down Control

Applications

Japan PDC Systems at 800 MHz and 1500 MHz Frequency Bands.



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Connection Diagram

24-Pin 5x4 LLP (LQ) Package



Note: Analog ground connected through exposed die attached pad.

Pin Descriptions

Pin Number	Name	I/O	Description
1	L1	—	RF2 VCO tank pin. An external inductor is required between pins
			L1 and L2 to set the resonant frequency of RF2 VCO (PDC800).
2	L2	—	RF2 VCO tank pin. An external inductor is required between pins
			L1 and L2 to set the resonant frequency of RF2 VCO (PDC800).
3	NC	—	Do not connect to any node on the printed circuit board.
4	NC	—	Do not connect to any node on the printed circuit board.
5	V_{DD}	—	Supply voltage for RF analog circuitry
6	RF1out	0	RF output of RF1 VCO for PDC1500
7	V _{DD}	—	Supply voltage for RF analog circuitry
8	RF2out	0	RF output of RF2 VCO for PDC800
9	V _{DD}	—	Supply voltage for analog circuitry
10	V _{cc}	_	Supply voltage for digital circuitry
11	GND	_	Ground for digital circuitry
12	V _{cc}	_	Supply voltage for digital circuitry
13	LE	I	MICROWIRE Latch Enable
14	DATA	I	MICROWIRE Data
15	CLK	I	MICROWIRE Clock
16	CE	I	Chip enable control pin
17	BS	I	Band select control pin
18	LD	0	Lock detect pin
19	V _{cc}	_	Supply voltage for digital circuitry
20	OSCin	I	Reference frequency input
21	GND	_	Ground for digital circuitry
22	V _{DD}	_	Supply voltage for analog circuitry
23	GND	_	Ground for analog circuitry
24	V _{DD}	_	Supply voltage for RF analog circuitry



Absolute Maximum Ratings (Notes 2, 3, 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Supply Voltage	V_{CC},V_{DD}	-0.5 to 3.6	V
Voltage on any pin	Vi	-0.3 to V _{CC} + 0.3	V
to GND		-0.3 to V _{DD} + 0.3	V
Storage Temperature Range	T _{STG}	-65 to 150	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Мах	Unit
Ambient Temperature	T _A	-30	25	85	°C
Supply Voltage (to GND)	V_{CC},V_{DD}	2.5		3.3	V

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the conditions listed.

Note 3: This device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should be done at ESD protected workstations.

Note 4: GND = 0 V.

Electrical Characteristics (V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for $T_A = 25$ °C; Limits in **boldface** type apply over the operating temperature range from -20 °C $\leq T_A \leq$ 75 °C unless otherwise noted.)

Symbol	Parameter	Condition	Min	Тур	Max	Units
I _{CC} PARA	METERS					
$I_{CC} + I_{DD}$	Supply Current (Note 5)	OB_CRL [1:0] = 10		10.6	12.0	mA
					12.3	
		OB_CRL [1:0] = 00		10.0	11.5	mA
					11.8	
$I_{CC} + I_{DD}$	Supply Current (Note 6)	OB_CRL [1:0] = 10		15.0	16.5	mA
					16.8	
		OB_CRL [1:0] = 00		14.2	15.6	mA
					15.9	
I _{PD}	Power Down Current	CE = LOW or			20	μA
. <u> </u>		RF_PD = 1				
REFEREN	CE OSCILLATOR PARAMETERS	I	1	1	1	
f _{OSCin}	Reference Oscillator Input Frequency	Supports 12.6, 14.4, 25.2	12.6	14.4	26.0	MHz
	(Note 7)	and 26.0 MHz.				
V _{OSCin}	Reference Oscillator Input Sensitivity			0.5	V _{cc}	Vp-p
RF1 VCO	FOR PDC1500	1		1	1	1
f _{RF1out}	Frequency Range (Note 8)	RF1 VCO for PDC1500	1270.22		1394.95	MHz
P _{RF1out}	Output Power	OB_CRL [1:0] = 11	-5	-2	1	dBm
		OB_CRL [1:0] = 10	-7	-4	-1	dBm
		OB_CRL [1:0] = 01	-10	-7	-4	dBm
		OB_CRL [1:0] = 00	-13	-10	-7	dBm
	Lock Time	Full frequency span within			300	μs
		each band in High Speed			(Note 9)	
		Mode (HS = 1).				
		Between bands High Speed			300	μs
		Mode (HS = 1).			(Note 9)	
		Full frequency span within			500	μs
		each band in Normal Mode			(Note 9)	
		(HS = 0).			375	μs
		(Note 11)			(Note 10)	
		Between bands in Normal			500	μs
		Mode (HS = 0).			(Note 9)	
					400	μs
. <u> </u>					(Note 10)	
	RMS Phase Error			1.3		degrees

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Electrical Characteristics (V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for $T_A = 25$ °C; Limits in **boldface** type apply over the operating temperature range from -20 °C $\leq T_A \leq 75$ °C unless otherwise noted.) (Continued)

Symbol	Parameter	Condition	Min	Тур	Max	Units
RF1 VCO	FOR PDC1500					
L(f) _{RF1out}	Phase Noise when RF1 VCO for PDC1500 is activated in Normal	@ 25 kHz offset		-95	-93 -91	dBc/Hz
	Mode (HS = 0).	@ 50 kHz offset		-106	-103 -101	dBc/Hz
		@ 100 kHz offset		-115	-113 -111	dBc/Hz
		@ 1 MHz offset			-135 -133	dBc/Hz
	2 nd Harmonic Suppression				-25	dBc
	3 rd Harmonic Suppression	OB CRL [1:0] = 11, 10, 01			-20	dBc
		OB_CRL [1:0] = 00			-14 -11	dBc
	Spurious Tones	@ ≤ 25 kHz offset			-45	dBc
		@ 25 kHz < offset ≤ 50 kHz			-60	dBc
		@ 50 kHz < offset ≤ 100 kHz			-69	dBc
		@ offset > 100 kHz			-75	dBc
RF2 VCO	FOR PDC800				11	
f _{RF2out}	Frequency Range (Note 8)	RF2 VCO for PDC800	633.15		768.00	MHz
P _{RF2out}	Output Power	OB_CRL [1:0] = 11	-6	-3	0	dBm
		OB_CRL [1:0] = 10	-9	-6	-3	dBm
		OB_CRL [1:0] = 01	-11	-8	-5	dBm
		OB_CRL [1:0] = 00	-15	-12	-9	dBm
	Lock Time	Full frequency span within			300	μs
		each band in High Speed Mode (HS = 1).			(Note 9)	
		Between bands High Speed Mode (HS = 1).			300 (Note 9)	μs
		Full frequency span within each band in Normal Mode			500 (Note 9)	μs
		(HS = 0). (Note 11)			375 (Note 10)	μs
		Between bands in Normal Mode (HS = 0)			500 (Note 9)	μs
					400	μs
<u> </u>	BMS Phase Error			1 2		degrees
L(f) _{RF2out}	Phase Noise when RF2 VCO for	@ 25 kHz offset		-95	-93	dBc/Hz
	(HS = 0).	@ 50 kHz offset		-106	-103	dBc/Hz
		@ 100 kHz offset		-115	-101 -113	dBc/Hz
		@ 1 MHz offset			-111 -135 -133	dBc/Hz
<u> </u>	2 nd Harmonic Suppression				-25	dBo
<u> </u>	3 rd Harmonic Suppression	OB_CBL[1:0] = 11_10_01			-20	dBc
		OB_CRL[1:0] = 00			-14	dBc
	<u> </u>				-11	

Electrical Characteristics (V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for $T_A = 25$ °C; Limits in **boldface** type apply over the operating temperature range from -20 °C $\leq T_A \leq 75$ °C unless otherwise noted.) (Continued)

Symbol	Parameter	Condition	Min	Тур	Max	Units
RF2 VCO	FOR PDC800					
	Spurious Tones	@ ≤ 25 kHz offset			-45	dBc
		@ 25 kHz < offset ≤ 50 kHz			-60	dBc
		@ 50 kHz < offset ≤ 100 kHz			-69	dBc
		@ offset > 100 kHz			-75	dBc
DIGITAL	INTERFACE (DATA, CLK, LE, LD, CE,	BS)				
V _{IH}	High-Level Input Voltage		0.8 V _{CC}		V _{cc}	V
			0.8 V _{DD}		V _{DD}	V
V _{IL}	Low-Level Input Voltage		-0.3		0.2 V _{CC}	V
			-0.3		0.2 V _{DD}	V
IIH	High-Level Input Current		-10		10	μA
IIL	Low-Level Input Current		-10		10	μA
	Input Capacitance			3		pF
	Rise/Fall Time			30		ns
V _{OH}	High-Level Output Voltage		V _{CC} - 0.4			V
			V _{DD} - 0.4			V
V _{OL}	Low-Level Output Voltage				0.4	V
	Output Capacitance				5	pF
MICROW	IRE INTERFACE TIMING					
t _{CS}	Data to Clock Set Up Time		50			ns
t _{CH}	Data to Clock Hold Time		10			ns
t _{CWH}	Clock Pulse Width HIGH		50			ns
t _{CWL}	Clock Pulse Width LOW		50			ns
t _{DS}	Latch Enable LOW to Data Set Up		50			ns
	Time					
t _{ES}	Clock to Latch Enable Set Up Time		50			ns
t _{EW}	Latch Enable Pulse Width		50			ns

Note 5: RF PLL and VCO in PDC800 mode.

Note 6: RF PLL and VCO in PDC1500 mode.

Note 7: The reference frequency must be programmed using the OSC_FREQ control bit. For other reference frequencies, please contact National Semiconductor. **Note 8:** For other frequency ranges, please contact National Semiconductor.

Note 9: Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/-1 kHz of the final frequency.

Note 10: Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/-3 kHz of the final frequency.

Note 11: Lock time specification also applies to power up with MICROWIRE serial interface.

Note 12: All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with $T_A = 25$ °C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.



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Note 13: Typical performance characteristics do not guarantee specific performance limits. For guaranteed specifications, refer to the Electrical Characteristics section.

Note 14: The frequency range is defined as the difference between the highest frequency and the lowest frequency of a given unit. For a chosen external inductance, the typical frequency range equals the difference between the Typical Maximum Frequency and the Typical Minimum Frequency. Typical frequency range may be assumed on any unit with that chosen external inductance, even if the unit has worst case Maximum Frequency or worst case Minimum Frequency.

Functional Description

GENERAL

The LMX2525 is a highly integrated frequency synthesizer system for Japan PDC wireless communication systems. The LMX2525 supports dual band operation for 800 MHz and 1500 MHz.

The LMX2525 includes all functional blocks for the RF PLL including RF VCOs, frequency dividers, PFDs, and loop filters. Only external passive elements for the RF2 VCO tank and supply bypassing are required to complete the RF synthesizer.

The LMX2525 uses a patent pending Fractional-N synthesizer architecture based on a delta sigma modulator to support fine frequency resolution. Four of the most common reference frequencies for PDC applications, 12.6 MHz, 14.4 MHz, 25.2 MHz and 26.0 MHz, are supported. The unique feature of this architecture is its low spurious modulation effect.

The use of a fractional synthesizer based on a delta sigma modulator allows for faster lock and system set-up times, which reduces system power consumption. The loop filter is included on chip to minimize the external noise coupling and to reduce the form factor applicable to the board level application. Only one of the two RF VCOs is activated at a given time, and each output is provided through its own output pin.

RF PLL SECTION

Frequency Selection

The divide ratio can be calculated using the following equations:

 $f_{VCO} = \{8 \text{ x RF}_B + \text{RF}_A + (\text{RF}_F\text{N} / \text{FD})\} \text{ x } (f_{OSC} / \text{ R}) \text{ where } (\text{RF}_A < \text{RF}_B) \text{ for PDC1500}$

 f_{VCO} = {4 x RF_B + RF_A + (RF_FN / FD)} x (f_{OSC} / R) where (RF_A < RF_B) for PDC800

 f_{VCO} : Output frequency of voltage controlled oscillator (VCO) RF_B: Preset divide ratio of binary 4-bit programmable counter (2 \leq RF_B \leq 15)

RF_A: Preset divide ratio of binary 3-bit swallow counter (0 \leq RF_A \leq 7 for PDC1500 and 0 \leq RF_A \leq 3 for PDC800)

RF_FN: Preset numerator of binary 10-bit modulus counter (0 \leq RF_FN < FD)

FD: Preset denominator for modulus counter (FD = $f_{OSC}/(R$ X $f_{CH})$ where f_{CH} is the channel spacing)

f_{OSC}: Reference oscillator frequency

R: Internal reference oscillator frequency divider (1 for 12.6 MHz and 14.4 MHz, 2 for 25.2 MHz and 26.0 MHz)

The denominator, FD, in the above equation is dependent on the channel spacing and reference oscillator frequency. The channel spacing will change based on the Rx/Tx and BS bits. *Table 6* in the R0 Register section summarizes the values of FD.

VCO Frequency Tuning

The center frequency of the RF VCOs are determined by the resonant frequency of the tank circuit, illustrated in *Figure 1*. With an internal fixed bonding-wire inductor and an external inductance, the center frequency of the VCO is given as follows:

$$f_{center} = \frac{1}{2\pi \sqrt{(L_{fixed} + L_{external}) \cdot C_{total}}}$$

where C_{total} is the total capacitance of the VCO, including the parasitic capacitance and the nominal self-tuning capacitance. Note, the external inductance consists of the PCB traces and lumped element inductor. The output frequency tuning range can be optimized for the specific application by selecting the appropriate external inductance. Refer to RF2 VCO Tuning Range vs. External Inductance plot to aid in selecting the appropriate external inductance. Care should be taken to ensure proper frequency coverage when choosing the tolerance of the lumped element inductor. For the 1500 MHz band, the internal bonding-wires provide the necessary inductance to set the VCO center frequency.



FIGURE 1. External Inductor Connection

In real implementation, the inductance of L_{fixed} and L_{external} can vary from its nominal value. The LMX2525 utilizes a built-in tracking algorithm to compensate for variations up to ±15% and tunes the VCO to the required frequency. During the frequency acquisition period, the loop bandwidth is extended to achieve the frequency lock. After the frequency lock, the loop bandwidth of the PLL is set to the nominal value and the phase lock is achieved. The transition between the two operating modes is very smooth and extremely fast to meet the stringent PDC requirements for lock time and phase noise.

POWER DOWN MODE

The LMX2525 includes the power down mode to reduce the power consumption. The LMX2525 enters the power down mode either by taking the CE pin LOW or by setting the RF_PD bit in the R0 register. If the CE pin is set LOW, the circuit is powered down regardless of the register values. When the CE pin is HIGH, the RF_PD bit controls power to the RF circuitry. Data can be written to the registers even when the CE pin is set LOW. The following truth table summarizes the power down logic.

TABLE 1. Pov	er Down Modes
--------------	---------------

CE Pin	RF_PD Bit	Mode
HIGH	0	Active
HIGH	1	Not Active
LOW	0	Not Active
LOW	1	Not Active

Functional Description (Continued)

BAND SELECT MODE

The BS pin and BS bit can be used to select one of the two RF VCO outputs. When using the BS pin, the BS bit must be set to 0, and when using the BS bit, the BS pin must be tied to ground. When using the BS pin, the state of the input must exceed the minimum band select set up time prior to the LE signal transition. The truth table summarizing the band select logic is as follows:

FABLE	2.	Band	Select	Modes

BS Pin	BS Bit	Mode
HIGH	0	PDC1500
LOW	0	PDC800
LOW	1	PDC1500

on the LD pin. When the PLL is not locked, the LD pin remains LOW. After obtaining phase lock, the LD pin will have a logical HIGH level. The LD output is always LOW when the LD register bit is 0 and in power down mode.

es

LD Bit	Mode
0	Disable (GND)
1	Enable

TABLE 4. Lock Detect Logic

RF PLL Section	LD Output
Locked	HIGH
Not Locked	LOW

LOCK DETECT MODE

The LD output can be used to indicate the lock status of the PLL. Bit 6 in Register R1 determines the signal that appears



FIGURE 2. Lock Detect Timing Diagram Waveform (Notes 15, 16, 17, 18, 19)

Note 15: LD output becomes LOW when the phase error is larger than t_{W2} . Note 16: LD output becomes HIGH when the phase error is less than t_{W1} for four or more consecutive cycles.

Note 17: Phase Error is determined on the leading edge. Only errors greater than t_{W1} and t_{W2} are labeled.

Note 18: t_{W1} is 5 ns for PDC1500 and 10 ns for PDC800. t_{W2} is 10 ns for both bands.

Note 19: The lock detect comparison occurs with every 64^{th} cycle of f_{R} and $f_{\text{N}}.$

Functional Description (Continued)

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FIGURE 3. Lock Detect Flow Diagram

LOCKING MODES

Two frequency-locking modes are provided: a Normal mode and a High Speed mode for faster lock times. The HS bit in register R0 controls the locking mode.

TADLE	-	L = a later as	N/
IABLE	5.	LOCKING	wodes

HS Bit	Mode
0	Normal mode
1	High Speed mode

MICROWIRE INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: CLK, DATA, and LE (Latch Enable). Serial data is clocked into the 24-bit shift register on the rising edge of the clock. The last bits decode the internal control register address. When the latch enable (LE) transitions from LOW to HIGH, data stored in the shift registers is loaded into the corresponding control register. The data is loaded MSB first.

Programming Description

GENERAL PROGRAMMING INFORMATION

The serial interface has a 24-bit shift register to store the incoming data bits temporarily. The incoming data is first loaded into the shift register from MSB to LSB. The data is shifted at the rising edge of the clock signal. When the latch enable signal transitions from LOW to HIGH, the data stored in shift register is transferred to the proper register depending on the address bit setting. The selection of the particular register is determined by the control bits indicated in boldface text.

At initial start-up, the MICROWIRE loading requires three default words (registers R2, loaded first, to R0, loaded last). After the device has been initially programmed, the RF VCO frequency can be changed using a single register (R0).

The control register content map describes how the bits within each control register are allocated to the specific control functions.

ster	MSB							SH	IFT I	REGI	STE	r Bi	r lo	CAT	ION									LSB
Regi	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0	RX/	RF_	RF_ HS 0 BS RF_B									À					RF	FN					0	0
(Default)	ТХ	PD					[3	:0]			[2:0]						[9:0]						
R1	SPI_	0	0	1	0	0	1	0	1	0	0	0	0 0 0 1 0 LD OB_ OSC_						0	1				
(Default)	DEF																		CF	٦L	FR	EQ		
																			[1:	0]	[1:0)]		
R2	1	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0
(Default)																								
R3	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1
R4	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	1	0	0	1	1	1
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

COMPLETE REGISTER MAP

Note: R0 control register will be used when hot start frequency change.

Note: Boldface text represent address bits.

R0 REGISTER

The R0 register address bits (R0 [1:0]) are "00".

The Rx/Tx bit selects between receive and transmit modes and, in conjunction with the band select bit (BS), the channel spacing to be synthesized.

The RF_PD bit selects the power down mode of the RF PLL and selected VCO.

The HS bit selects between normal and high speed locking mode.

The BS bit determines which of the two internal VCOs (PDC800 or PDC1500) is active.

The RF N counter consists of the 4-bit programmable counter (RF_B counter), the 3-bit swallow counter (RF_A counter) and the 10-bit delta sigma modulator (RF_FN counter). The equations for calculating the counter values are presented below.

	R0 REGISTER																					
	MSB							SHIF	TR	GIS	TER	BIT	LOC	ATIO	Ν							LSB
ter	23	3 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2															1	0				
egis	Data Field														Address							
å																	Fie	ld				
R0	RX/	RF_	HS	0	BS		RF	_В		F	RF_A	1				F	RF_F	=N			0	0
(Default)	ТΧ	PD					[3:	:0]			[2:0]						[9:0)]				

Name	Functions
RX/TX	RX/TX Mode
	0 = Rx
	1 = Tx
RF_PD	Power Down of RF Synthesizer
	0 = RF synthesizer on (Active mode)
	1 = RF synthesizer powered down
HS	Locking Mode
	0 = Normal Mode
	1 = High Speed Mode
BS	Band Select
	1 = RF1 VCO (PDC1500)
	0 = RF2 VCO (PDC800)
RF_B [3:0]	RF_B Counter
	4-bit programmable counter
	$0 \le RF_B \le 15$ for both bands
RF_A [2:0]	RF_A Counter
	3-bit swallow counter
	$0 \le RF_A \le 7$ for PDC1500
	$0 \le RF_A \le 3$ for PDC800
RF_FN [9:0]	RF_FN Counter
	10-bit modulus counter
	$0 \le RF_FN \le FD$ See <i>Table 6</i> for FD values.

Counter Name	Symbol	Functions
Modulus Counter	RF_FN	RF N Divider
Programmable Counter	RF_B	$N = 8 \times RF_B + RF_A + RF_FN/FD (PDC1500)$
Swallow Counter	RF_A	$N = 4 \times RF_B + RF_A + RF_FN/FD (PDC800)$

PULSE SWALLOW FUNCTION

 $f_{VCO} = \{8 \text{ x RF}_B + \text{RF}_A + (\text{RF}_F\text{N} / \text{FD})\} \text{ x } f_{OSC} / \text{R where } (\text{RF}_A < \text{RF}_B) \text{ for PDC1500}$

 $f_{VCO} = \{4 \ x \ RF_B + RF_A + (RF_FN \ / \ FD)\} \ x \ f_{OSC} \ / \ R \ where \ (RF_A < RF_B) \ for \ PDC800$

 f_{VCO} : Output frequency of voltage controlled oscillator (VCO)

RF_B: Preset divide ratio of binary 4-bit programmable counter (2 \leq RF_B \leq 15)

RF_A: Preset divide ratio of binary 3-bit swallow counter ($0 \le RF_A \le 7$ for PDC1500 and $0 \le RF_A \le 3$ for PDC800)

RF_FN: Preset numerator of binary 10-bit modulus counter (0 \leq RF_FN < FD)

FD: Preset denominator for modulus counter (FD = $f_{OSC}/(R \times f_{CH})$ where f_{CH} is the channel spacing)

f_{OSC}: Reference oscillator frequency

R: Internal reference oscillator frequency divider

OSC_FREQ [1:0]	Reference Oscillator Frequency (MHz)	R Divider
00	12.6	1
01	14.4	1
10	25.2	2
11	26.0	2

The value of the denominator (FD) is depended on the channel spacing and reference oscillator frequency. *Table 6* summarizes the denominator values based on the settings of the Rx/Tx, BS, and OSC_FREQ [1:0] bits.

Rx/Tx	BS	OSC_FREQ [1:0]	Reference Oscillator Frequency (MHz)	R	f _{CH} (kHz)	Denominator(FD)
0	0	00	12.6	1	25.0	504
0	0	01	14.4	1	25.0	576
0	0	10	25.2	2	25.0	504
0	0	11	26.0	2	25.0	520
0	1	00	12.6	1	25.0	504
0	1	01	14.4	1	25.0	576
0	1	10	25.2	2	25.0	504
0	1	11	26.0	2	25.0	520
1	0	00	12.6	1	20.0	630
1	0	01	14.4	1	20.0	720
1	0	10	25.2	2	20.0	630
1	0	11	26.0	2	20.0	650
1	1	00	12.6	1	22.22	567
1	1	01	14.4	1	22.22	648
1	1	10	25.2	2	22.22	567
1	1	11	26.0	2	22.22	585

TABLE 6. Demonimator Values

R1 REGISTER

The R1 register address bits (R1 [1:0]) are "01".

The SPI_DEF bit allows for the programming of words R3 to R5. Under most circumstances, the SPI_DEF bit should be set to 1.

The LD bit sets the function of the lock detect pin. Enabling the lock detect function provides a digital lock detect output of the active RF synthesizer at the LD pin.

The OB_CRL [1:0] bits determine the power level of the RF output buffer. The power level can be adjusted to best meet the system requirement. Refer to the Electrical Characteristics section for power output specifications.

The reference frequency selection bits, OSC_FREQ [1:0], are used to set the reference clock and R divider for use with one of the following reference frequencies: 12.6 MHz, 14.4 MHz, 25.2 MHz or 26.0 MHz. The LMX2525 uses the OSC_FREQ bits along with the BS and RX/TX bits to determine the correct divide ratios needed to meet the required channel spacing for the mode of operation selected. Refer to *Table 6* for a summary of denominator values.

	R1 REGISTER																							
	MSB							S	SHIFT	RE(GIST	ER E	BIT L	OCA	TIC	N								LSB
iter	23	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 D + F + + + + + + + + + + + + + + + + +															1	0						
sige	Data Field A															Ad	Address							
å		Field															ld							
R1	SPI_	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	LD	OB		OS	C_	0	1
(Default)	DEF																		CR	L	FRE	EQ		
																			[1:0)]	[1:0]		

Name	Functions
SPI_DEF	Default Register Selection
	0 = OFF (Use values set in R0 to R5)
	1 = ON (Use default values set in R0 to R2)
LD	Lock Detect
	0 = Disable (GND)
	1 = Enable
OB_CRL [1:0]	Output Buffer Control
	00 = Minimum Output Power
	01 =
	10 =
	11 = Maximum Output Power
OSC_FREQ [1:0]	Reference Frequency Selection
	00 = 12.6 MHz
	01 = 14.4 MHz
	10 = 25.2 MHz
	11 = 26.0 MHz

R2 REGISTER

The R2 register address bits (R2 [1:0]) are "10".

	R2 REGISTER																	
	MSB SHIFT REGISTER BIT LOCATION																LSB	
iter	23	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2															1	0
Regis	Data Field															Ad Fie	dress Id	
R2 (Default)	1	1 1 0 0 1 0 0 1 1 1 1 0 0 0 0 0 1														1	1	0

R3 REGISTER

The R3 register address bits (R3 [2:0]) are "011". This register is only written to if the SPI_DEF bit is set to 0.

	R3 REGISTER																							
	MSB	ISB SHIFT REGISTER BIT LOCATION															LSB							
ster	23	22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0													0									
gis		Data Field Addres															SS							
Å																						Fie	eld	
R3	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1

R4 REGISTER

The R4 register address bits (R4 [3:0]) are "0111". This register is only written to if the SPI_DEF bit is set to 0.

	R4 REGISTER																							
	MSB	SB SHIFT REGISTER BIT LOCATION															LSB							
ster	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gis		Data Field Address																						
Å																					Fie	eld		
R4	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	1	0	0	1	1	1

R5 REGISTER

The R5 register address bits (R5 [4:0]) are "01111". This register is only written to if the SPI_DEF bit is set to 0.

_		ho headoren																							
	ter	MSB	SB SHIFT REGISTER BIT LOCATION															LSB							
	gis	23	22	22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1													0								
	Re		Data Field Address Field														ield								
Γ	R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

R5 REGISTER



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