



LMV115

GSM Baseband 30MHz 2.8V Oscillator Buffer

General Description

The LMV115 is a 30MHz buffer specially designed to minimize the effects of spurious signals from the base band chip to the oscillator. The buffer also minimizes the influence of varying load resistance and capacitance to the oscillator and increases the drive capability.

The input of the LMV115 is internally biased with two equal resistors to the power supply rails. This allows AC coupling on the input.

The LMV115 offers a shutdown function to optimize current consumption. This shutdown function can also be used to control the supply voltage of an external oscillator. The device is in shutdown mode when the shutdown pin is connected to V_{DD} .

The LMV115 comes in SC70-6 package. This space saving product reduces components, improves clock signal and allows ease of placement for the best form factor.

Features

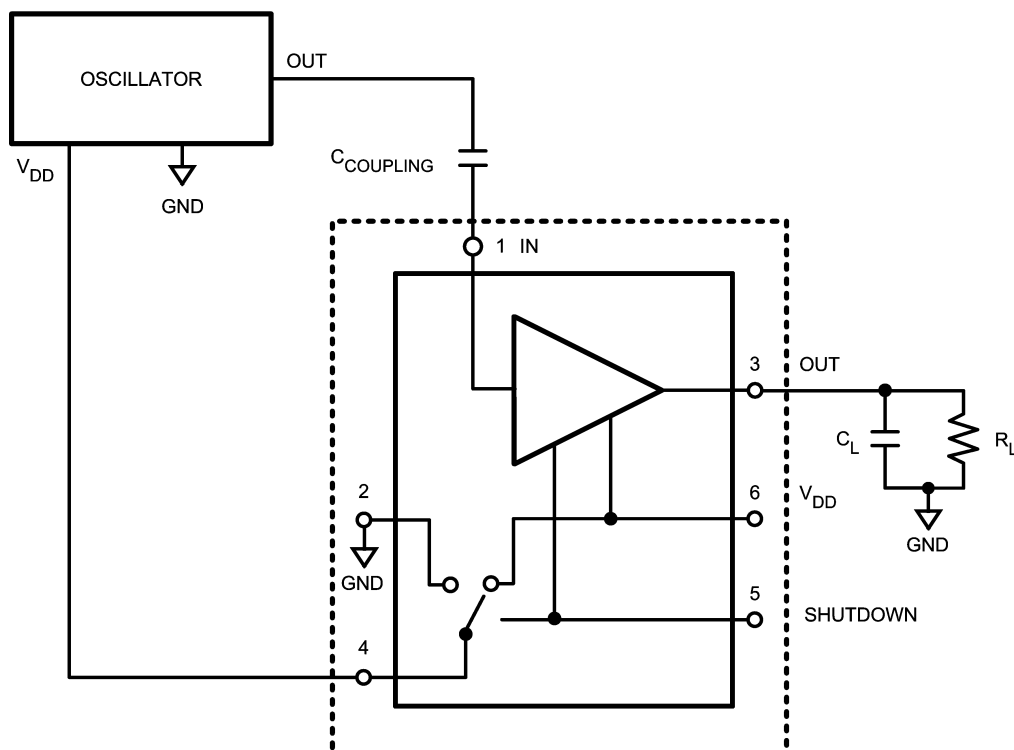
(Typical 2.8V supply; values unless otherwise specified)

- Low supply current: 0.3mA
- 2.5V to 3.3V supply
- AC coupling possible without external bias resistors.
- Includes shutdown function external oscillator
- SC70-6 pin package 2.1 x 2mm
- Operating Temperature Range -40°C to 85°C

Applications

- Cellular phones
- GSM Modules
- Oscillator Modules

Schematic Diagram



20075129

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance

Human Body Model	2000V (Note 2)
Machine Model	150V (Note 3)
Supply Voltage ($V^+ - V^-$)	3.6V
Output Short Circuit to V^+	(Note 4), (Note 5)
Output Short Circuit to V^-	(Note 4), (Note 5)
Storage Temperature Range	-65°C to +150°C

Junction Temperature (Note 6)

+150°C

Mounting Temperature

Infrared or Convection (20 sec.)

235°C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	2.5V to 3.3V
Temperature Range (Note 6), (Note 7)	-40°C to +85°C
Package Thermal Resistance (Note 6), (Note 7)	SC70-6
	414°C/W

2.8V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.8\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, shutdown = 0.0V, and $R_L = 50\text{k}\Omega$ to $V^+/2$, $C_L = 5\text{pF}$ to $V^+/2$ and $C_{COUPLING} = 1\text{nF}$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
SSBW	Small Signal Bandwidth	V _{OUT} < 0.5V _{PP} ; −3dB		31		MHz
GFN	Gain Flatness < 0.1dB	f > 50kHz		2.8		MHz
FPBW	Full Power Bandwidth (−3dB)	V _{OUT} = 1.0V _{PP} (+4.5dBm)		9		MHz
Time Domain Response						
t _r	Rise Time	0.1V _{STEP} (10-90%)		11		ns
t _f	Fall Time			11		
t _s	Settling Time to 0.1%	0.1V _{STEP}		95		ns
OS	Overshoot	0.1V _{STEP}		24		%
SR	Slew Rate	(Note 11)		18		V/μs
Distortion and Noise Performance						
HD2	2 nd Harmonic Distortion	V _{OUT} = 500mV _{PP} ; f = 100kHz		−41		dBc
HD3	3 rd Harmonic Distortion	V _{OUT} = 500mV _{PP} ; f = 100kHz		−43		dBc
THD	Total Harmonic Distortion	V _{OUT} = 500mV _{PP} ; f = 100kHz		−38		dBc
e _n	Input-Referred Voltage Noise	f = 1MHz		27		nV/ √Hz
Isolation	Output to Input	See also Typical Performance Characteristics		>40		dB
Static DC Performance						
A _{CL}	Small Signal Voltage Gain	V _{OUT} = 100mV _{PP}	0.90 0.85	0.998	1.10 1.11	V/V
V _{OS}	Output Offset Voltage			3.5	35 55	mV
TC V _{OS}	Temperature Coefficient Output Offset Voltage	(Note 12)		102		μV/°C
R _{OUT}	Output Resistance	f = 10kHz		61		Ω
		f = 25MHz		330		
PSRR	Power Supply Rejection Ratio	V ⁺ = 2.8V to V ⁺ = 3.3V	41 38	42		dB
I _S	Supply Current	No Load; Shutdown = 2.8V		0.0	2.00	μA
		No Load; Shutdown = 0V		314	450 520	
Miscellaneous Performance						
R _{IN}	Input Resistance	Shutdown = 2.8V		65		kΩ
		Shutdown = 0V		64		
C _{IN}	Input Capacitance	Shutdown = 2.8V		1.82		pF
		Shutdown = 0V		1.50		

2.8V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.8\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, shutdown = 0.0V , and $R_L = 50\text{k}\Omega$ to $V^+/2$, $C_L = 5\text{pF}$ to $V^+/2$ and $C_{COUPLING} = 1\text{nF}$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 9)	Typ (Note 8)	Max (Note 9)	Units
Z_{IN}	Input Impedance	$f = 25\text{MHz}$; Shutdown = 2.8V		2.38		$\text{k}\Omega$
		$f = 25\text{MHz}$; Shutdown = 0V		2.47		
V_O	Output Swing Positive	$R_L = 50\text{k}\Omega$ to $V^+/2$	1.90 1.65	2.16		V
	Output Swing Negative	$R_L = 50\text{k}\Omega$ to $V^+/2$		1.05	1.35 1.30	
I_O	Linear Output Current	No Load; $V_{OUT} = V^+ - 1.1\text{V}$ (Sourcing)	-90 -35	-206		μA
		No Load; $V_{OUT} = V^- + 1.1\text{V}$ (Sinking)	100 50	205		
I_{SC}	Output Short-Circuit Current (Note 5)	No Load; Sourcing to $V^+/2$	-90 -35	-186		μA
		No Load; Sinking from $V^+/2$	100 50	191		
R_{ON}	Switch in ON Position			21	40 45	Ω

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human Body Model (HBM) is $1.5\text{k}\Omega$ in series with 100pF .

Note 3: Machine Model, 0Ω in series with 200pF .

Note 4: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

Note 5: Infinite Duration; Short circuit test is a momentary test. See next note.

Note 6: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 7: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. There is no guarantee of parametric performance as indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information on temperature de-rating of this device.

Note 8: Typical Values represent the most likely parametric norm.

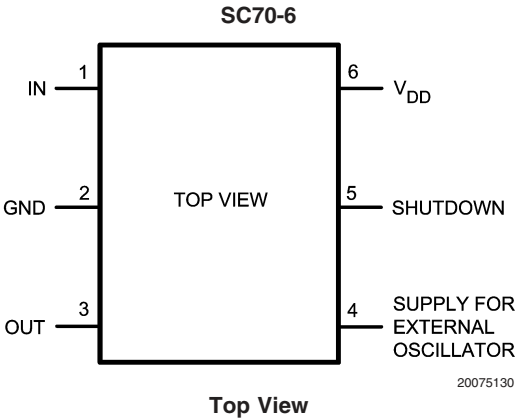
Note 9: All limits are guaranteed by testing or statistical analysis.

Note 10: Positive current corresponds to current flowing into the device.

Note 11: Slew rate is the average of the positive and negative slew rate.

Note 12: Average Temperature Coefficient is determined by dividing the change in a parameter at temperature extremes by the total temperature change.

Connection Diagram

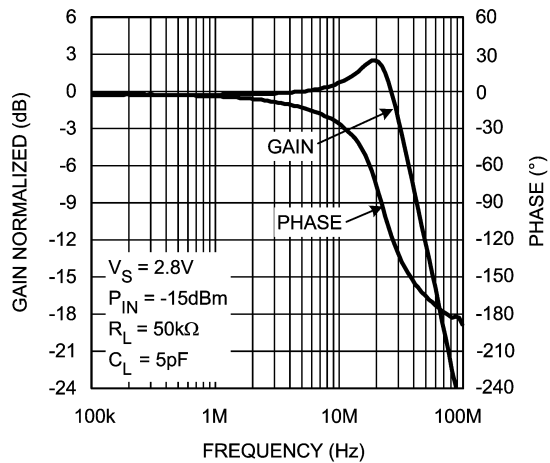


Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
SC70-6	LMV115MG	B04	250 Units Tape and Reel	MAA06A
	LMV115MGX		3k Units Tape and Reel	

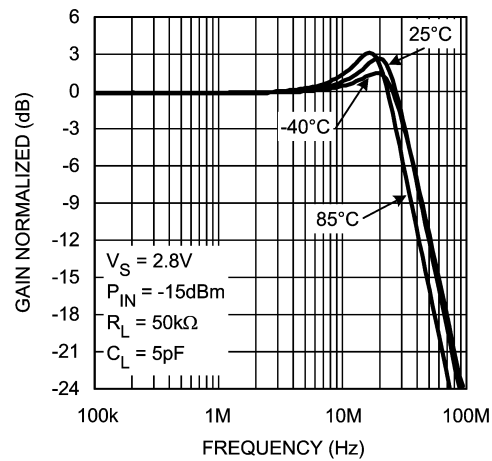
Typical Performance Characteristics $T_J = 25^\circ\text{C}$, $V^+ = 2.8\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, and R_L , C_L is connected to $V^+/2$; Unless otherwise specified.

Frequency and Phase Response



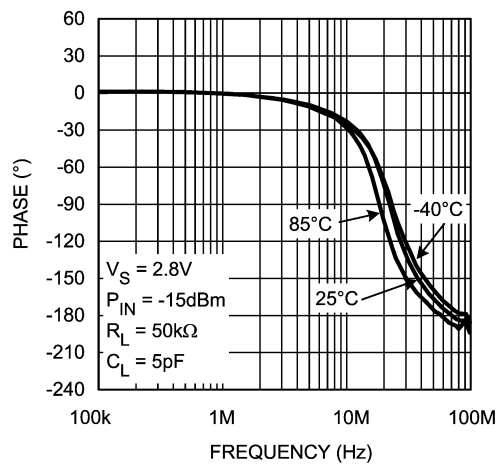
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Frequency Response Over Temperature



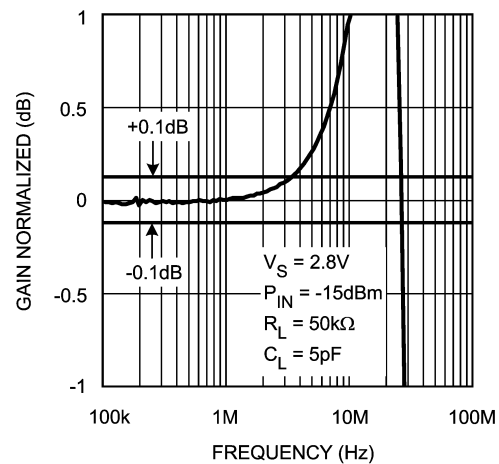
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Phase Response Over Temperature



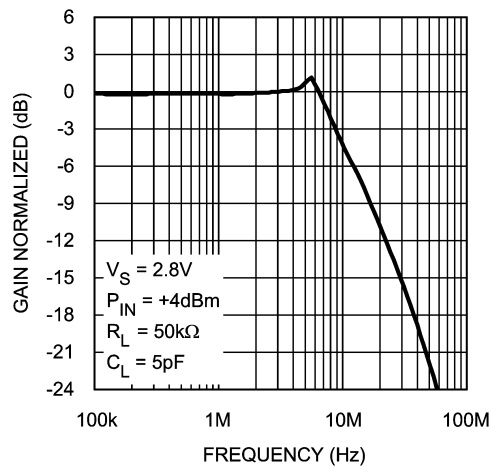
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Gain Flatness 0.1dB



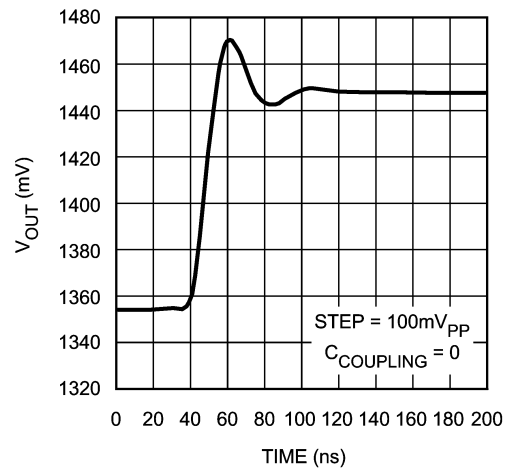
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Full Power Bandwidth



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Transient Response Positive

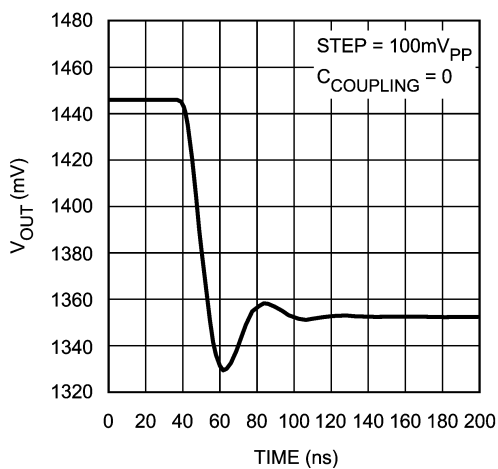


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Typical Performance Characteristics

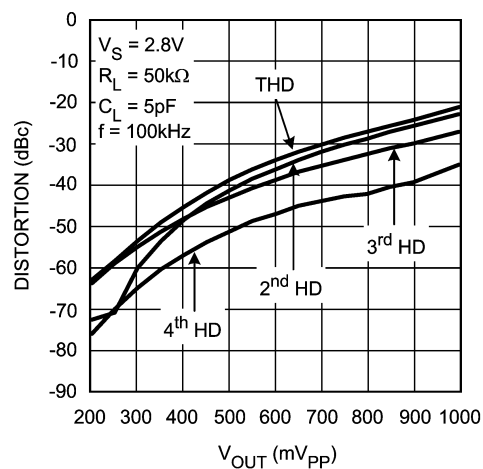
$T_J = 25^\circ\text{C}$, $V^+ = 2.8\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, and R_L , C_L is connected to $V^+/2$; Unless otherwise specified. (Continued)

Transient Response Negative



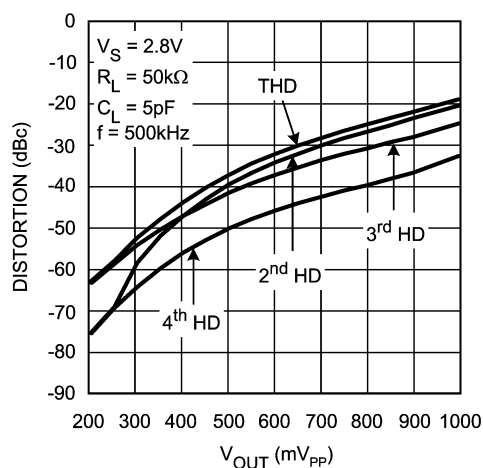
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Harmonic Distortion vs. V_{OUT} @ 100kHz



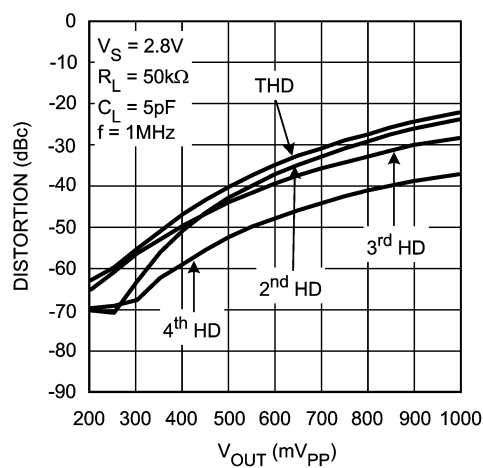
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Harmonic Distortion vs. V_{OUT} @ 500kHz



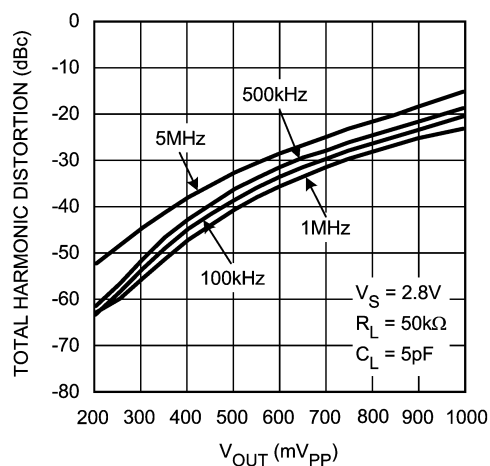
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Harmonic Distortion vs. V_{OUT} @ 1MHz



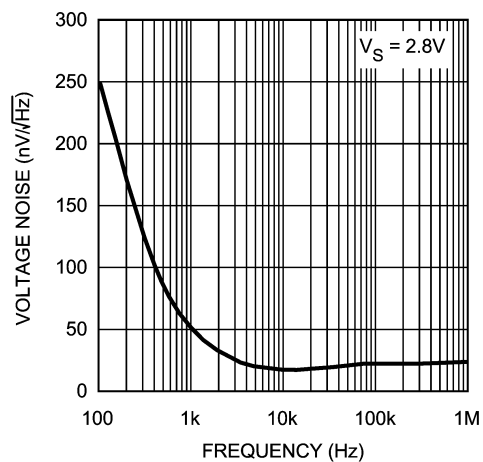
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THD vs. V_{OUT} for Various Frequencies



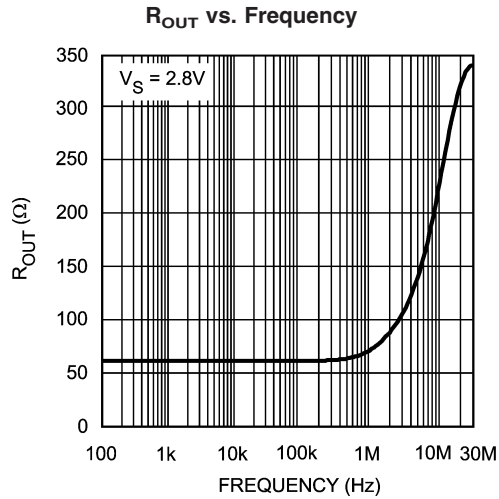
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Voltage Noise

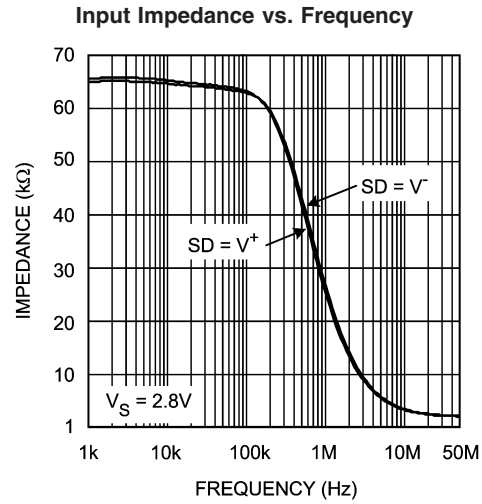


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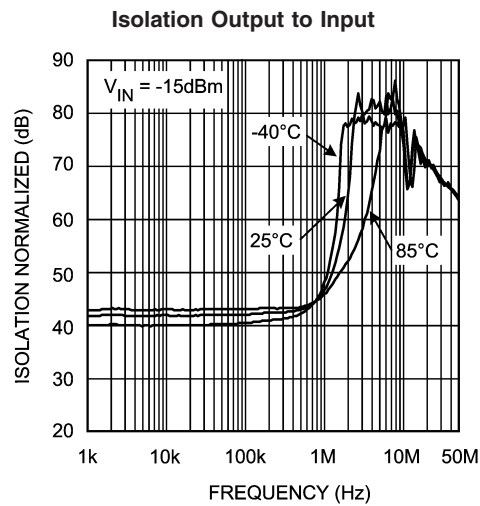
Typical Performance Characteristics $T_J = 25^\circ\text{C}$, $V^+ = 2.8\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V^+/2$, and R_L , C_L is connected to $V^+/2$; Unless otherwise specified. (Continued)



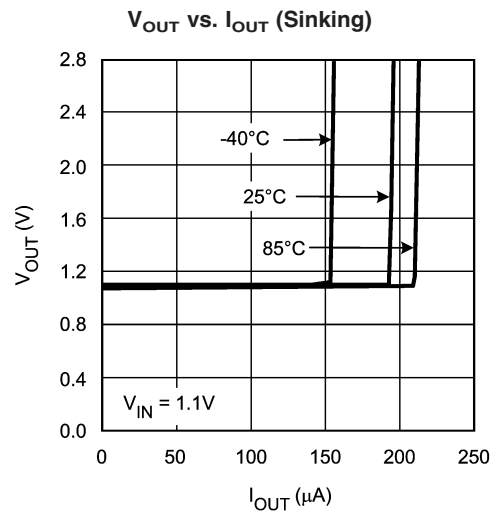
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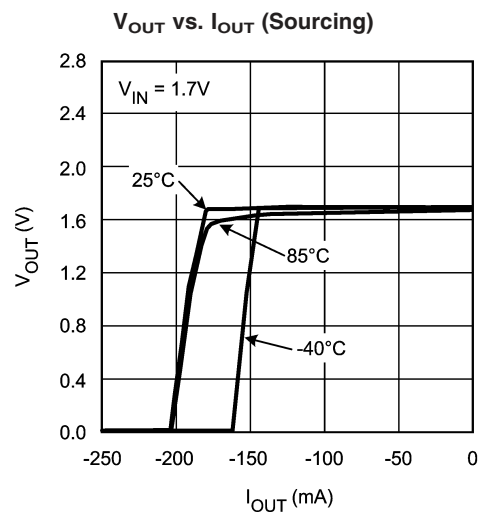
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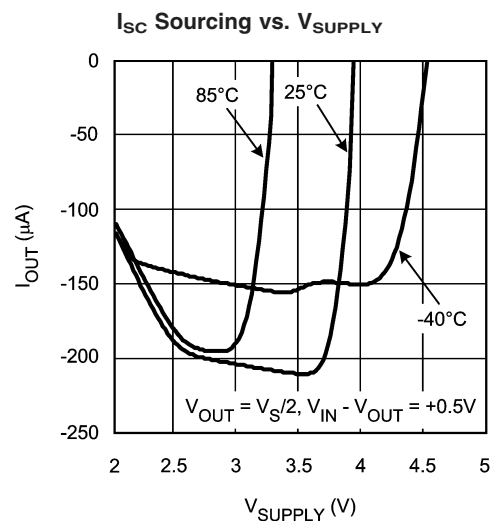
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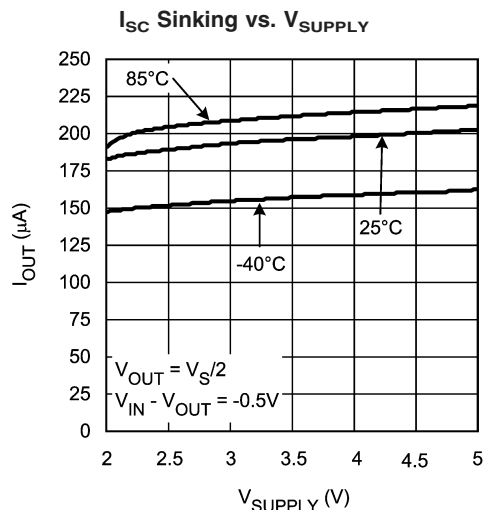
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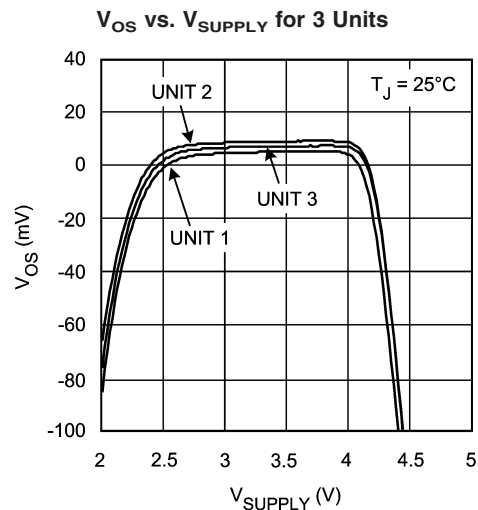
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Typical Performance Characteristics

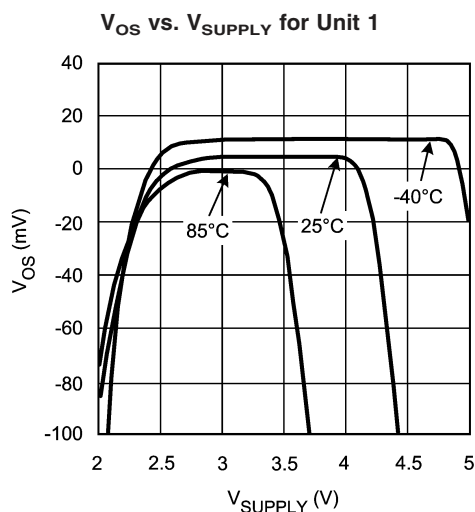
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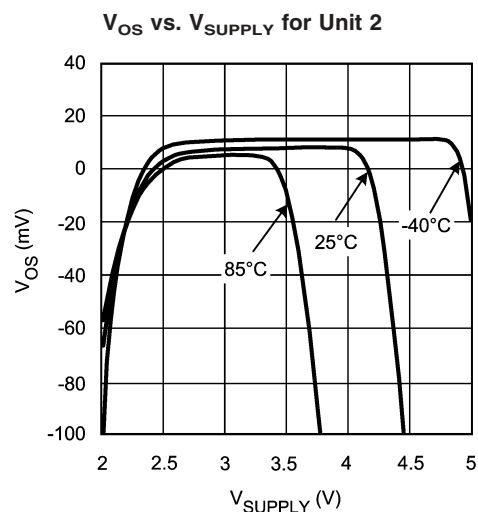
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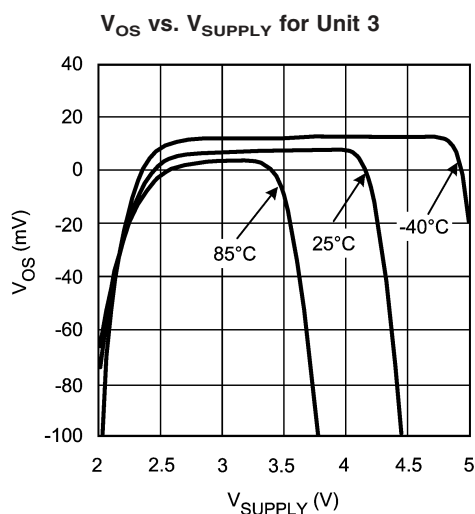
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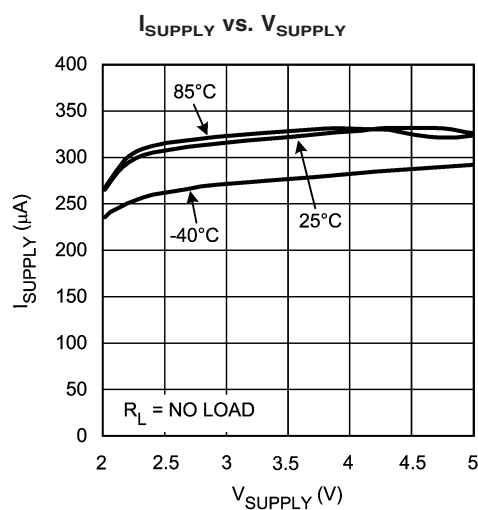
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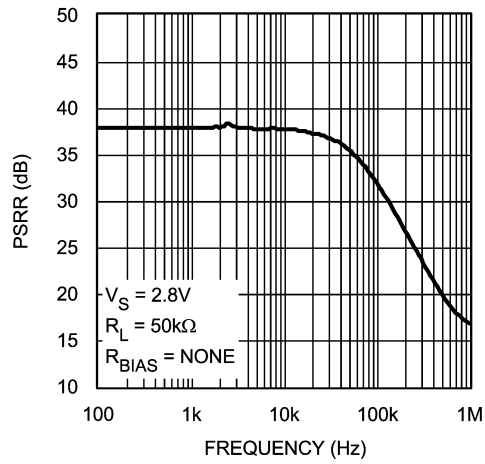


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Typical Performance Characteristics

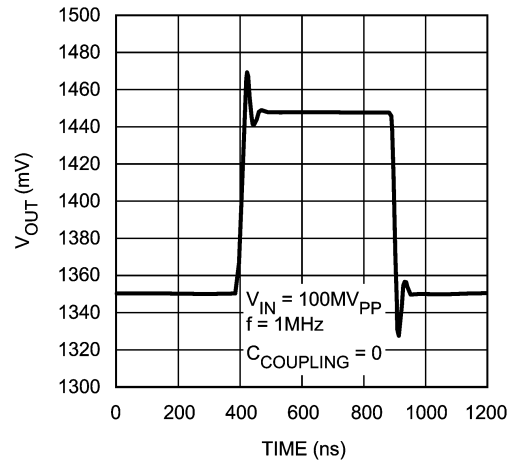
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PSRR vs. Frequency



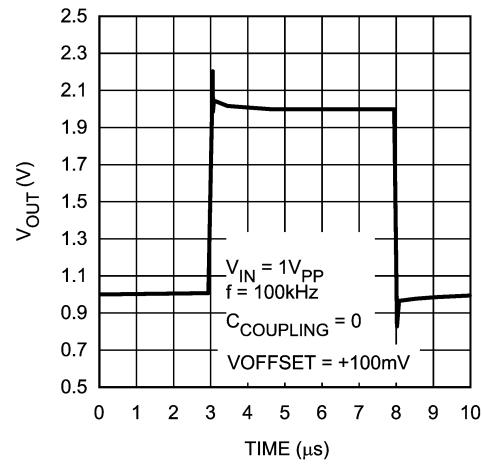
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Small Signal Pulse Response



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Large Signal Pulse Response



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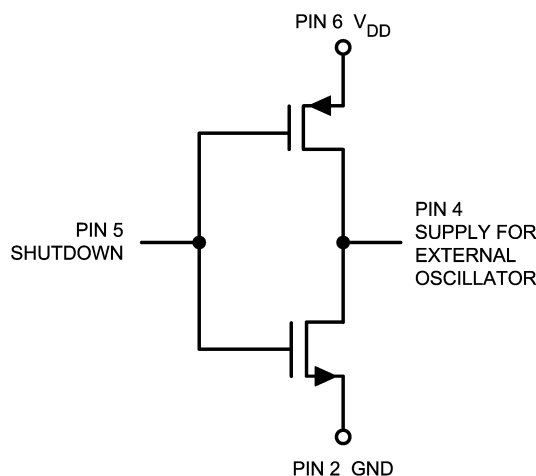
Application Section

GENERAL

The LMV115 is specially designed to minimize the effects of spurious signals from the base band chip to the oscillator. Beside this the influence of varying load resistance and capacitance to the oscillator is minimized, while increasing the drive capability. The input of the LMV115 is internally biased with two equal resistors to the power supply rails, and makes AC coupling possible without external bias resistors at the input. The LMV115 has excellent gain phase margin. The LMV115 offers a shutdown pin that can be used to disable the device in order to optimize current consumption and also has a feature to control the supply voltage to an external oscillator. When the shutdown pin is connected to V_{DD} the device is in shutdown mode.

SWITCHED POWER SUPPLY CONNECTION

The LMV115 features an enable/disable function for an external oscillator by controlling its supply voltage (pin 4). See also the schematic diagram on the front page. During normal operating mode, pin 4 is connected to the positive supply rail via an internal switch. The resistance between the positive supply rail and pin 4, R_{ON} , is specified in the electrical characterization table. Oscillators with a supply current up to several milliamps can easily be powered from pin 4. During shutdown, pin 4 is switched to the negative supply rail. The simplified schematic for this part of the device is shown in Figure 1

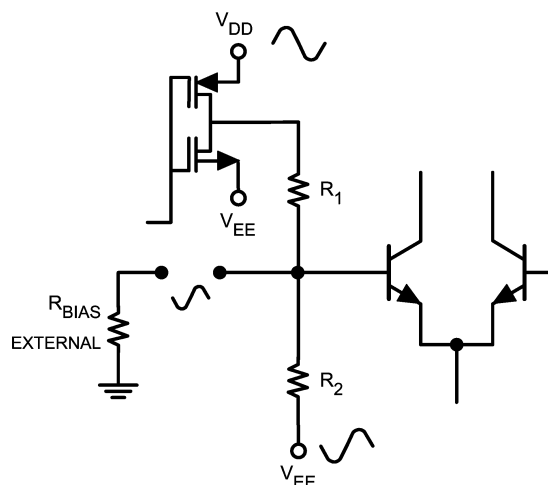


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FIGURE 1. Supply For External Oscillator

INPUT CONFIGURATION

The input of the LMV115 is internally biased at mid-supply by a divider of two equal resistors. With the LMV115 in shutdown mode, the internal resistor connected to the V_{DD} is shortened to the negative power supply rail via a switch. This makes the power consumption in 'off' mode almost zero, but causes a small difference for the input impedance between the on and off modes. Both resistors are 110k Ω so the resulting input impedance will be approximately 55k Ω . The input configuration allows AC coupling on the input of the LMV115. A simplified schematic of the input is shown in Figure 2.



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FIGURE 2. Dual Supply Mode

PSRR

If an AC signal is applied to one of the supply lines, while the input is floating, the signal at the input pin is half the signal at the supply line, causing the same signal at the output of the buffer. This will result in a PSRR of only 6dB (see Figure 2).

In a typical application the input is driven from a low ohmic source that means the disturbance at the supply lines is attenuated by the series resistors of 110k and the source impedance. In case the buffer is connected to a 50 Ω source, the resulting suppression will be $20 \cdot \log [(R_1 + R_{BIAS})/R_{BIAS}] = 67\text{dB}$ for signals at the supply line. The PSRR can also be measured correctly for this type of input by shortening the input to mid-supply. Due to the internal structure it is not recommended to measure with the input connected to ground. To measure correctly the PSRR, two signals are applied to both V_{DD} and V_{EE} but with 180° phase difference (see Figure 2). In this case, both signals are subtracted and there will be no signal at the input. The resulting disturbance at the output is now only caused by the signals at the supply lines.

INPUT AND OUTPUT LEVEL

Due to the internal loop gain of 1, the output will follow the input. The output voltage cannot swing as close to the supply rail as the input voltage. For linear operation the input voltage swing should not exceed the output voltage swing. The restrictions for the output voltage can be examined by the two curves in Figure 3. The curve V_{OUT} (V) shows the response of the output signal versus the input signal and the curve $V_{OUT} - V_{IN}$ (V) shows the difference between the output and the input signal.

Application Section (Continued)

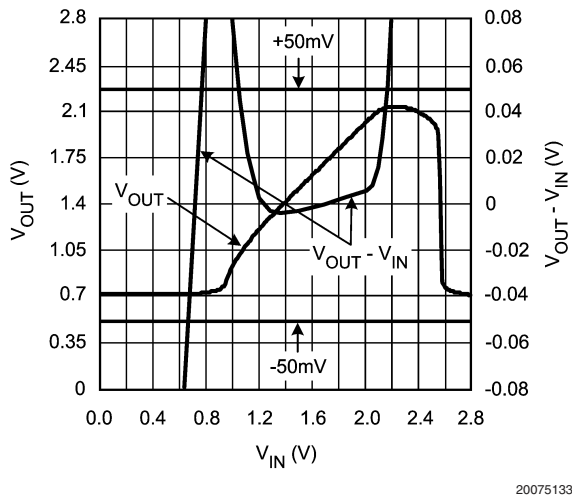


FIGURE 3. $V_{OUT} - V_{IN}$

In Figure 3 the input signal is swept between both supply rails (0V - 2.8V). The linear part of the plot ' V_{OUT} vs. V_{IN} ' covers approximately the voltage range between 1.0V and 2.0V. If a difference of 50mV between output and input is acceptable, the output range is between 1.05V and 2.15V (see curve $V_{OUT} - V_{IN}$). Alternatively the output voltage swing can be determined by using Figure 4. In the plot 'Gain vs. V_{IN} ' it can be seen that the gain is flat for input voltages from 1.15V till 2.1V. Outside this range the gain differs from 1. This will introduce distortion of the output signal.

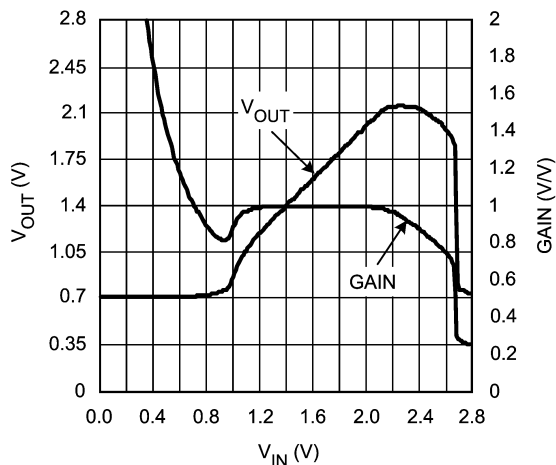


FIGURE 4. Gain

Another point is the DC bias voltage necessary to get the optimum output voltage swing. As discussed above, the output voltage swing can be $1V_{PP}$, but if the two internal bias resistors are used, the DC bias will be 1.4V, which is half of the supply voltage of 2.8V. In this situation the output swing will exceed the lower limit of 1.15V, so it is necessary to introduce a small DC offset of 200mV to make use of the full output swing range of the output stage.

DRIVING RESISTIVE AND CAPACITIVE LOADS

The maximum output current of the LMV115 is about 200 μ A which means the output can drive a maximum load of $1V / 200\mu A = 5k\Omega$. Using lower load resistances will exceed the maximum linear output current. The LMV115 can drive a small capacitive load, but make sure that every capacitor directly connected to the output becomes part of the loop of the buffer and will reduce the gain/phase margin, increasing the instability at higher capacitive values. This will lead to peaking in the frequency response and in extreme situations oscillations can occur. A good practice when driving larger capacitive loads is to include a series resistor to the load capacitor. A to D converters present complex and varying capacitive loads to the buffer. The best value for this isolation resistance is often found by experimentation.

SHUTDOWN MODE

LMV115 offers a shutdown function that can be used to disable the device and to optimize current consumption. Switching between the normal mode and the shutdown mode requires connecting the shutdown pin either to the negative or the positive supply rail. If directly connected to one of the supply rails, the part is guaranteed in the correct mode. But if the shutdown pin is driven by other output stages, there is a voltage range in which the installed mode is not certainly set and it is recommended not to drive the shutdown pin in this voltage range. As can be seen in Figure 5 this hysteresis varies from 1V to 1.6V. Below 1V the LMV115 is securely 'ON' and above 1.6V securely 'OFF' while using a supply voltage of 2.8V.

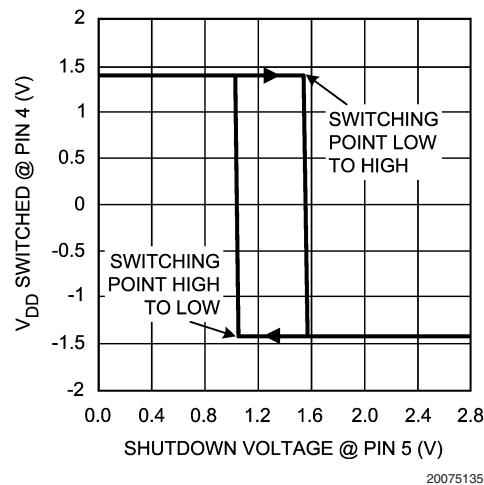


FIGURE 5. Hysteresis

PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT VALUES SELECTION

For a good high frequency design both the active parts and the passive ones should be suitable for the purpose they are used for. Amplifying high frequencies is possible with standard through-hole components, but for frequencies above several hundreds of MHz the best choice is using surface mount devices. Nowadays designs are often assembled with surface mount devices for the aspect of minimizing space, but this also greatly improves the performance of designs, handling high frequencies. Another important issue is the PCB, which is no longer a simple carrier for all the parts and a medium to interconnect them. The board becomes a real

Application Section (Continued)

part itself, adding its own high frequency properties to the overall performance of the circuit. It is good practice to have at least one ground plane on a PCB giving a low impedance path for all decoupling and other ground connections. In order to achieve high immunity for unwanted signals from outside, it is important to place the components as flat as possible on the PCB. Be aware that a long lead can act as an inductor, a capacitor or an antenna. A pair of leads can even form a transformer. Careful design of the PCB avoids oscillations or other unwanted behavior. Another important issue is the value of components, which also determines the sensitivity to pick-up unwanted signals. Choose the value of resistors as low as possible, but avoid using values that

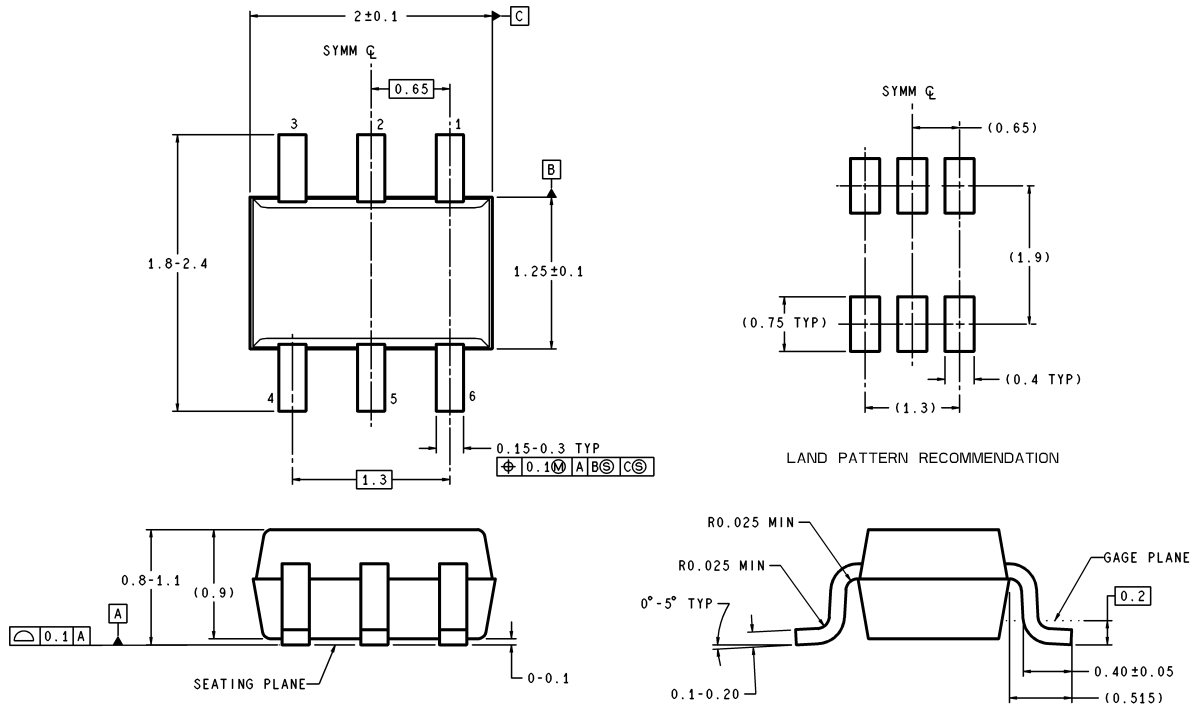
causes a significant increase in power consumption, while loading inputs or outputs too heavily.

NSC suggests the following evaluation board as a guide for high frequency layout and as an aid in device testing and characterization.

Device	Package	Evaluation Board PN
LMV115	SC70-6	LMV115/117 Eval Board

This free evaluation board is shipped when a device sample request is placed with National Semiconductor.

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

MAA06A (Rev A)

NS Package Number MAA06A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



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