National Semiconductor

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LMC6009
9 Channel Buffer Amplifier for TFT-LCD

General Description

The LMC6009 is a CMOS integrated circuit that buffers 9 reference voltages for gamma correction in a Thin Film Transistor Liquid Crystal Display (TFT-LCD). Guaranteed to operate at both 3.3V and 5V supplies, this integrated circuit contains nine, independent unity gain buffers that can source 130 mA into a capacitive load without oscillation.

The LMC6009 is useful for buffering gamma voltages into column drivers that employ the resistor-divider architecture. High output current capability and fast settling characteristics of this device improve display quality by minimizing rise time errors at the outputs of the column driver. The integration of nine buffers and a multiplexer eliminates the need for discrete buffers and a separate multiplexer (MUX) chip on the panel.

The LMC6009 is available in 48-pin surface mount TSSOP.

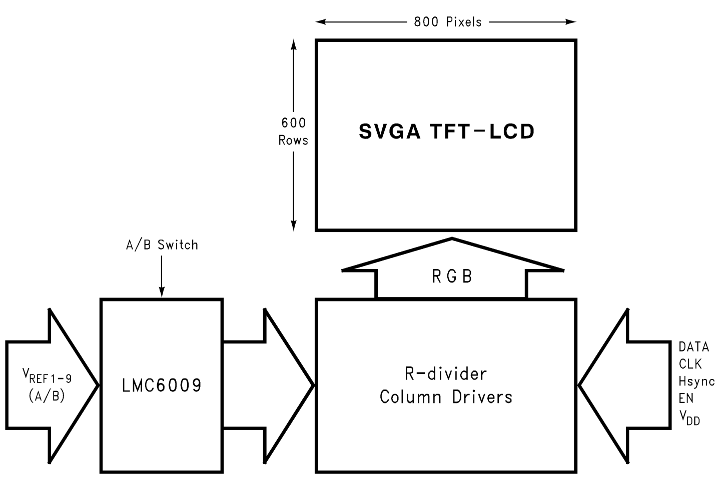
Features

- Number of inputs 18
- 3.3V and 5V operation
- Supply current 3.5 mA
- Settling time 3 µs
- A/B channel inputs for asymmetrical Gamma
- Number of outputs 9
- Number of control inputs 1
- Built-in thermal shutdown protection

Applications

- VGA/SVGA TFT-LCD drive circuits
- Electronic Notebooks
- Electronic Games
- Personal Communication Devices
- Personal Digital Assistants (PDA)

Application in VGA/SVGA TFT-LCD



DS012533-1

Ordering Information

Package	Temperature Range	Transport Media	NSC Drawing
48-pin TSSOP	−20˚C–+75˚C		MTD48
	LMC6009MT		
	LMC6009MTX	Tape and Reel	

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	1.0 kV
Input Voltage	GND–0.3V ≤ V^+ ≤ V_{DD}+0.3V_{DC}
Supply Voltage (V_{DD})	−0.3 to +6.5 V_{DC}
Operating Temperature	−20˚C to +75˚C
Storage Temperature Range	−55˚C to +150˚C
Maximum Junction Temperature (T_J)	+150˚C
Maximum Power Dissipation (P_D)	1.09W

Operating Ratings (Note 1)

Supply Voltage	2.7V ≤ V_{DD} ≤ 5.5V
Frequency	DC-50 kHz
Thermal Resistance (θ_{JA})	
Derating	8.70 mW/˚C

3V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, and V_{DD} = 3.0 V_{DC}.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		2.7	3.0	3.3	V
V_{OS}	Offset Voltage	R_S = 10k			20	mV
I_B	Input Bias Current				1500	nA
V_{OL}	Output Voltage, Low	Amp A8 and A9 I_{SINK} = 13 mA			GND + 0.2	V
		Amp A1–A7 I_{SINK} = 13 mA			GND + 0.6	V
V_{OH}	Output Voltage, High	Amp A1 and A2 I_{SOURCE} = 13 mA	V_{DD}–0.2			V
		Amp A3–A9 I_{SOURCE} = 13 mA	V_{DD}–0.6			V
I_{SC}	Output Short Circuit Current	V_{OUT} - 1.65V (Note 1)	80	150		mA
I_{DD}	Supply Current	No Load		3.5	5	mA
ΔV_L	Load Regulation	V_{IN} = 0.3–3 V_{DC} I_{SOURCE} = 13 mA			−10	mV
		I_{SINK} = 13 mA			+10	mV
V_{IH}	A/B Switch Logic Voltage, High	Select A	2			V
V_{IL}	A/B Switch Logic Voltage, Low	Select B			0.8	V
I_{IH}	A/B Switch Logic Current, High				1.5	µA
I_{IL}	A/B Switch Logic Current, Low				1	µA
A_V	Voltage Gain		0.985			V/V

Note 1: See Test Circuit (*Figure 2*)

5V DC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, and V_{DD} = 5 V_{DC}.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.5	5	5.5	V
V_{OS}	Offset Voltage	R_S = 10k			20	mV
I_B	Input Bias Current				1500	nA
V_{OL}	Output Voltage, Low	Amp A8 and A9 I_{SINK} = 20 mA			GND + 0.2	V
		Amp A1–A7 I_{SINK} = 20 mA			GND + 1.0	V
V_{OH}	Output Voltage, High	Amp A1 and A2 I_{SOURCE} = 20 mA	V_{DD}–0.2			V
		Amp A3–A9 I_{SOURCE} = 20 mA	V_{DD}–1.0			V
I_{SC}	Output Short Circuit Current	V_{OUT} - 1.65V (Note 1)	120	200		mA
I_{DD}	Supply Current	No Load		4.5	6	mA

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, and V_{DD} = 5 V_{DC}.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ΔV_L	Load Regulation	V_{IN} = 0.5–4.5 V_{DC} I_{SOURCE} = 20 mA			−10	mV
		I_{SINK} = 20 mA			+10	mV
V_{IH}	A/B Switch Logic Voltage, High	Select A	2			V
V_{IL}	A/B Switch Logic Voltage, Low	Select B			0.8	V
I_{IH}	A/B Switch Logic Current, High				1.5	µA
I_{IL}	A/B Switch Logic Current, Low				1	µA
A_V	Voltage Gain		0.985			V/V

AC Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_J = 25˚C, and V_{DD} = 3 V_{DC}.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{S1}	Settling Time 1 (Note 2)	I_{DC} = 13 mA (Sink/Source)		3	6	µs
T_{S2}	Settling Time 2 (Note 2)	I_{DC} = 13 mA (Sink/Source)		3	6	µs

Note 2: See test circuits (*Figure 3* , *Figure 4* and *Figure 5*)

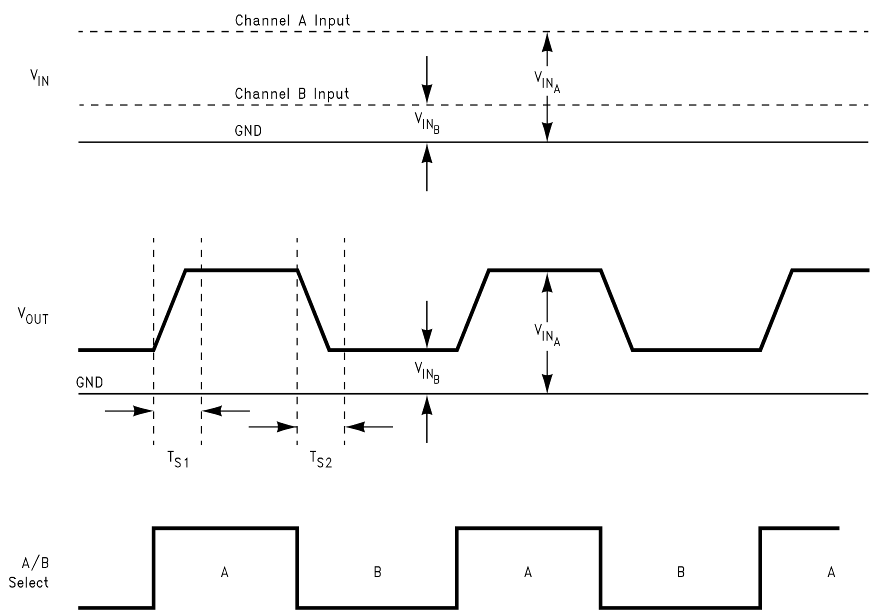


FIGURE 1. Rise and Fall Times at Outputs

AC Electrical Characteristics

(Continued)

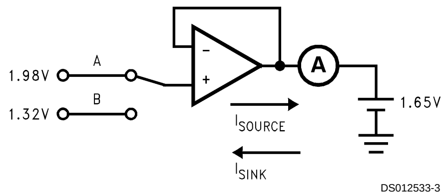


FIGURE 2.

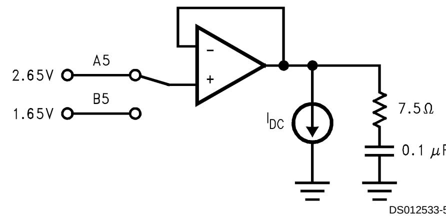


FIGURE 4. 13 mA Sink/Source

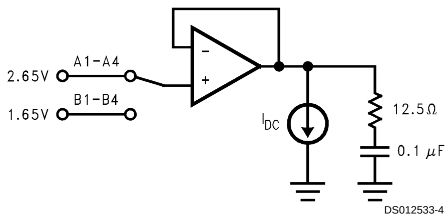


FIGURE 3. A1: 13 mA Source only A2–A4: 13 mA Sink/Source

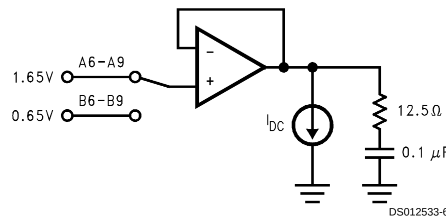


FIGURE 5. A6–A8: 13 mA Sink/Source A9: 13 mA Sink Only

Description of Pins; LMC6009

Pin 1	NC	Pin 25	NC
Pin 2	NC	Pin 26	NC
Pin 3	NC	Pin 27	NC
Pin 4	A1 in (A)	Pin 28	NC
Pin 5	A1 in (B)	Pin 29	A/B Switch
Pin 6	A2 in (A)	Pin 30	V_{DD} (C)
Pin 7	A2 in (B)	Pin 31	GND (C)
Pin 8	A3 in (A)	Pin 32	A9 out
Pin 9	A3 in (B)	Pin 33	A8 out
Pin 10	A4 in (A)	Pin 34	A7 out
Pin 11	A4 in (B)	Pin 35	A6 out
Pin 12	A5 in (A)	Pin 36	A5 out
Pin 13	A5 in (B)	Pin 37	GND (B)
Pin 14	A6 in (A)	Pin 38	V_{DD} (B)
Pin 15	A6 in (B)	Pin 39	A4 out
Pin 16	A7 in (A)	Pin 40	A3 out
Pin 17	A7 in (B)	Pin 41	A2 out
Pin 18	A8 in (A)	Pin 42	A1 out
Pin 19	A8 in (B)	Pin 43	GND (A)
Pin 20	A9 in (A)	Pin 44	V_{DD} (A)
Pin 21	A9 in (B)	Pin 45	NC
Pin 22	NC	Pin 46	NC
Pin 23	NC	Pin 47	NC
Pin 24	NC	Pin 48	NC

Block Diagram

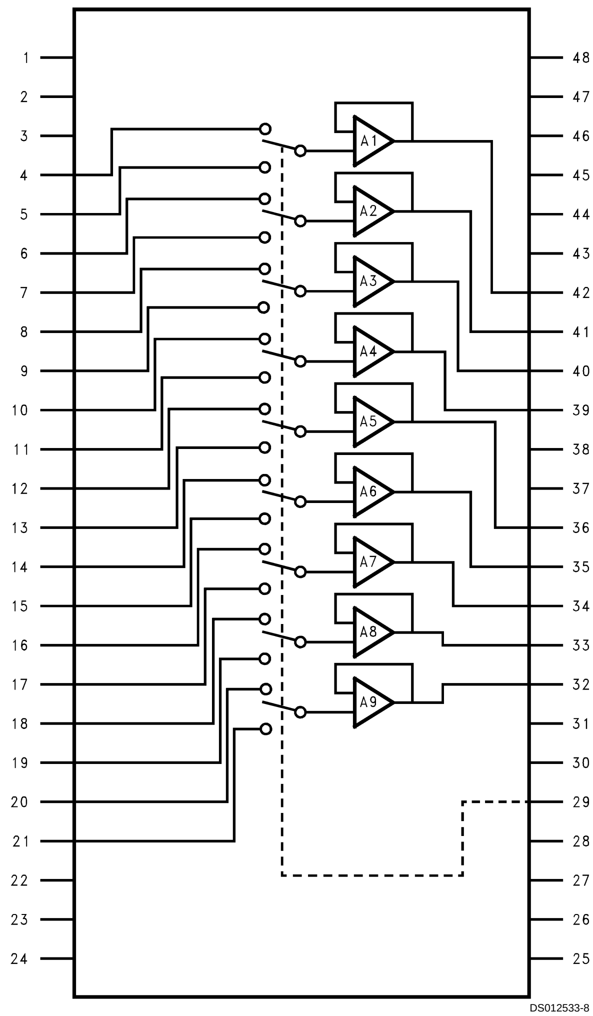


FIGURE 6. Block Diagram of LMC6009

Applications

The LMC6009 is useful for buffering the nine reference voltages for gamma correction in a TFT-LCD as shown in *Figure 7*. The A/B channel inputs allow the user to alternate two sets of gamma references to compensate for asymmetrical Gamma characteristic during Row Inversion. The LMC6009 eliminates the need for nine external switches or an 18-to-9 multiplexer.

Since the buffers in the LMC6009 draw extremely low bias current (1.5 µA max), large resistance values can be used in the reference voltage string. This allows the power dissipation in the gamma reference circuit to be minimized. The nine buffers are guaranteed to deliver 80 mA to the load, allowing the pixel voltages of the TFT-LCD to settle very quickly.

Applications (Continued)

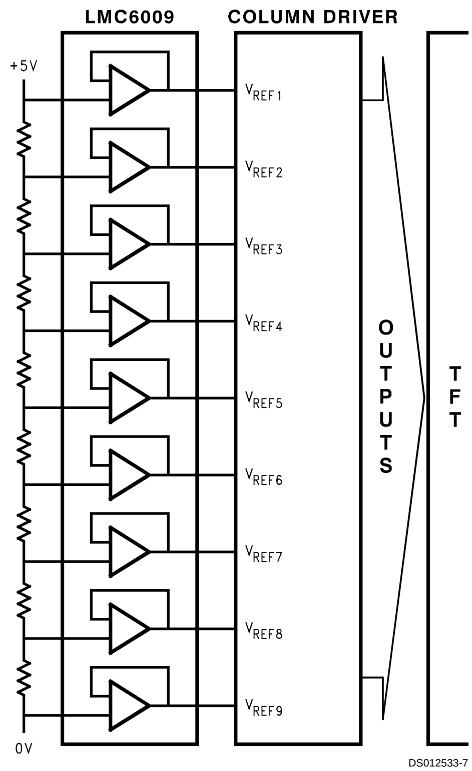


FIGURE 7.

Example: Below is a calculation of pixel charge time (for a black to black transition) in a VGA display operating at a vertical refresh rate of 60 Hz, with a panel capacitance of 50 pF per sub-pixel:

A full black to black transition represents the maximum charging time for the panel, since it requires that the panel capacitance be driven by a 4V swing from node V_{REF1} (*Figure 7*).

Total capacitive load presented to the LMC6009 is

C_L = 50 pF x 3 x 640 = 96 nF

Output current of the LMC6009 is:

I_{SC} = 80 mA

Hence, slew time t_{SLEW} = (96 nF x 4V)/80 mA = 3.07 µs

The total line time for a VGA system is approximately 34 µs. Therefore, the LMC6009 easily meets the drive requirements for the application. The input resistance seen between the V_{REFn} and $V_{REF(n+1)}$ inputs, (where n = 0 thru 8) of the Column Driver (*Figure 7*) also draw current from the LMC6009. Thus, the actual current available for charging the panel capacitance is:

Ipx = 80 mA - (V_{VREF1}–V_{VREF2})/R_{CD}

where

$V_{V\ REFn}$ = Voltage at node V_{REFn},

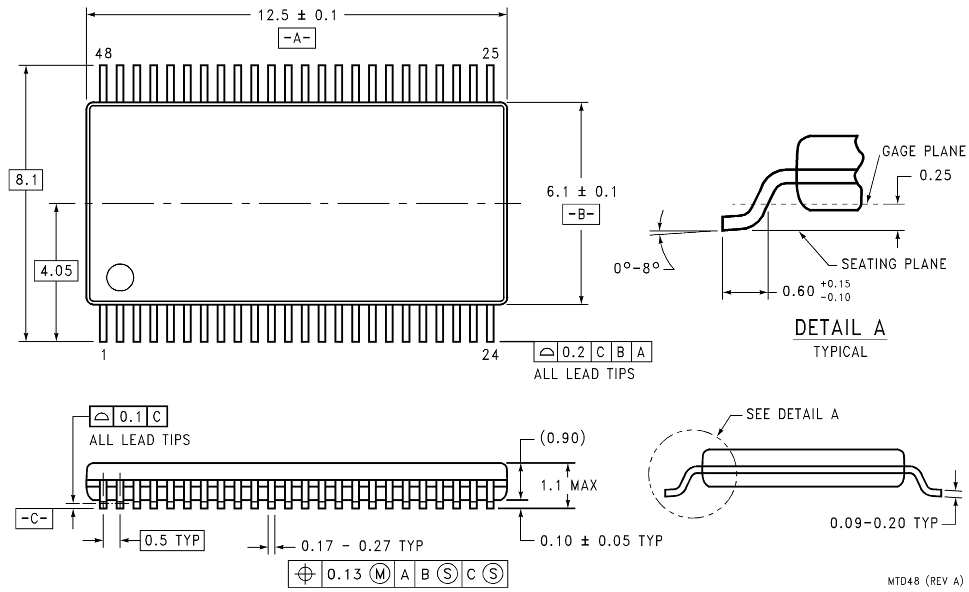
$V_{VREF(n+1)}$ = Voltage at node $V_{REF(n+1)}$, and

R_{CD} = Column driver input resistance between

VREFn and VREF(n+1)

Since the LMC6009 is capable of sourcing 80 mA, the pixel charging time is primarily limited only by the length of the R_{CD}. C_L time constant. To implement a high quality display, column drivers that allow the shortest possible time constant (lower values of R_{CD}) are desirable. However, lower values of R_{CD} result in increased system quiescent power dissipation. It is therefore important to optimize system performance by carefully considering speed vs power tradeoffs.

Physical Dimensions inches (millimeters) unless otherwise noted



All dimensions are in millimeters

48-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48

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