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August 2005

DS90C401
Dual Low Voltage Differential Signaling (LVDS) Driver

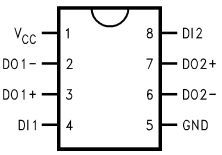
General Description

The DS90C401 is a dual driver device optimized for high data rate and low power applications. This device along with the DS90C402 provides a pair chip solution for a dual high speed point-to-point interface. The DS90C401 is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is in a 8 lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 340 mV.

Features

- Ultra low power dissipation
- Operates above 155.5 Mbps
- Standard TIA/EIA-644
- 8 Lead SOIC Package saves space
- Low Differential Output Swing typical 340 mV

Connection Diagram



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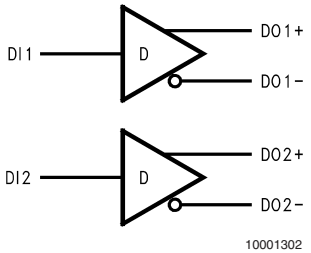
Order Number DS90C401M
See NS Package Number M08A

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Output Voltage (D_{OUT+}, D_{OUT-})	−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration (D_{OUT+}, D_{OUT-})	Continuous
Maximum Package Power Dissipation @ +25˚C	
M Package	1068 mW
Derate M Package	8.5 mW/˚C above +25˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature Range Soldering (4 sec.)	+260˚C
Maximum Junction Temperature	+150˚C
ESD Rating	
(HBM, 1.5 kΩ, 100 pF)	≥ 3,500V
(EIAJ, 0 Ω, 200 pF)	≥ 250V

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Operating Free Air Temperature (T_A)	−40	+25	+85	˚C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	D_{OUT-}, D_{OUT+}	250	340	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.41	1.60	V
V_{OL}	Output Voltage Low			0.90	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 8)			−3.5	−5.0	mA
V_{IH}	Input Voltage High		D_{IN}	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{CC}	No Load Supply Current	D_{IN} = V_{CC} or GND	V_{CC}		1.7	3.0	mA
		D_{IN} = 2.5V or 0.4V			3.5	5.5	mA
I_{CCL}	Loaded Supply Current	R_L = 100Ω All Channels V_{IN} = V_{CC} or GND (all inputs)			8	14.0	mA

Switching Characteristics

V_{CC} = +5.0V ±10%, T_A = −40˚C to +85˚C (Notes 3, 4, 5, 6, 9)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (*Figure 2* and *Figure 3*)	0.5	2.0	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	2.1	3.5	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	80	900	ps
t_{SK1}	Channel-to-Channel Skew (Note 4)		0	0.3	1.0	ns
t_{SK2}	Chip to Chip Skew (Note 5)				3.0	ns
t_{TLH}	Rise Time			0.35	2.0	ns
t_{THL}	Fall Time			0.35	2.0	ns

Parameter Measurement Information

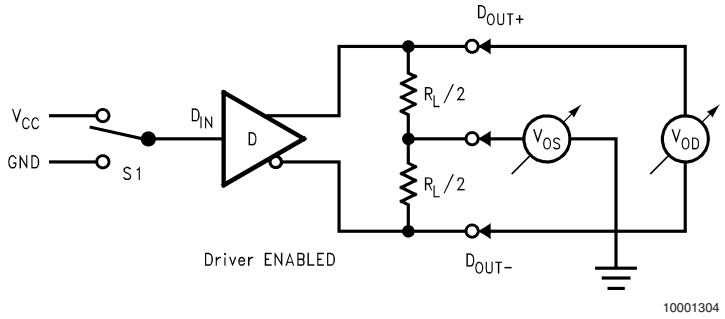


FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit

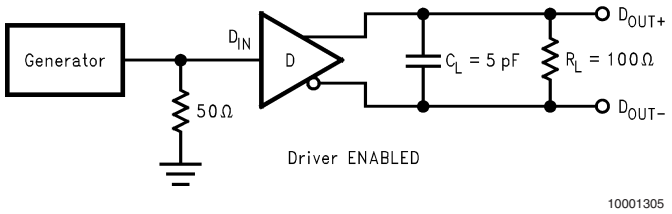


FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

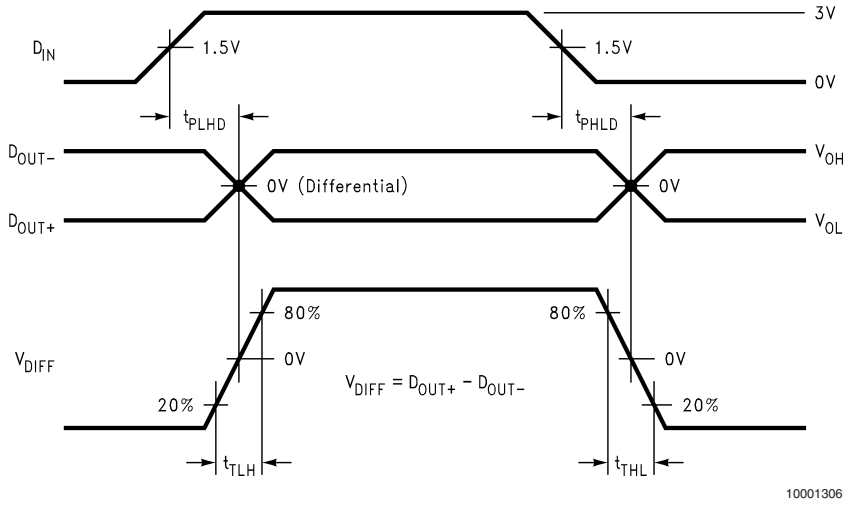


FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

Typical Application

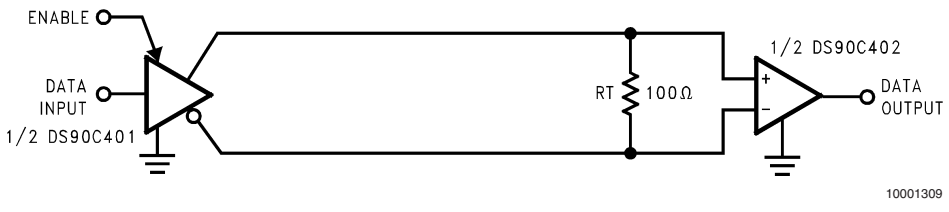


FIGURE 4. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 4*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C401 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.4 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 4*. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV – 100 mV = 240 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in *Figure 5*. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

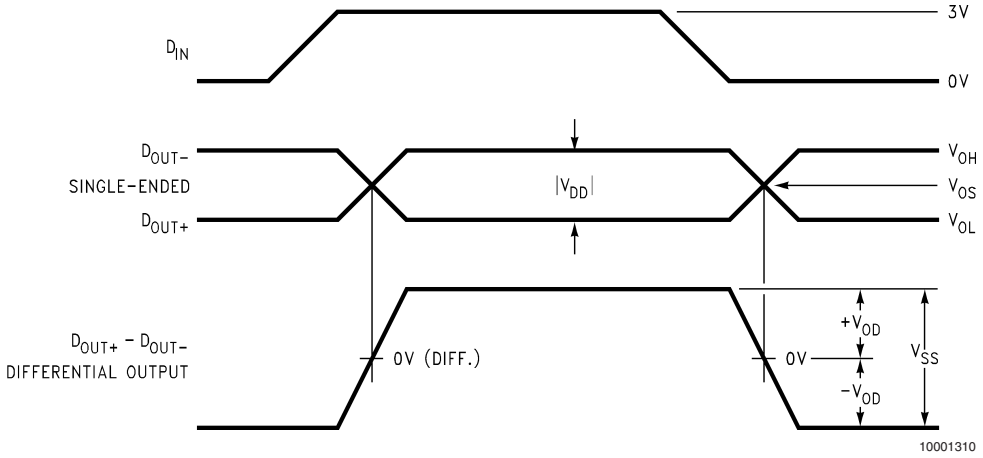


FIGURE 5. Driver Output Levels

Pin Descriptions

TABLE 1. Device Pin Descriptions

Pin No.	Name	Description
4, 8	D_{IN}	TTL/CMOS driver input pins
3, 7	D_{OUT+}	Non-inverting driver output pin
2, 6	D_{OUT-}	Inverting driver output pin
5	GND	Ground pin
1	V_{CC}	Positive power supply pin, +5.0V ± 10%

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40˚C to +85˚C	SOP/M08A	DS90C401M

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25˚C.

Note 4: Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.

Note 5: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Note 6: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, $t_r \le 6$ ns, and $t_f \le 6$ ns.

Note 7: ESD Ratings:

HBM (1.5 kΩ, 100 pF) ≥ 3,500V

EIAJ (0Ω, 200 pF) ≥ 250V

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 9: C_L includes probe and jig capacitance.

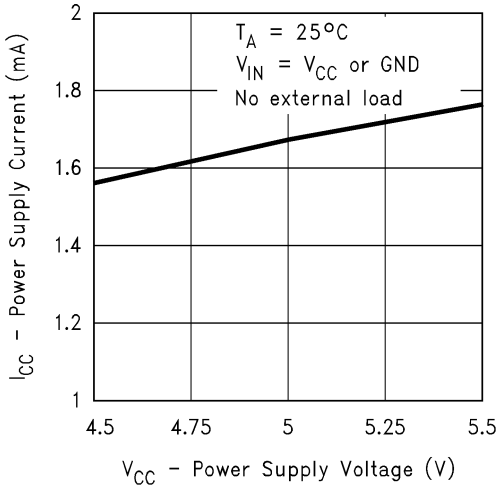
Truth Table

D_{IN}	D_{OUT+}	D_{OUT-}
L	L	H
H	H	L
D_{IN} > 0.8V and D_{IN} < 2.0V	X	X

H = Logic high level
L = Logic low level
X = Indeterminant state

Typical Performance Characteristics

Power Supply Current vs Power Supply Voltage



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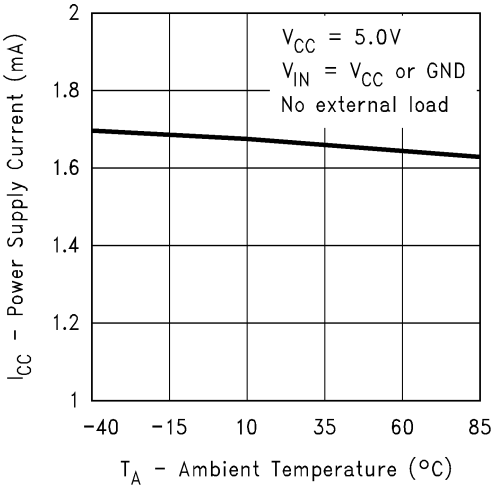
Power Supply Current vs Temperature



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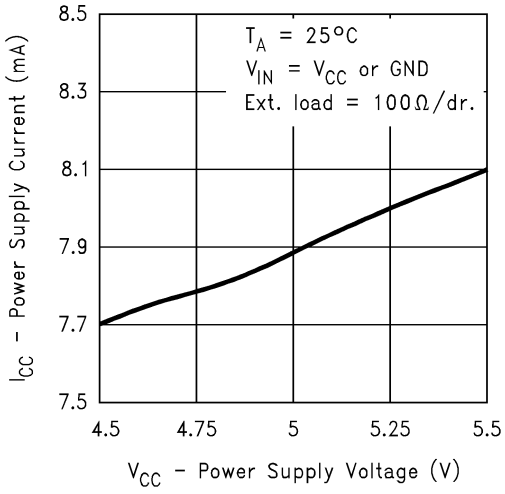
Typical Performance Characteristics (Continued)

Power Supply Current vs Power Supply Voltage



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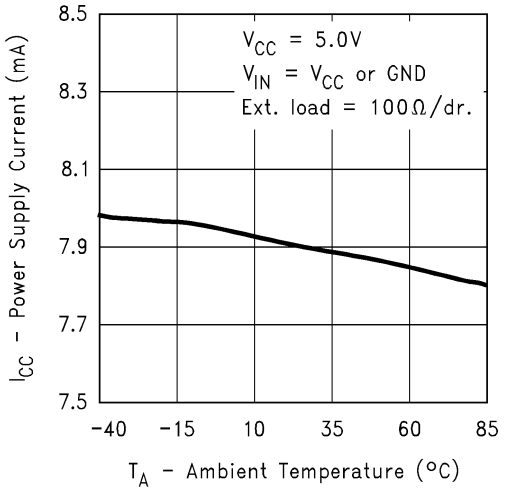
Power Supply Current vs Temperature



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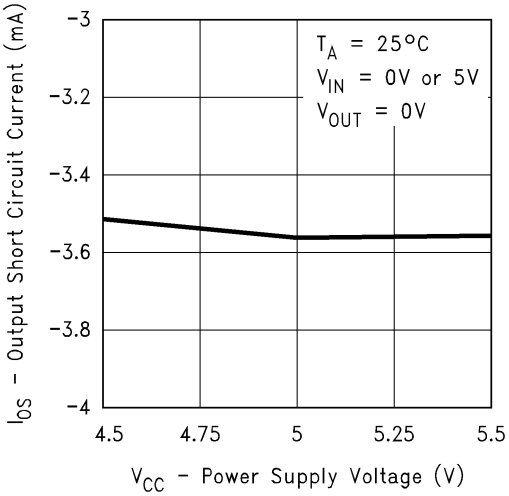
Output Short Circuit Current vs Power Supply Voltage



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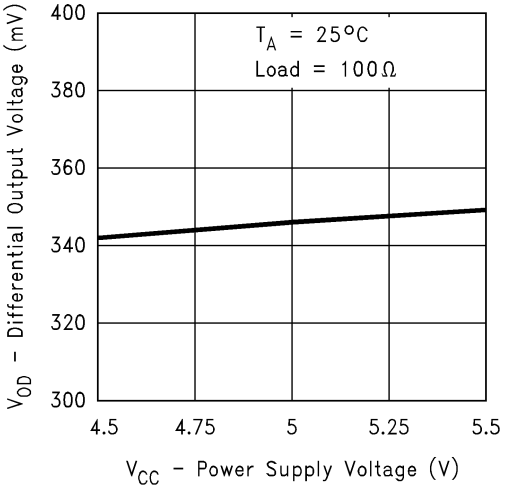
Differential Output Voltage vs Power Supply Voltage



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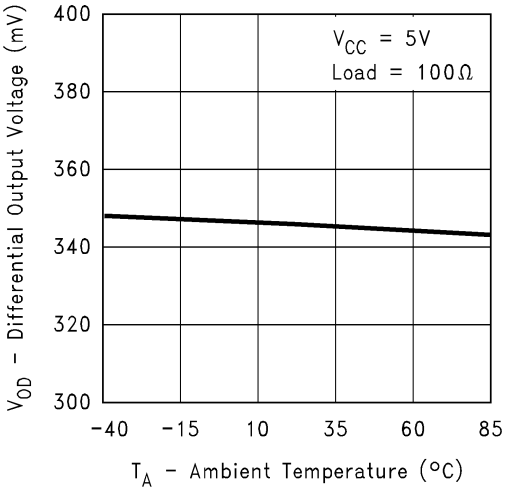
Typical Performance Characteristics (Continued)

Differential Output Voltage vs Ambient Temperature



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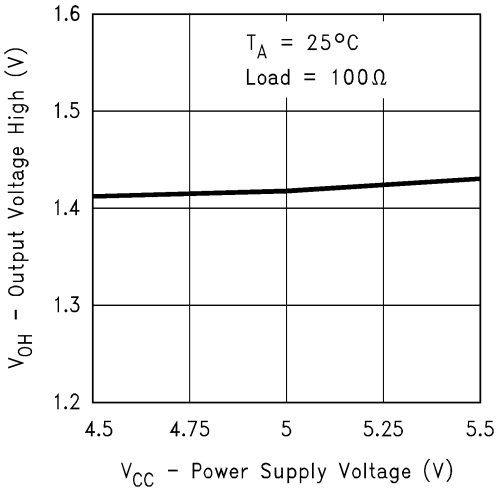
Output Voltage High vs Power Supply Voltage



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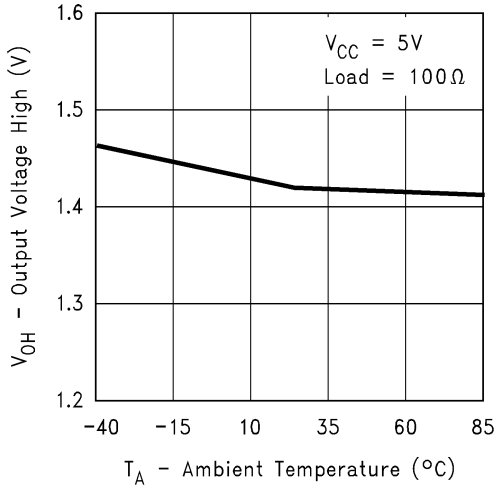
Output Voltage High vs Ambient Temperature



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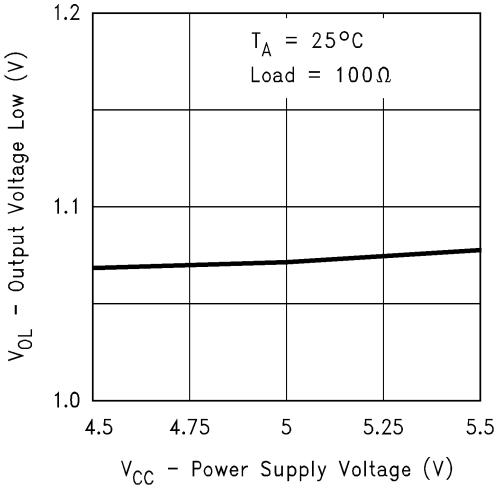
Output Voltage Low vs Power Supply Voltage



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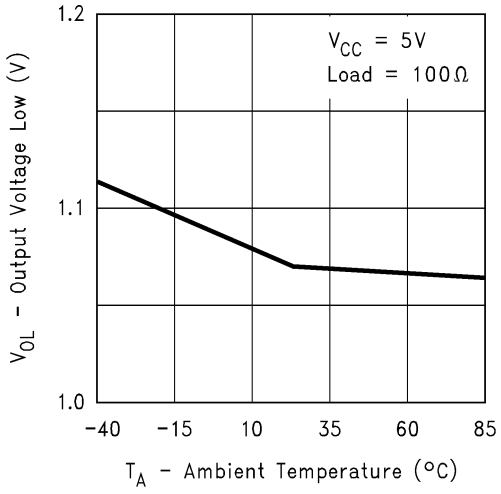
Typical Performance Characteristics (Continued)

Output Voltage Low vs Ambient Temperature



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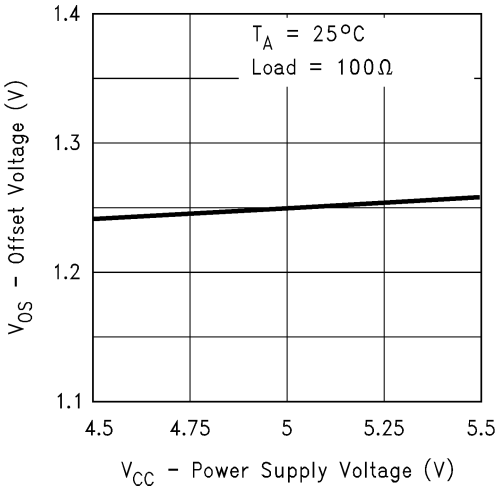
Offset Voltage vs Power Supply Voltage



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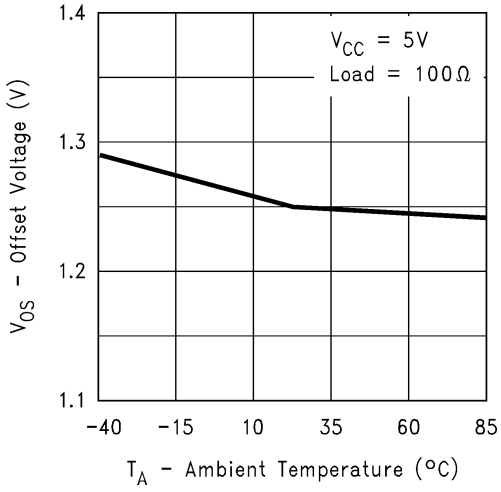
Offset Voltage vs Ambient Temperature



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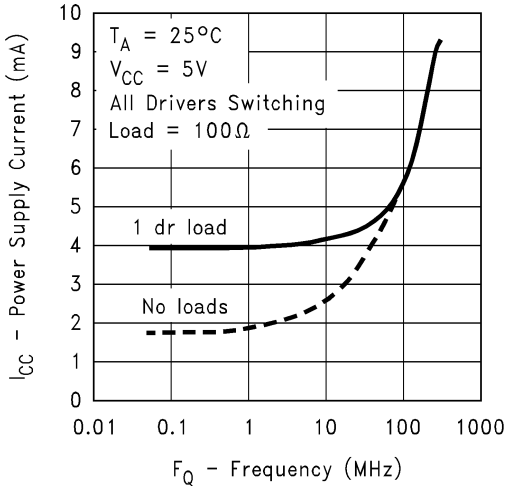
Power Supply Current vs Frequency



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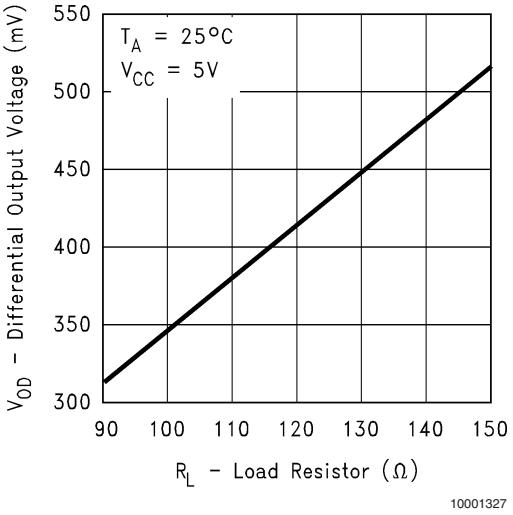
Typical Performance Characteristics (Continued)

Differential Output Voltage vs Load Resistor



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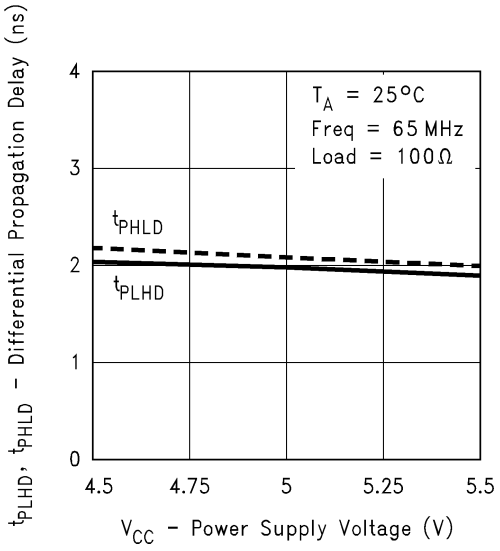
Differential Propagation Delay vs Power Supply Voltage



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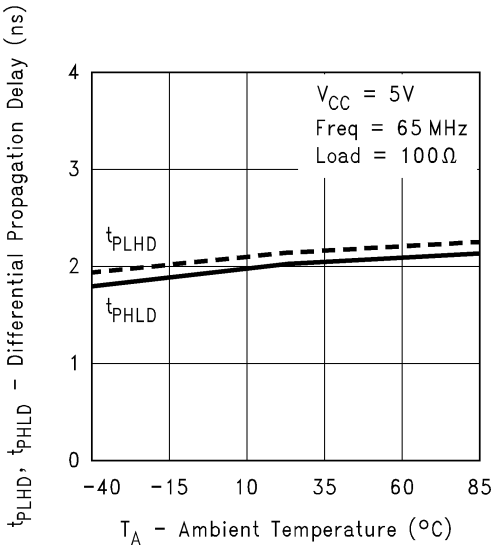
Differential Propagation Delay vs Ambient Temperature



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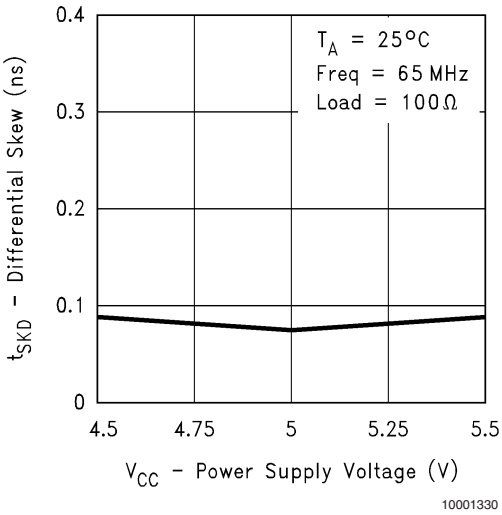
Differential Skew vs Power Supply Voltage



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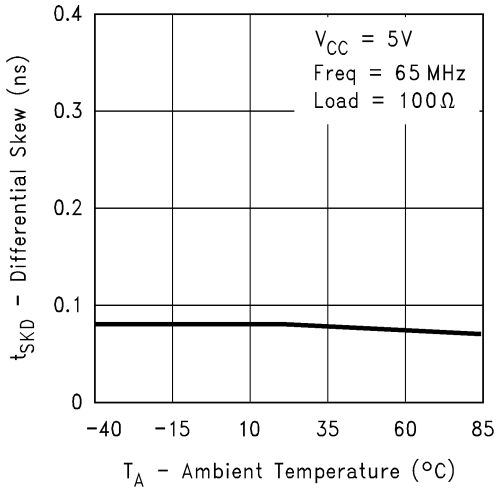
Typical Performance Characteristics (Continued)

Differential Skew vs Ambient Temperature



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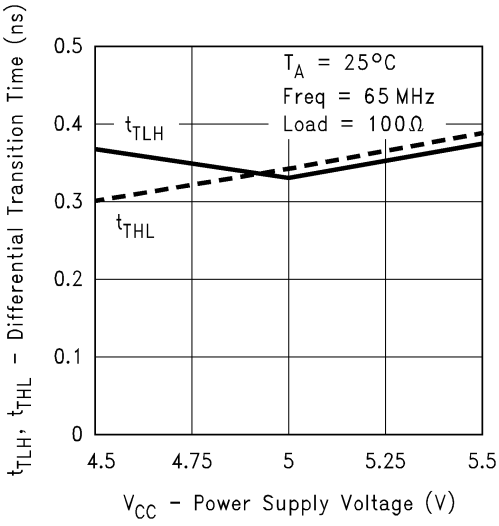
Differential Transition Time vs Power Supply Voltage



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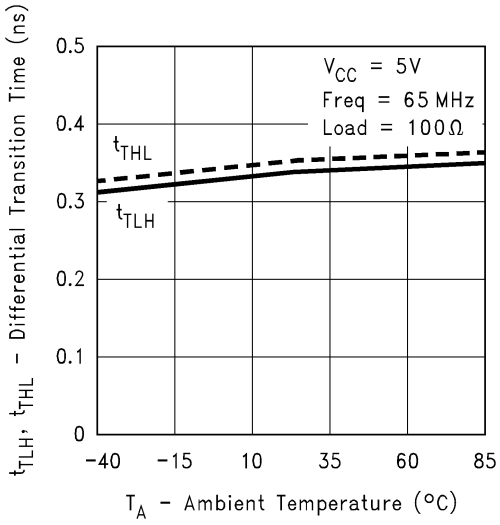
Differential Transition Time vs Ambient Temperature



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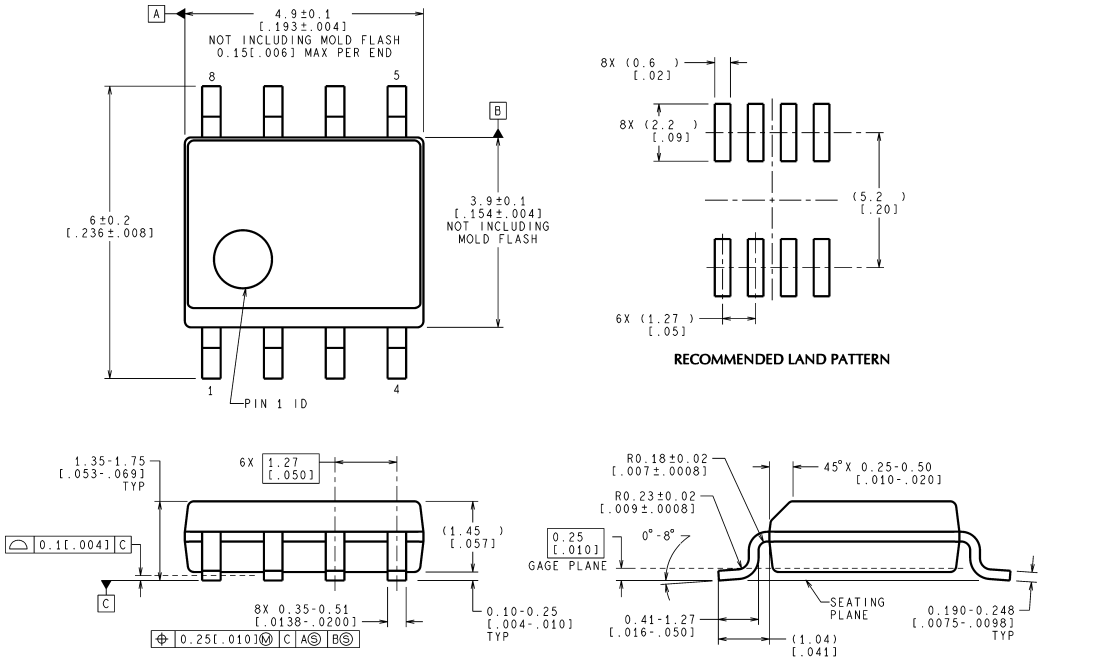
Physical Dimensions inches (millimeters) unless otherwise noted



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M08A (Rev K)

8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number DS90C401M
NS Package Number M08A

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