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SEMICONDUCTOR
PRODUCT BRIEF

MPC561/MPC562
MPC563/MPC564

Product Brief

MPC561/MPC562 / MPC563/MPC564 RISC MCU Including Peripheral Pin Multiplexing with Flash and Code Compression Options

Features

The MPC561/MPC562 / MPC563/MPC564 are members of the Motorola MPC500 RISC Microcontroller family. As shown in the block diagram, they are composed of:

- High performance CPU system
  - — High performance core
    - Single issue integer core
    - Compatible with PowerPC instruction set architecture
    - Precise exception model
    - Floating point
    - Extensive system development support
      - — On-chip watchpoints and breakpoints
      - — Program flow tracking
      - — Background debug mode (BDM)
      - — IEEE-ISTO Nexus 5001-1999 Class 3 Debug Interface
  - — MPC500 system interface (USIU, BBC, L2U)
  - — Fully static design
  - — Four major power saving modes
    - On, doze, sleep, deep-sleep and power-down
  - — 32-Kbyte static RAM (CALRAM)
  - — 512-Kbyte flash (UC3F) on MPC563/MPC564
  - — General-purpose I/O support
    - On address (24) and data (32) pins
    - 16 GPIO in MIOS14
    - Many peripheral pins can be used as GPIO when not used as primary functions
    - 2.6-V outputs on external bus pins
- PPM (peripheral pin multiplexing with parallel-to-serial driver) module
- Available in package or die
  - — Plastic ball grid array (PBGA) packaging

Key Feature Details

MPC500 System Interface (USIU)

- System configuration and protection features:
  - — Periodic-interrupt timer
  - — Bus monitor
  - — Software watchdog timer
  - — Real-time clock (RTC)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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— Decrementer
— Time base
- Clock synthesizer
- Power management
- Reset controller
- External bus interface that tolerates 5-V inputs, provides 2.6-V outputs and supports multiple-master designs
- Enhanced interrupt controller that supports up to eight external and 40 internal interrupts, simplifies the interrupt structure and decreases interrupt processing time
- USIU supports dual mapping to map part of one internal/external memory to another external memory
- USIU supports dual mapping of flash on MPC563 and MPC564 to move part of internal flash memory to external bus for development
- External bus, supporting non-wraparound burst for instruction fetches, with up to 8 instructions per memory cycle

Burst Buffer Controller (BBC) Module

- Support for enhanced interrupt controller (EIC)
- Support for enhanced exception table relocation feature
- Branch target buffer
- Contains 2-Kbytes of decompression RAM (DECRAM) for code compression. This RAM may also be used as general-purpose RAM when code compression feature not used.

Flexible Memory Protection Unit

- Flexible memory protection units (MPU) in BBC and L2U
- Default attributes available in one global entry
- Attribute support for speculative accesses
- Up to eight memory regions are supported, four for data and four for instructions

Memory Controller

- Four flexible chip selects via memory controller
- 24-bit address and 32-bit data buses
- 4-Kbyte to one 16-Mbyte (data) or four-Gbyte (instruction) region size support
- Supports enhanced external burst
- Up to eight-beat transfer bursts, two-clock minimum bus transactions
- Use with SRAM, EPROM, flash and other peripherals
- Byte selects or write enables
- 32-bit address decodes with bit masks
- Four regions

512-Kbytes of CDR3 Flash EEPROM Memory (UC3F) – MPC563 Only

- One 512-Kbyte module
- Page read mode
- Block (64 Kbytes) erasable
- External 4.75- to 5.25-V VFLASH power supply for program, erase, and read operations

32-Kbyte static RAM (CALRAM)

- Composed of one 32-Kbyte CALRAM module
  — 28-Kbyte static RAM
  — 4-Kbyte calibration (overlay) RAM feature that allows calibration of flash-based constants
- Eight 512-byte overlay regions
- One clock fast accesses
- Two-clock cycle access option for power saving
- Keep-alive power (VDDSRAM) for data retention

General-Purpose I/O Support

- 24 Address pins and 32 data pins can be used for general-purpose I/O in single-chip mode
- 16 GPIO in MIOS14
- Many peripheral pins can be used as GPIO when not used as primary functions
- 2.6-V outputs on external bus pins
- 5-V outputs with slew rate control

NEXUS Debug Port (Class 3)

- Compliant with Class 3 of the IEEE-ISTO Nexus 5001-1999
- Program trace via branch trace messaging (BTM)
- Data trace via data write messaging (DWM) and data read messaging (DRM)
- Ownership trace via ownership trace messaging (OTM)
- Run-time access to on-chip memory map and MPC5xx special purpose registers (SPRs) via the READI read/write access protocol
- Watchpoint messaging via the auxiliary port
- Reduced-port mode (1 MDI, 2 MDO) or full-port mode (2 MDI. 8 MDO)
- All features configurable and controllable via the auxiliary port
- Security features for production environment
- Supports the RCPU debug mode via the auxiliary port
- READI module can be reset independent of system reset

Integrated I/O System

Two Time Processor Units (TPU3)

- True 5-V I/O
- Two time processing units (TPU3) with16 channels each
- Each TPU3 is a micro-coded timer subsystem
- Eight-Kbytes of dual port TPU RAM (DPTRAM) shared by two TPU3 modules for TPU micro-code

22-Channel Modular I/O System (MIOS14)

- Six modulus counter sub-modules (MCSM)
- 10 double-action sub-modules (DASM)
- 12 dedicated PWM sub-modules (PWMSM)
- One MIOS14 16-bit parallel port I/O sub-modules (MPIOSM)

Two Enhanced Queued Analog-to-Digital Converter Modules (QADC64E)

- Two queued analog-to-digital converter modules (QADC64_A, QADC64_B) providing a total of 32 analog channels
- 16 analog input channels on each QADC64E module using internal multiplexing
- Directly supports up to four external multiplexers
- Up to 41 total input channels on the two QADC64E modules with external multiplexing
- Software configurable to operate in Enhanced or Legacy (MPC555 compatible) mode
- Unused analog channels can be used as digital input/output pins
  - — GPIO on all channels in Enhanced mode
- 10-bit A/D converter with internal sample/hold
- Typical conversion time of less than 5 µs (>200 K samples/second)
- Two conversion command queues of variable length
- Automated queue modes initiated by:
  - — External edge trigger
  - — Software command
  - — Periodic/interval timer within QADC64E module, that can be assigned to both queue 1 and 2
  - — External Gated trigger (queue 1only)
- 64 result registers
  - — Output data is right- or left-justified, signed or unsigned

- Alternate reference input (ALTREF), with control in the conversion command word (CCW)

Three CAN 2.0B Controller (TouCAN) Modules

- Three TouCAN modules (TOUCAN_A, TOUCAN_B, TOUCAN_C)
- Each TouCAN provides the following features:
  - — 16 message buffers each, programmable I/O modes
  - — Maskable interrupts
  - — Independent of the transmission medium (external transceiver is assumed)
  - — Open network architecture, multi-master concept
  - — High immunity to EMI
  - — Short latency time for high-priority messages
  - — Low-power sleep mode, with programmable wake-up on bus activity
  - — TOUCAN_C pins are shared with MIOS14 GPIO or QSMCM

Queued Serial Multi-Channel Module (QSMCM)

- One queued serial module with one queued SPI and two SCIs (QSMCM)
- QSMCM matches full MPC555 QSMCM functionality
- Queued SPI
  - — Provides full-duplex communication port for peripheral expansion or inter-processor communication
  - — Up to 32 preprogrammed transfers, reducing overhead
  - — Synchronous serial interface with baud rate of up to system clock / 4
  - — Four programmable peripheral-selects pins:
  - — Support up to 16 devices with external decoding
  - — Support up to eight devices with internal decoding
  - — Special wrap-around mode allows continuous sampling of a serial peripheral for efficient interfacing to serial analog-to-digital (A/D) converters
- SCI
  - — UART mode provides NRZ format and half- or full-duplex interface
  - — 16 register receive buffers and 16 register transmit buffers on one SCI
  - — Advanced error detection and optional parity generation and detection
  - — Word-length programmable as eight or nine bits
  - — Separate transmitter and receiver enable bits, and double buffering of data
  - — Wake-up functions allow the CPU to run uninterrupted until either a true idle line is detected, or a new address byte is received

Peripheral Pin Multiplexing (PPM) PPM

- Synchronous serial interface between the microprocessor and an external device
- Four internal parallel data sources can be multiplexed through the PPM
  - — TPU3_A: 16 channels
  - — TPU3_B: 16 channels
  - — MIOS14: 12 PWM channels, 4 MDA channels
  - — Internal GPIO: 16 general-purpose inputs, 16 general-purpose outputs
- Software configurable stream size
- Software configurable clock (TCLK) based on system clock
- Software selectable clock modes (SPI mode and TDM mode)
- Software selectable operation modes
  - — Continuous mode
  - — Start-transmit-receive (STR) mode
- Software configurable internal modules interconnect (shorting)

MPC561/MPC562 / MPC563/MPC564 Optional Features

The following are optional features of the MPC561/MPC562 / MPC563/MPC564:

- 56-MHz operation (40 MHz is default)
- Code compression supported on the MPC562 and the MPC564
  - — Compression reduces instruction memory requirements by 40-50%
  - — Compression optimized for automotive (non-cached) applications
- 512 Kbytes flash (available on the MPC563/MPC564 only)
  - — Single array
  - — Page mode read
  - — Block (64 Kbytes) erasable
  - — External 4.75- to 5.25-V VFLASH program, erase, and read power supply

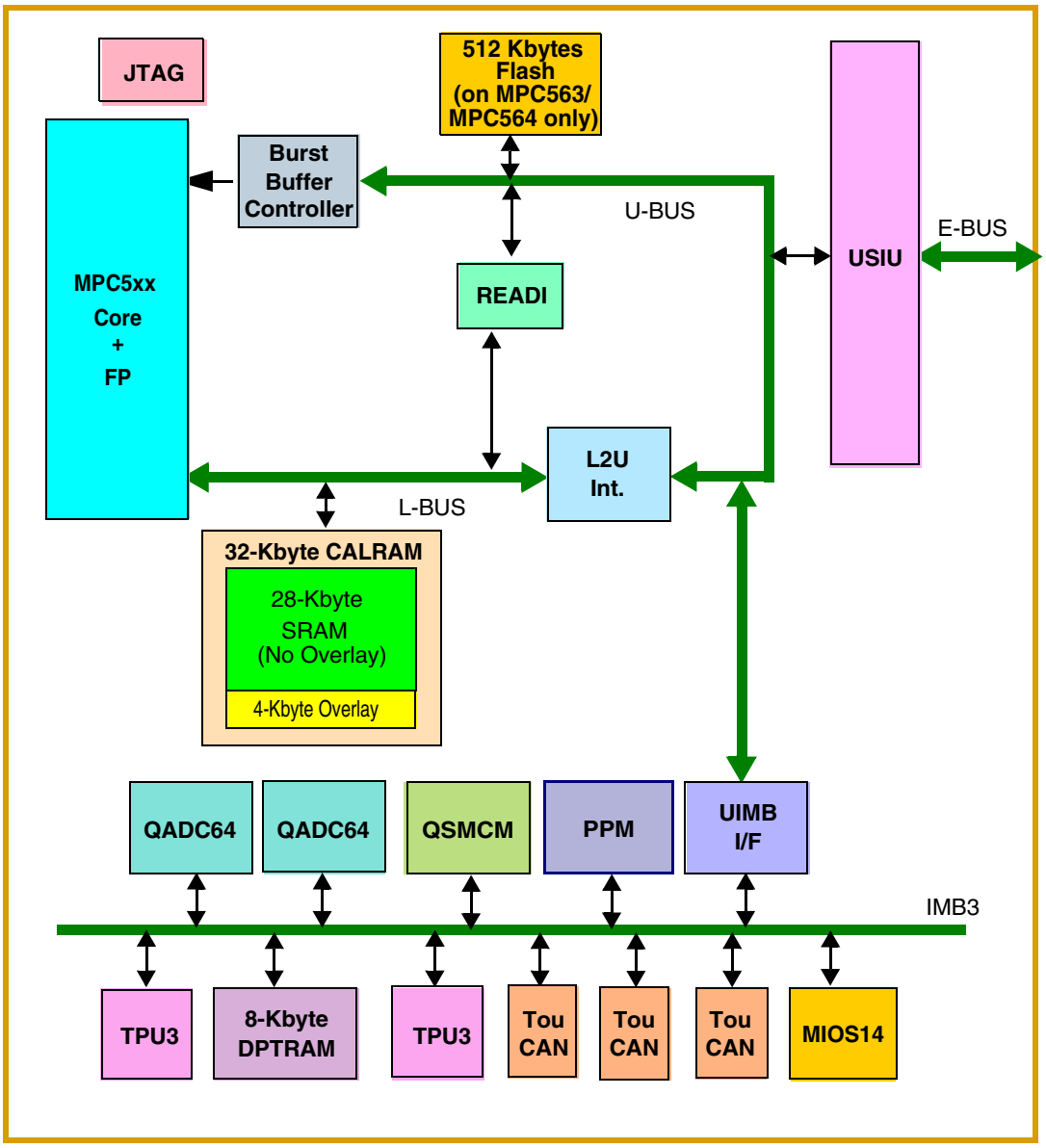
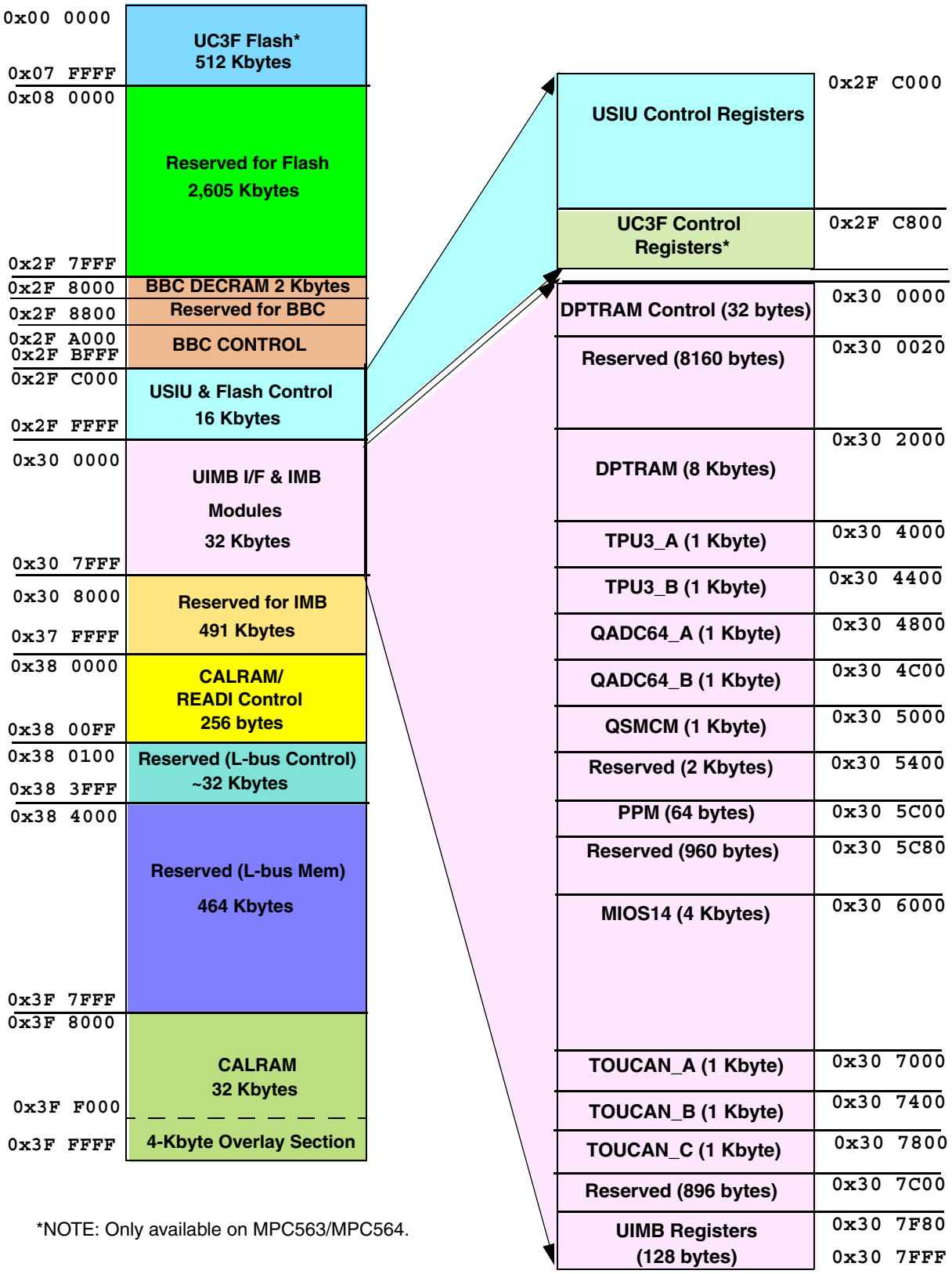


Figure 1 MPC561/MPC562 / MPC563/MPC564 Block Diagram



*NOTE: Only available on MPC563/MPC564.

Figure 2 MPC561 / MPC563 Internal Memory Map

MPC561 / MPC563 Ball Map
(As viewed from top, through the package and silicon)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VDD	VSS	VSS	VSS	A_TPUCH3	A_TPUCH7	A_TPUCH11	A_TPUCH15	VSSA	VRL	A_AN3_ANZ_PQB3	A_AN51_PQB7	A_AN55_PQA3	A_AN56_PQA4	B_AN0_ANW_PQB0	B_AN48_PQB4	B_AN52_MA0_PQA0	B_AN56_PQA4	VSS	ETRIG2_PCS7	MDA13	MDA28	VSS	VSS	VDD	VSS	A
B	VSS	VDD	VSS	VSS	A_TPUCH2	A_TPUCH6	A_TPUCH10	A_TPUCH14	VSSA	ALTREF	A_AN2_ANY_PQB2	A_AN50_PQB6	A_AN54_MA2_PQA2	A_AN58_PQA6	B_AN1_ANX_PQB1	B_AN49_PQB5	B_AN53_MA1_PQA1	B_AN57_PQA5	VSS	ETRIG1_PCS6	MDA14	MDA29	VSS	VDD	VSS	QVDDL	B
C	VSS	VSS	VDD	VSS	A_TPUCH1	A_TPUCH4	A_TPUCH8	A_TPUCH12	NVDDL	VRH	A_AN0_ANW_PQB0	A_AN48_PQB4	A_AN52_MA0_PQA0	A_AN59_PQA7	B_AN2_ANY_PQB2	B_AN50_PQB6	B_AN54_MA2_PQA2	B_AN58_PQA6	VDDH	MDA11	MDA15	VDDH	VDD	VSS	QVDDL	VSS	C
D	VSS	VSS	VSS	VDD	VSS	A_TPUCH5	A_TPUCH9	A_TPUCH13	NVDDL	VDDA	A_AN1_ANX_PQB1	A_AN49_PQB5	A_AN53_MA1_PQA1	A_AN57_PQA5	B_AN3_ANZ_PQB3	B_AN51_PQB7	B_AN55_PQA3	B_AN59_PQA7	VDDH	MDA12	MDA27	VDD	VSS	QVDDL	VSS	VSS	D
E	VDDH	VSS	VSS	VSS																			QVDDL	VSS	VSS	VSS	E
F	B_T2CLK_PCS4	A_T2CLK_PCS5	A_TPUCH0	QVDDL																			VDDH	MDA30	MDA31	MPWM0_MDI1	F
G	B_TPUCH12	B_TPUCH13	B_TPUCH14	B_TPUCH15																			MPWM1_MDO2	MPWM16	MPWM3_PPM_RX1	MPWM2_PPM_TX1	G
H	B_TPUCH8	B_TPUCH9	B_TPUCH10	B_TPUCH11																			MPWM17_MDO3	MPWM18_MDO6	MPWM19_MDO7	MPIO32B5_MDO5	H
J	B_TPUCH4	B_TPUCH5	B_TPUCH6	B_TPUCH7																			MPIO32B6_MPWM4_MDO6	MPIO32B7_MPWM5	MPIO32B8_MPWM20	MPIO32B9_MPWM21	J
K	B_TPUCH0	B_TPUCH1	B_TPUCH2	B_TPUCH3																			MPIO32B12_C_CNTX0	MPIO32B11_C_CNRX0	MPIO32B10_PPM_TSYNC	MPIO32B13_PPM_TCLK	K
L	JCOMP_RSTI_B	TCK_DSCK_MCKI	B_CNRX0	B_CNTX0																			VF0_MPIO32B0_MDO1	VF1_MPIO32B1_MCKO	MPIO32B15_PPM_TX0	MPIO32B14_PPM_RX0	L
M	TDI_DSDI_MDI0	TMS_EVTI_B	VDDSRAM	TDO_DSDO_MDO0																			A_CNTX0	VF2_MPIO32B2_MSEI_B	VFLS0_MPIO32B3_MSEO_B	VFLS1_MPIO32B4	M
N	IRQ3_B_KR_B_RETRY_B_SGPIOC3	IWP0_VFLS0	IWP1_VFLS1	SGPIOC6_FRZ_PTR_B																			PCS2_QGPIO2	PCS1_QGPIO1	PCS0_SS_B_QGPIO0	A_CNRX0	N
P	IRQ4_B_AT2_SGPIOC4	IRQ2_B_CR_B_SGPIOC2_MDO5_MTS	IRQ0_B_SGPIOC0_MDO4	IRQ1_B_RSV_B_SGPIOC1																			SCK_QGPIO6	MOSI_QGPIO5	MISO_QGPIO4	PCS3_QGPIO3	P
R	SGPIOC7_IRQOUT_B_LWP0	BB_B_VF2_IWP3	BG_B_VF0_LWP1	BR_B_VF1_IWP2																			RXD1_QGPI1	TXD2_QGPO2_C_CNTX0	TXD1_QGPO1	PULL-SEL	R
T	WE_B_AT0	WE_B_AT1	WE_B_AT2	WE_B_AT3																			EPEE	BOEPEE	VDDH	RXD2_QGPI2_C_CNRX0	T
U	CS0_B	CS1_B	CS2_B	CS3_B																			CLKOUT	VSSF	VDDF	VFLASH	U
V	RD_WR_B	OE_B	TEA_B	TSIZ0																			VDD	EXTCLK	VSS	ENGCLK_BUCLK	V
W	TSIZ1	TS_B	TA_B	BDIP_B																			HRESET_B	SRESET_B	PORESET_B_TRST_B	KAPWR	W
Y	BURST_B	BI_B_STS_B	ADDR_SGPIOA12	ADDR_SGPIOA11																			NVDDL	IRQ7_B_MODCK3	RSTCONF_B_TEXP	VDDSYN	Y
AA	VSS	VSS	VSS	QVDDL																			VSS	VSS	VSS	XFC	AA
AB	VSS	VSS	QVDDL	VSS																			QVDDL	VSS	VSS	VSSSYN	AB
AC	VSS	QVDDL	VSS	NVDDL	VSS	ADDR_SGPIOA10	ADDR_SGPIOA18	ADDR_SGPIOA20	ADDR_SGPIOA23	NVDDL	ADDR_SGPIOA26	DATA_SGPIOD1	DATA_SGPIOD5	DATA_SGPIOD7	NVDDL	DATA_SGPIOD9	DATA_SGPIOD11	DATA_SGPIOD12	NVDDL	DATA_SGPIOD14	VSS	VDD	VSS	QVDDL	VSS	EXTAL	AC
AD	QVDDL	VSS	NVDDL	VSS	VSS	QVDDL	ADDR_SGPIOA13	ADDR_SGPIOA16	ADDR_SGPIOA19	ADDR_SGPIOA21	ADDR_SGPIOA24	ADDR_SGPIOA25	DATA_SGPIOD0	DATA_SGPIOD28	DATA_SGPIOD26	DATA_SGPIOD24	DATA_SGPIOD22	DATA_SGPIOD13	DATA_SGPIOD15	DATA_SGPIOD16	IRQ5_B_SGPIOC5_MODCK1	VSS	VDD	VSS	QVDDL	XTAL	AD
AE	VSS	NVDDL	VSS	VSS	VSS	QVDDL	ADDR_SGPIOA14	ADDR_SGPIOA17	ADDR_SGPIOA31	ADDR_SGPIOA30	ADDR_SGPIOA28	ADDR_SGPIOA29	DATA_SGPIOD30	DATA_SGPIOD29	DATA_SGPIOD27	DATA_SGPIOD25	DATA_SGPIOD23	DATA_SGPIOD21	DATA_SGPIOD19	DATA_SGPIOD17	IRQ6_B_MODCK2	VSS	VSS	VDD	VSS	QVDDL	AE
AF	NVDDL	VSS	VSS	VSS	VDDH	VSS	ADDR_SGPIOA15	ADDR_SGPIOA9	ADDR_SGPIOA8	ADDR_SGPIOA22	ADDR_SGPIOA27	DATA_SGPIOD31	DATA_SGPIOD3	DATA_SGPIOD2	DATA_SGPIOD4	DATA_SGPIOD6	DATA_SGPIOD8	DATA_SGPIOD10	DATA_SGPIOD20	DATA_SGPIOD18	VDDH	VSS	VSS	VSS	VDD	VSS	AF

NOTE: The flash balls are only available on the MPC563 and MPC564. These are no connect balls on the MPC561 and MPC562. Flash supplies and inputs are located on the following balls: T23, T24, U24, U25. U26.

Figure 3 MPC561 / MPC563 Ball Map

Ordering Information

Table 1 MPC561/562 / MPC563/564

Device Name	Order Part Number[1]	Package Info	Temperature Range	Maximum Frequency	Code Compression
MPC561	MPC561MZP40	388 PBGA	-40 – 125° C	40 MHz	No
MPC561	MPC561CZP40	388 PBGA	-40 – 85° C	40 MHz	No
MPC561	MPC561MZP56	388 PBGA	-40 – 125° C	56 MHz	No
MPC561	MPC561CZP56	388 PBGA	-40 – 85° C	56 MHz	No
MPC562	MPC562MZP40	388 PBGA	-40 – 125° C	40 MHz	Yes
MPC562	MPC562CZP40	388 PBGA	-40 – 85° C	40 MHz	Yes
MPC562	MPC562MZP56	388 PBGA	-40 – 125° C	56 MHz	Yes
MPC562	MPC562CZP56	388 PBGA	-40 – 85° C	56 MHz	Yes
MPC563	MPC563MZP40	388 PBGA	-40 – 125° C	40 MHz	No
MPC563	MPC563CZP40	388 PBGA	-40 – 85° C	40 MHz	No
MPC563	MPC563MZP56	388 PBGA	-40 – 125° C	56 MHz	No
MPC563	MPC563CZP56	388 PBGA	-40 – 85° C	56 MHz	No
MPC564	MPC564MZP40	388 PBGA	-40 – 125° C	40 MHz	Yes
MPC564	MPC564CZP40	388 PBGA	-40 – 85° C	40 MHz	Yes
MPC564	MPC564MZP56	388 PBGA	-40 – 125° C	56 MHz	Yes
MPC564	MPC564CZP56	388 PBGA	-40 – 85° C	56 MHz	Yes

NOTES:
1. Add R2 suffix for parts shipped in tape and reel media.

Table 2 lists the documents that provide a complete description of the MPC561/563 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola Semiconductor documentation page on the Internet (the source for the latest information).

Table 2 Available Documentation

Document Number	Title
MPC561_3RM/AD	*MPC561/MPC563 Reference Manual*
AN1821/D	*Exception Table Relocation and Multi-Processor Address Mapping in the Embedded MPC5XX Family*
AN2109/D	*MPC555 Interrupts.*
AN2127/D	*EMC Guidelines for MPC500-Based Automotive Powertrain Systems*

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