Product Preview

SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

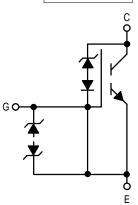
This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

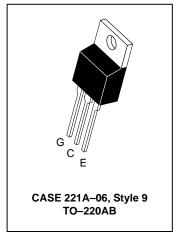
- Temperature Compensated Gate—Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- · High Pulsed Current Capability



MGP20N14CL

20 AMPERES
VOLTAGE CLAMPED
N-CHANNEL IGBT
V_{Ce(on)} = 1.9 VOLTS
135 VOLTS (CLAMPED)





MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	VCES	CLAMPED	Vdc
Collector–Gate Voltage	VCGR	CLAMPED	Vdc
Gate–Emitter Voltage	VGE	CLAMPED	Vdc
Collector Current — Continuous @ $T_C = 25^{\circ}C$ — Single Pulsed ($t_p = \pm 10 \mu s$)	I _C	20 60	Adc Apk
Total Power Dissipation @ T _C = 25°C (TO–220) Derate Above 25°C	PD	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 175	°C
Single Pulse Collector–Emitter Avalanche Energy @ Starting T _J = 25°C (V _{CC} = 80 V, V _{GE} = 5 V, Peak I _L = 10 A, L = 10 mH)	EAS	500	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{ heta JC} \ R_{ heta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	TL	275	°C
Mounting Torque, 6–32 or M3 screw	10 lbf∙in (1.13 N∙m)		

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This document contains information on a new product. Specifications and information herein are subject to change without notice.



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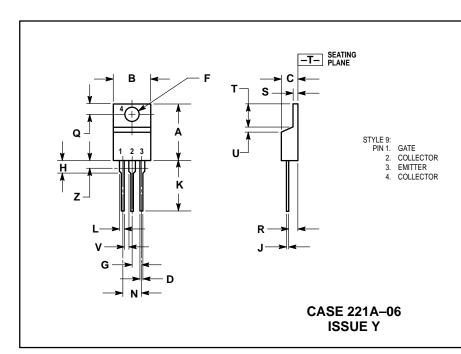
$\textbf{ELECTRICAL CHARACTERISTICS} \ (T_C = 25^{\circ}\text{C unless otherwise noted})$

Cha	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS		•				
Clamp Voltage (IClamp = 10 mA, T _J = -40 to 150°C)		BVCES	135			Vdc
Zero Gate Voltage Collector Current (VCE = 100 V, VGE = 0 V) (VCE = 100 V, VGE = 0 V, TJ = 150°C)		CES	_	_	10 100	μΑ
Gate-Emitter Clamp Voltage (IG =	1 mA)	BVGES	10			Vdc
Gate-Emitter Leakage Current (V	GE = ±5 V, V _{CE} = 0 V)	IGES	_	_	1.0	μΑ
ON CHARACTERISTICS (1)		•				
Gate Threshold Voltage (VCE = VGE, IC = 1 mA) Threshold Temperature Coefficie	ent (Negative)	VCE(th)	1.0	1.5 4.4	2.0	V mV/°C
Collector–Emitter On–Voltage (V _{GE} = 5 V, I _C = 10 A) (V _{GE} = 5 V, I _C = 10 Adc, T _J = 175°C)		VCE(on)	_		1.9 1.8	V
Forward Transconductance ($V_{CE} > 15 \text{ V}, I_{C} = 10 \text{ A}$)		9fs	8.0	15	_	Mhos
DYNAMIC CHARACTERISTICS		•				
Input Capacitance		C _{iss}	_	430	600	pF
Output Capacitance	$(V_{CE} = 25 \text{ Vdc}, V_{GE} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C _{oss}	_	182	250	1
Transfer Capacitance	,	C _{rss}	_	48	100	1
SWITCHING CHARACTERISTICS	(1)	•				
Turn-On Delay Time		td(on)	_	TBD	TBD	ns
Rise Time	$(V_{CC} = 68 \text{ V}, I_{C} = 20 \text{ A},$	t _r	_	TBD	TBD	
Turn-Off Delay Time	$V_{GE} = 5 \text{ V}, R_{G} = 9.1 \Omega$	t _d (off)	_	TBD	TBD	1
Fall Time		t _f	-	TBD	TBD	1
Total Gate Charge		Qg	_	14	20	nC
Gate-Emitter Charge	$(V_{CC} = 108 \text{ V, I}_{C} = 20 \text{ A,} $ $V_{GF} = 5 \text{ V})$	Qgs	_	3.0	_	1
Gate-Collector Charge	*GE - 3 */	Q _{qd}	<u> </u>	6.0	_	1

Gate–Collector Charge

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

PACKAGE DIMENSIONS



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.405	9.66	10.28	
С	0.160	0.190	4.07	4.82	
D	0.025	0.035	0.64	0.88	
F	0.142	0.147	3.61	3.73	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.155	2.80	3.93	
J	0.018	0.025	0.46	0.64	
K	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.39	
T	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
٧	0.045		1.15		
Z		0.080		2.04	

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