

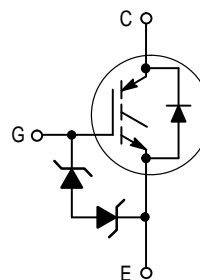
Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N-Channel Enhancement-Mode Silicon Gate

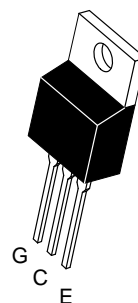
This Insulated Gate Bipolar Transistor (IGBT) is co-packaged with a soft recovery ultra-fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. Its new 600 V IGBT technology is specifically suited for applications requiring both a high temperature short circuit capability and a low $V_{CE(on)}$. It also provides fast switching characteristics and results in efficient operation at high frequencies. Co-packaged IGBTs save space, reduce assembly time and cost. This new E-series introduces an energy efficient, ESD protected, and rugged short circuit device.

- Industry Standard TO-220 Package
- High Speed: $E_{off} = 60 \mu J$ per Amp typical at 125°C
- High Voltage Short Circuit Capability – 10 μs minimum at 125°C, 400 V
- Low On-Voltage — 2.0 V typical at 8.0 A
- Soft Recovery Free Wheeling Diode is included in the Package
- Robust High Voltage Termination
- ESD Protection Gate-Emitter Zener Diodes



MGP11N60ED

IGBT & DIODE IN TO-220
11 A @ 90°C
15 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED
LOW ON-VOLTAGE



CASE 221A-09
STYLE 9
TO-220AB

MAXIMUM RATINGS ($T_J = 25^\circ C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	600	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 M\Omega$)	V_{CGR}	600	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ C$ — Continuous @ $T_C = 90^\circ C$ — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	15 11 22	Adc Apk
Total Power Dissipation @ $T_C = 25^\circ C$ Derate above 25°C	P_D	96 0.77	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Short Circuit Withstand Time ($V_{CC} = 400 Vdc, V_{GE} = 15 Vdc, T_J = 125^\circ C, R_G = 20 \Omega$)	t_{sc}	10	μs
Thermal Resistance — Junction to Case — IGBT — Junction to Case — Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JD}$ $R_{\theta JA}$	1.3 2.3 65	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C
Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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MGP11N60ED**ELECTRICAL CHARACTERISTICS** ($T_J = 25^\circ\text{C}$ unless otherwise noted)

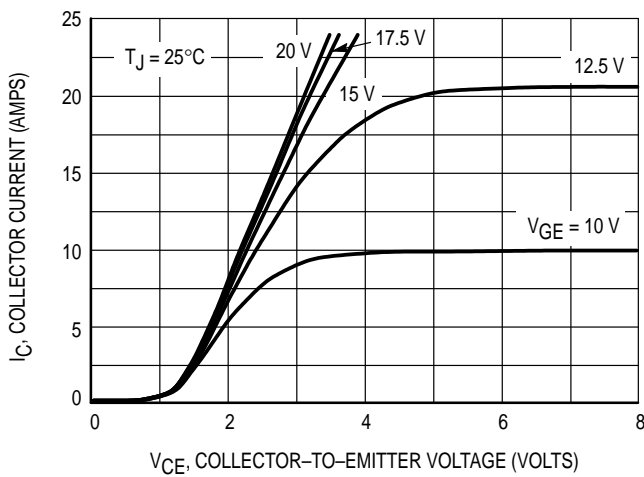
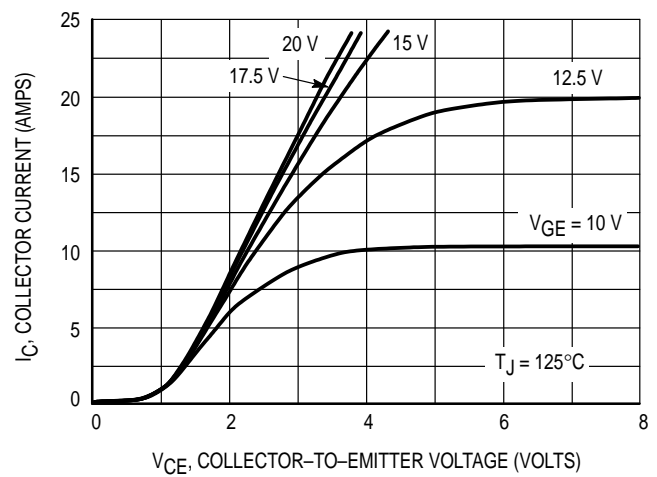
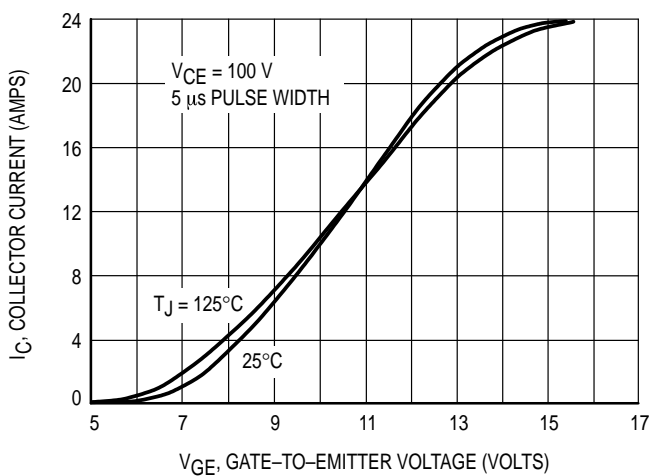
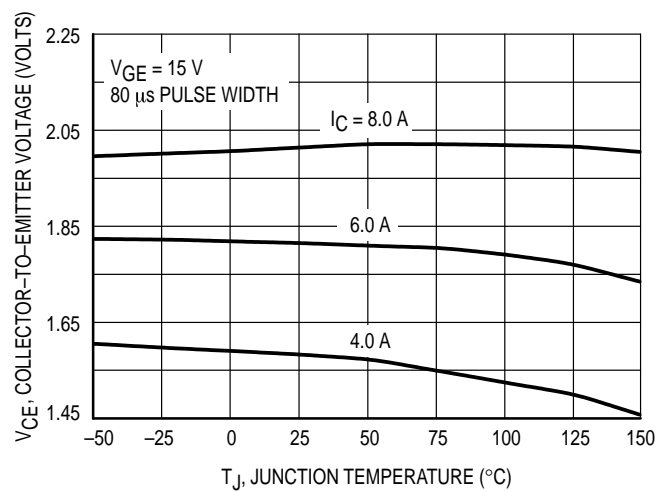
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage (V _{GE} = 0 Vdc, I _C = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)CES}	600 —	— 870	— —	Vdc mV/°C
Zero Gate Voltage Collector Current (V _{CE} = 600 Vdc, V _{GE} = 0 Vdc) (V _{CE} = 600 Vdc, V _{GE} = 0 Vdc, T _J = 125°C)	I _{CES}	— —	— —	10 200	μAdc
Gate-Body Leakage Current (V _{GE} = ± 20 Vdc, V _{CE} = 0 Vdc)	I _{GES}	—	—	50	μAdc
ON CHARACTERISTICS (1)					
Collector-to-Emitter On-State Voltage (V _{GE} = 15 Vdc, I _C = 4.0 Adc) (V _{GE} = 15 Vdc, I _C = 4.0 Adc, T _J = 125°C) (V _{GE} = 15 Vdc, I _C = 8.0 Adc)	V _{CE(on)}	— — —	1.6 1.5 2.0	1.9 — 2.4	Vdc
Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V _{CE} = 10 Vdc, I _C = 8.0 Adc)	g _{fe}	—	3.5	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	779	pF
Output Capacitance		C _{oes}	—	81	
Transfer Capacitance		C _{res}	—	13	
SWITCHING CHARACTERISTICS (1)					
Turn-On Delay Time	(V _{CC} = 360 Vdc, I _C = 8.0 Adc, V _{GE} = 15 Vdc, L = 300 μH, R _G = 20 Ω) Energy losses include “tail”	t _{d(on)}	—	46	ns
Rise Time		t _r	—	34	
Turn-Off Delay Time		t _{d(off)}	—	102	
Fall Time		t _f	—	226	
Turn-Off Switching Loss		E _{off}	—	0.32	mJ
Turn-On Switching Loss		E _{on}	—	0.11	
Total Switching Loss		E _{ts}	—	0.43	
Turn-On Delay Time	(V _{CC} = 360 Vdc, I _C = 8.0 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω, T _J = 125°C) Energy losses include “tail”	t _{d(on)}	—	42	ns
Rise Time		t _r	—	26	
Turn-Off Delay Time		t _{d(off)}	—	214	
Fall Time		t _f	—	228	
Turn-Off Switching Loss		E _{off}	—	0.48	mJ
Turn-On Switching Loss		E _{on}	—	0.16	
Total Switching Loss		E _{ts}	—	0.64	
Gate Charge	(V _{CC} = 360 Vdc, I _C = 8.0 Adc, V _{GE} = 15 Vdc)	Q _T	—	39.2	nC
		Q ₁	—	8.7	
		Q ₂	—	17.4	
DIODE CHARACTERISTICS					
Diode Forward Voltage Drop (I _{EC} = 3.25 Adc) (I _{EC} = 3.25 Adc, T _J = 125°C) (I _{EC} = 6.5 Adc)	V _{FEC}	— — 1.7	1.63 1.24 2.0	— — 2.3	Vdc

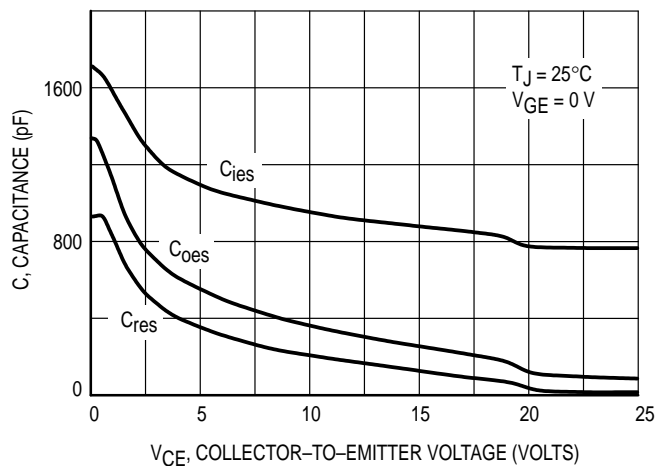
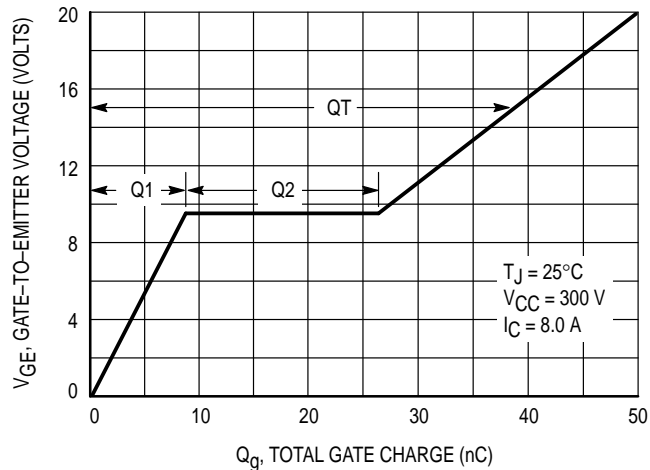
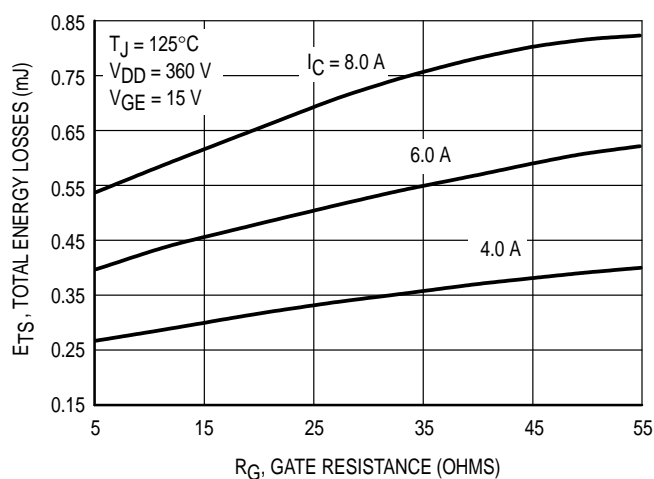
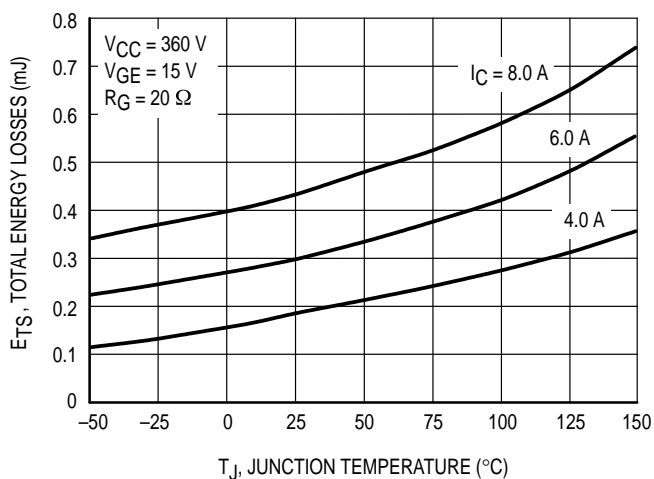
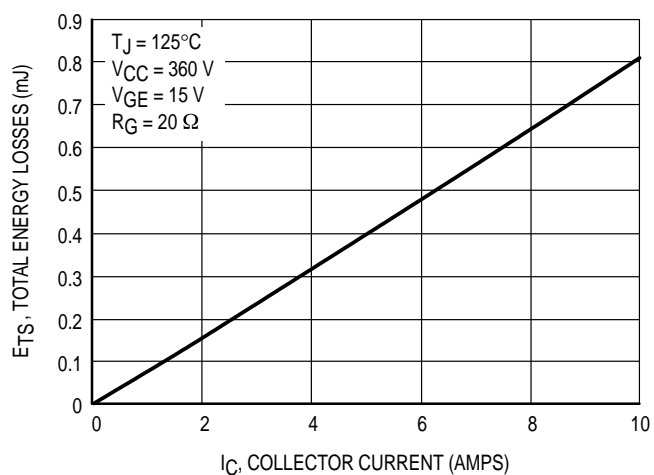
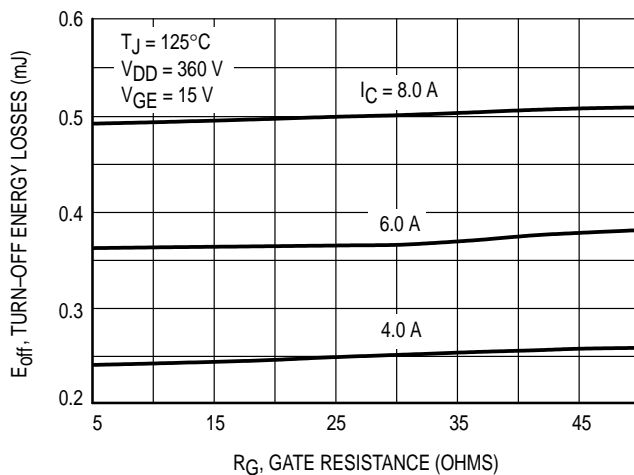
(1) Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

(continued)

ELECTRICAL CHARACTERISTICS — continued ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued					
Reverse Recovery Time	$(I_F = 8.0 \text{ Adc}, V_R = 360 \text{ Vdc}, dI_F/dt = 200 \text{ A}/\mu\text{s})$	t_{rr}	—	57	ns
		t_a	—	18	
		t_b	—	39	
Reverse Recovery Stored Charge		Q_{RR}	—	107	μC
Reverse Recovery Time	$(I_F = 8.0 \text{ Adc}, V_R = 360 \text{ Vdc}, dI_F/dt = 200 \text{ A}/\mu\text{s}, T_J = 125^\circ\text{C})$	t_{rr}	—	91	ns
		t_a	—	28	
		t_b	—	63	
Reverse Recovery Stored Charge		Q_{RR}	—	275	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L_E	—	7.5	—	nH

**Figure 1. Output Characteristics****Figure 2. Output Characteristics****Figure 3. Transfer Characteristics****Figure 4. Collector-To-Emitter Saturation Voltage versus Junction Temperature**


Figure 5. Capacitance Variation

Figure 6. Gate-To-Emitter Voltage versus Total Charge

Figure 7. Total Energy Losses versus Gate Resistance

Figure 8. Total Energy Losses versus Junction Temperature

Figure 9. Total Energy Losses versus Collector Current

Figure 10. Turn-Off Losses versus Gate Resistance

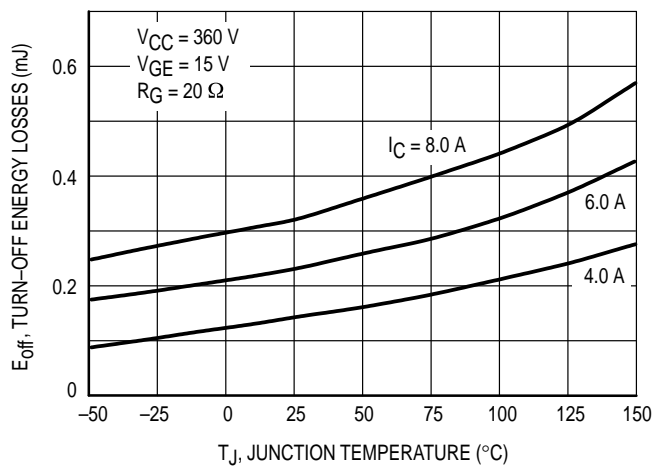


Figure 11. Turn-Off Losses versus Junction Temperature

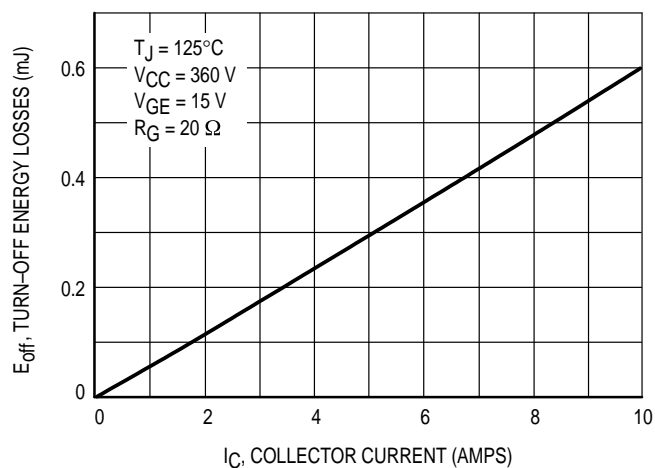


Figure 12. Turn-Off Losses versus Collector Current

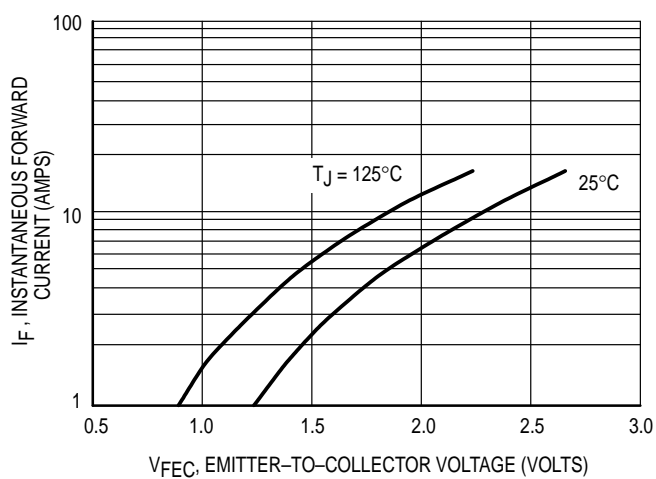


Figure 13. Forward Characteristics versus Current

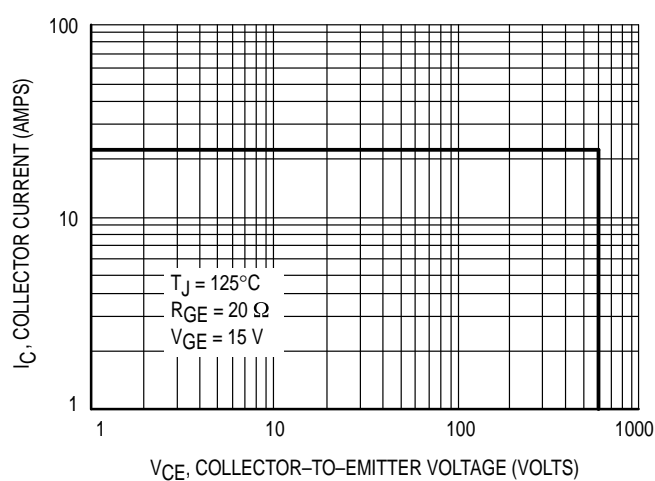
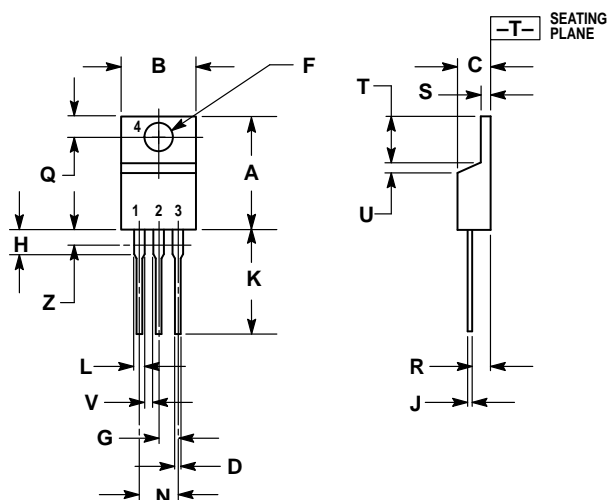


Figure 14. Reverse Biased Safe Operating Area

PACKAGE DIMENSIONS



NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

**CASE 221A-09
TO-220AB
ISSUE Z**

STYLE 9:

- PIN 1: GATE
2: COLLECTOR
3: EMITTER
4: COLLECTOR

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