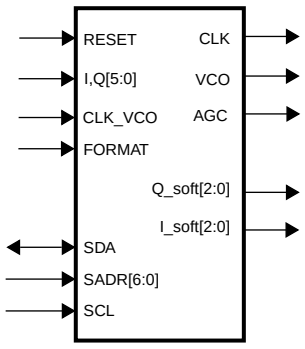
MC92303

Product Brief

QPSK/BPSK DIGITAL DEMODULATOR



The MC92303 is a coherent digital demodulator for QPSK and BPSK modulated signals utilized in Digital-TV applications according to the EBU defined DVB transmission standard for satellite Set-Top systems or similar. The MC92303 contains all the functionality required to lock onto signals with frequency offsets as large as the baud rate and extract the desired signal from a frequency band with adjacent channel interference and other undesirable signals.

Feature Summary

- DVB compliant QPSK/BPSK Coherent Demodulator
- Variable Modulation Rate up to 30 MBaud to work with all present European DVB Channels
- Selectable Input Format (Offset Binary/2's Complement)
- DC Offset Removal, I/Q-swapping and Input Format Selection in one block
- Decimation Filters for Oversampling Ratios of 2/T, 3/T, 4/T, 6/T, 8/T, 12/T and 16/T
- Half Nyquist Baseband Filters (α=0.35)
- Internal Numerically Controlled Oscillator (NCO)
- Automatic Gain Control (AGC) provided to analog front-end
- Automatic Frequency Control (AFC) to ±Rs (Symbol Rate)
- Clock Synchronization with 1-Bit ΣΔ-Converter Output for ADC control
- Programmable Second Order Loop Filters for Carrier Recovery and AGC
- 3-bit Soft Decision output per Symbol with selectable format (Offset Binary/2's Complement/Sign Magnitude)
- Programmable Sampling Rates of the Digital Sigma-Delta Converters
- < 0.5 dB Implementation Loss from theory
- I^2C Programmable Interface
- 0.5µ CMOS Process at 3.3V

Ordering Information

Device	Package
MC92303BT	160QFP

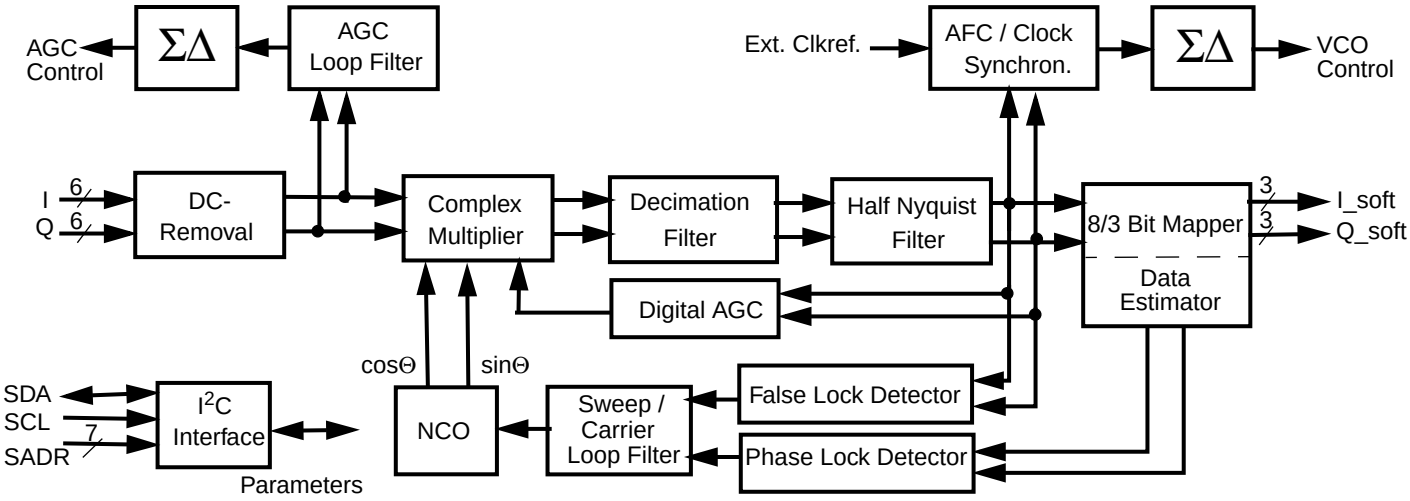


Figure 1. QPSK/BPSK Demodulator Block Diagram

This document contains information on a new product.
Specifications and information herein are subject to change without notice.

Control Loops

The inputs to the device are 6 bit I and Q digital signals. A pin programmable input format selector allows use of A/D converters with either offset binary or 2's complement output format. The A/D output data is fed into the carrier synchronization loop which is capable of locking onto signals with frequency offsets as large as the baud rate. The carrier synchronizer includes a complex multiplier, a phase detector, a programmable second order loop filter, a phase lock detector, a false lock detector and a frequency sweep function. The carrier tracking loop is closed digitally using an internal numerically controlled oscillator (NCO). The frequency sweep rate, the frequency sweep limit, the phase and frequency lock detector thresholds and the loop parameters are programmable. The I and Q QPSK symbols produced in this loop are further processed by a Decimation Filter and a Half Nyquist Filter (roll-off factor of 0.35) to perform the matched filtering. Once processed, the filtered data samples are passed to the data estimator which produces 3 bits of I and Q soft decision data (device output) as well as I and Q error vectors.

The demodulator also performs a non-coherent automatic gain control (AGC) function on the IF signal using a total power algorithm and generates a single bit output signal which must be lowpass filtered and interfaced to the gain control port of a variable gain amplifier. The AGC includes a programmable second order loop filter.

Another control loop, the mid-symbol sampling synchronization loop, ensures that the optimum A/D sampling times are determined by providing a single bit output signal to a voltage controlled oscillator (VCO) clock generator. This VCO quiescent frequency is automatically set to 2, 3, 4, 6, 8,12 or 16 Rs depending on the oversampling factor. Its output signal levels must be suitable for clocking both the A/D converter and the QPSK demodulator.

Decimation Filter

The Decimation Filter block consists of three switchable decimation filters: two 1/2-band filters and a 2/3-band filter. Together with a switchable input decimation of 2, the decimation filter block enables the demodulator to operate at an oversampling ratio of 2, 3, 4, 6, 8, 12, or 16. The variable sampling demodulator minimizes the external components to build a Set Top box for the whole range of data rates. In order to compensate different signal gains after the decimation an internal Digital AGC produces a control signal which adjusts the gain after the complex multiplier.

I^2C interface

The MC92303 is a slaved device that is intended to be controlled via the I^2C interface. In accordance with the I^2C specification, the I^2C master initiates all data transfers to and from the demodulator and provides the I^2C clock. Data is always transferred one byte at a time, MSB first, and the receiver must acknowledge each byte by pulling the data line low during the cycle following the LSB. The demodulator interprets the byte following its slave address as an 8-bit sub-address which selects a particular register to be written to or read from.

Application

The demodulator can be used to implement a DVB compliant demodulator with the circuitry shown in Figure 2. The 3 bit soft decision data of the demodulator is connected directly toa Viterbi Decoder or a combined Viterbi and Reed Solomon Decoder.

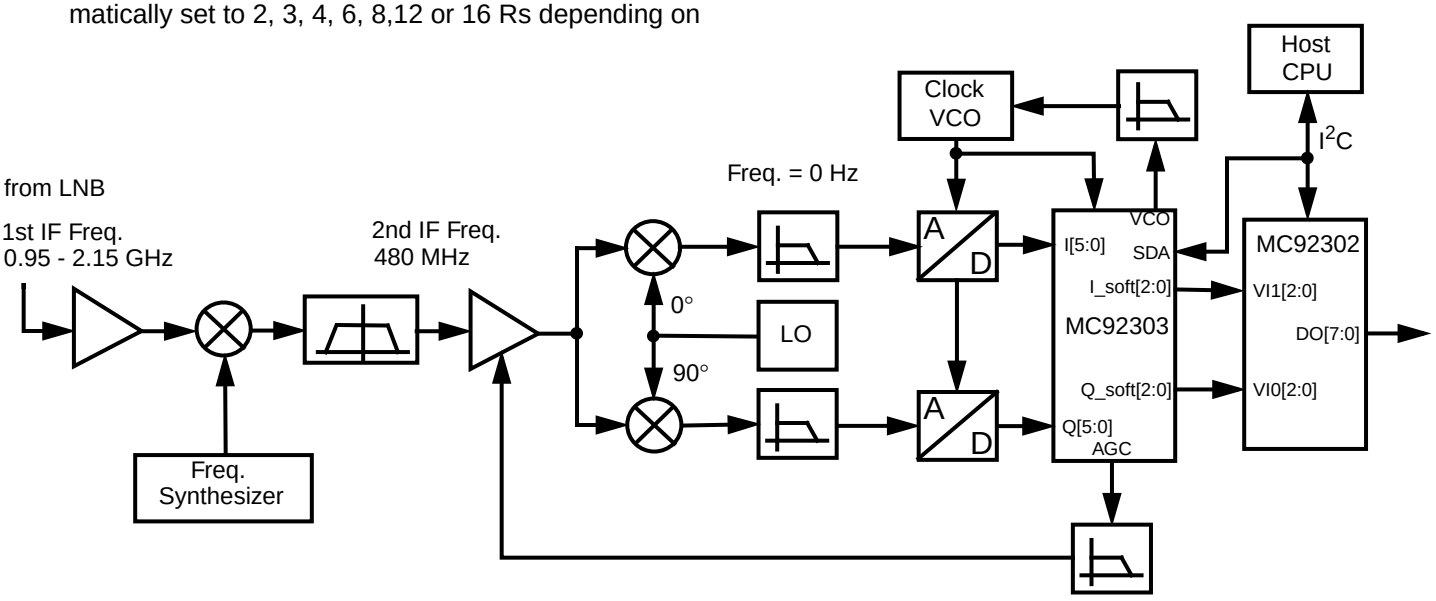


Figure 2. DVB Application Example

Table 1. MC92303 Pin Description

SIGNAL	FUNCTIONALITY
RESET	Asynchronous Reset
SDA	Data Bus of I^2C-interface
SADR[6:0]	Slave Address of I^2C-interface
SCL	Clock Line of I^2C-interface
I,Q[5:0]	Inphase and Quadrature Symbol Inputs
CLK_VCO	Input Clock from VCO
FORMAT	Input Format Selection
I_soft[2:0], Q_soft[2:0]	Soft Decision Output Signals
BPSK	Demodulated BPSK Signal
AGC	AGC Control Signal
VCO	Control Signal for External VCO
CLK	Control Signal for Clock VCO

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