

Differential Clock D Flip-Flop

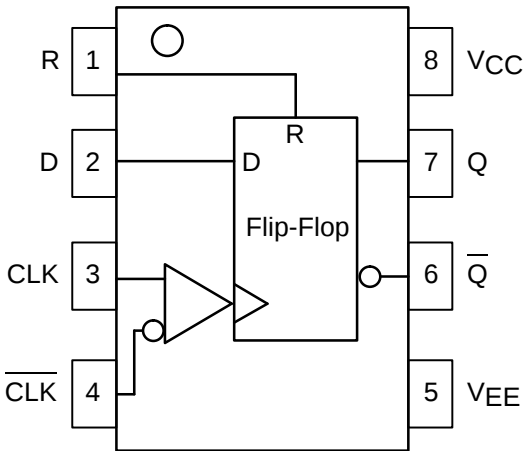
The MC10EL/100EL51 is a differential clock D flip-flop with reset. The device is functionally similar to the E151 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E151 the EL51 is ideally suited for those applications which require the ultimate in AC performance.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input (pulled down to V_{EE}) conditions.

- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC10EL51 MC100EL51



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition



MC10EL51 MC100EL51

DC CHARACTERISTICS ($V_{EE} = V_{EE}(\min)$ to $V_{EE}(\max)$; $V_{CC} = GND$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		24 24	29 29		24 24	29 29		24 24	29 29		24 30	29 36	mA
V_{EE}	Power Supply Voltage	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	V
I_{IH}	Input HIGH Current			150			150			150			150	μA

AC CHARACTERISTICS ($V_{EE} = V_{EE}(\min)$ to $V_{EE}(\max)$; $V_{CC} = GND$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	1.8	2.8		2.2	2.8		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	325 305	465 455	605 605	375 355	465 455	555 555	385 355	475 465	565 565	440 410	530 510	620 620	ps
t_S	Setup Time	150	0		150	0		150	0		150	0		ps
t_H	Hold Time	250	100		250	100		250	100		250	100		ps
t_{RR}	Reset Recovery	400	200		400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Reset	400			400			400			400			ps
V_{PP}	Minimum Input Swing ¹	150			150			150			150			mV
V_{CMR}	Common Mode Range ²	-0.4		See ²	-0.4		See ²	-0.4		See ²	-0.4		See ²	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

1. Minimum input swing for which AC parameters are guaranteed.

2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to $V_{EE} + 2.5V$.

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