Differential Clock D Flip-Flop

MC10EL51
MC100EL51

The MC10EL/100EL51 is a differential clock D flip-flop with reset. The device is functionally similar to the E151 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E151 the EL51 is ideally suited for those applications which require the ultimate in AC performance.

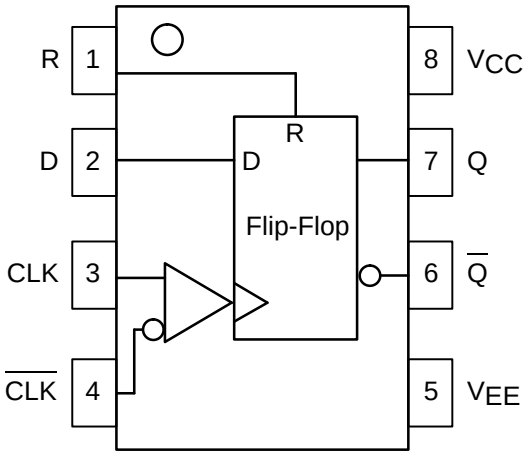
The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input (pulled down to V_{EE}) conditions.

- 475ps Propagation Delay
- 2.8GHz Toggle Frequency
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current 10EL		24	29		24	29		24	29		24	29	mA
	100EL		24	29		24	29		24	29		30	36	
V_{EE}	Power Supply Voltage 10EL	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
	100EL	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current			150			150			150			150	µA

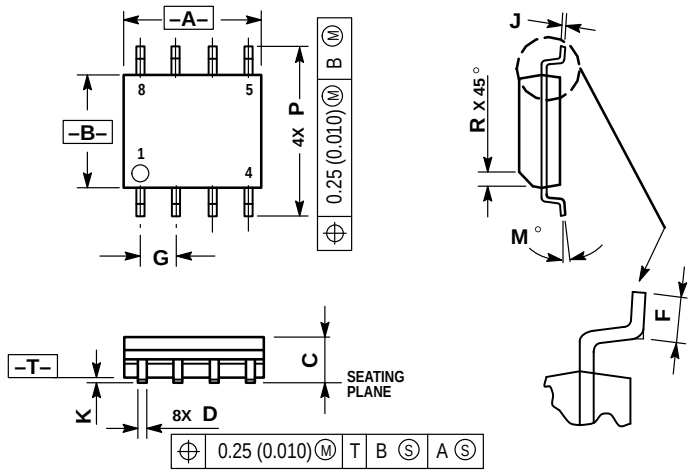
AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	1.8	2.8		2.2	2.8		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK	325	465	605	375	465	555	385	475	565	440	530	620	ps
	R	305	455	605	355	455	555	355	465	565	410	510	620	
t_S	Setup Time	150	0		150	0		150	0		150	0		ps
t_H	Hold Time	250	100		250	100		250	100		250	100		ps
t_{RR}	Reset Recovery	400	200		400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Reset	400			400			400			400			ps
V_{PP}	Minimum Input Swing[1]	150			150			150			150			mV
V_{CMR}	Common Mode Range[2]	–0.4		See[2]	–0.4		See[2]	–0.4		See[2]	–0.4		See[2]	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	100	225	350	ps

1. Minimum input swing for which AC parameters are guaranteed.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range is dependent on V_{EE} and is equal to V_{EE} + 2.5V.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05
ISSUE P



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0 °	7 °
P	5.80	6.20
R	0.25	0.50

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298