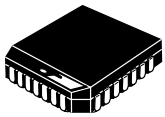
4-Bit Serial/Parallel Converter

MC10E445
MC100E445

4-BIT SERIAL/
PARALLEL CONVERTER

The MC10/100E445 is an integrated 4-bit serial to parallel data converter. The device is designed to operate for NRZ data rates of up to 2.0Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q0, the second to Q1 etc.

- On-Chip Clock ÷4 and ÷8
- 2.0Gb/s Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-Ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8-Bits
- Internal 75kΩ Input Pulldown Resistors
- Extended 100E V_{EE} Range of –4.2V to –5.46V



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Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel to serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse applied asynchronously for at least two input clock cycles shifts the start bit for conversion from Qn to Qn–1. For each additional shift required an additional pulse must be applied to the SYNC input. Asserting the SYNC input will force the internal clock dividers to "swallow" a clock pulse, effectively shifting a bit from the Qn to the Qn–1 output (see Timing Diagram B).

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the data on the output will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E445's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 2.0Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E445.

For lower data rate applications a V_{BB} reference voltage is supplied for single-ended inputs. When operating at clock rates above 500MHz differential input signals are recommended. For single-ended inputs the V_{BB} pin is tied to the inverting differential input and bypassed via a 0.01µF capacitor. The V_{BB} provides the switching reference for the input differential amplifier. The V_{BB} can also be used to AC couple an input signal, for more information on AC coupling refer to the interfacing section of the design guide in the ECLinPS™ data book.

Upon power-up the internal flip-flops will attain a random state. To synchronize multiple E445's in a system the master reset must be asserted.

PIN NAMES

Pin	Function
SINA, $\overline{\text{SINA}}$	Differential Serial Data Input A
SINB, $\overline{\text{SINB}}$	Differential Serial Data Input B
SEL	Serial Input Selector Pin
Q0–Q3	Parallel Data Outputs
CLK, $\overline{\text{CLK}}$	Differential Clock Inputs
CL/4, $\overline{\text{CL/4}}$	Differential ÷4 Clock Output
CL/8, $\overline{\text{CL/8}}$	Differential ÷8 Clock Output
MODE	Conversion Mode 4-Bit/8-Bit
SYNCH	Conversion Synchronizing Input

FUNCTION TABLES

Mode	Conversion	SEL	Serial Input
L	4-Bit	H	A
H	8-Bit	L	B

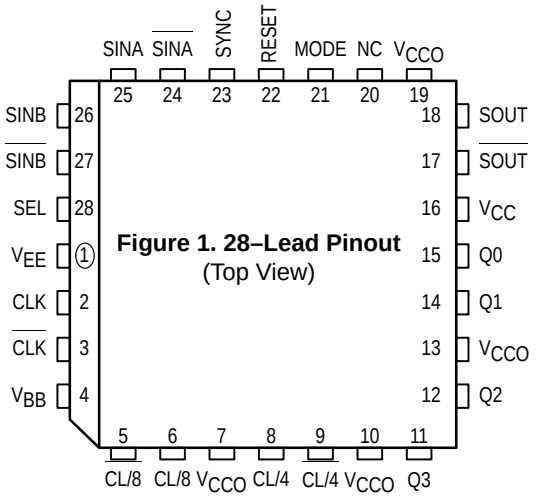


Figure 1. 28–Lead Pinout
(Top View)

MOTOROLA

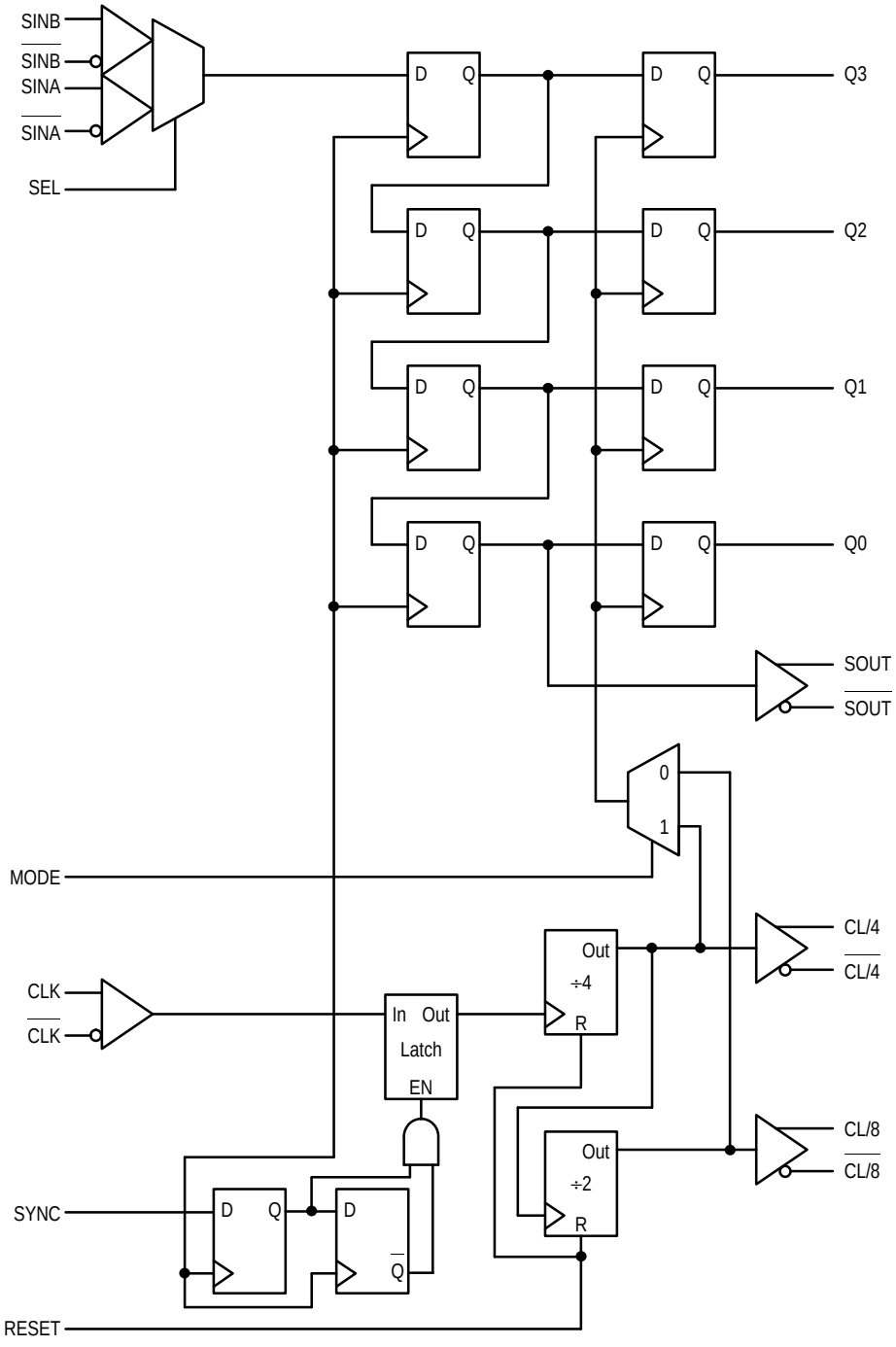


Figure 2. Logic Diagram

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

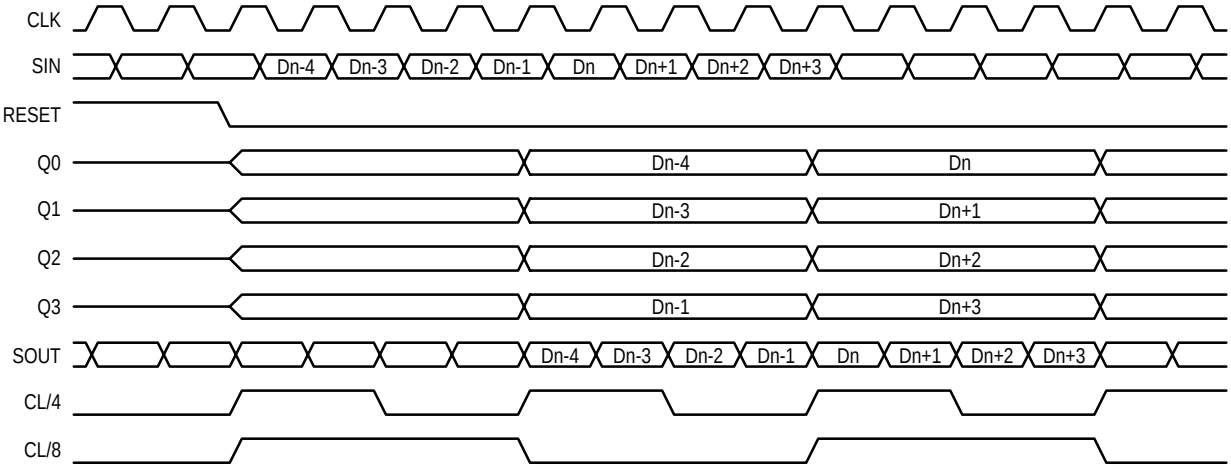
Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
I_{IH}	Input HIGH Current			150			150			150	µA	
V_{OH}	Ouput HIGH Current 10E (SOUT Only) 100E (SOUT Only)	 –1020 –1025		 –790 –830	 –980 –1025		 –760 –830	 –910 –1025		 –670 –830	V	 1 1
V_{BB}	Output Reference Voltage 10E 100E	 –1.38 –1.38		 –1.27 –1.26	 –1.35 –1.38		 –1.25 –1.26	 –1.31 –1.38		 –1.19 –1.26	V	
I_{EE}	Power Supply Current 10E 100E		 154 154	 185 185		 154 154	 185 185		 154 177	 185 212	mA	

1. The maximum V_{OH} limit was relaxed from standard ECL due to the high frequency output design. All other outputs are specified with the standard 10E and 100E V_{OH} levels.

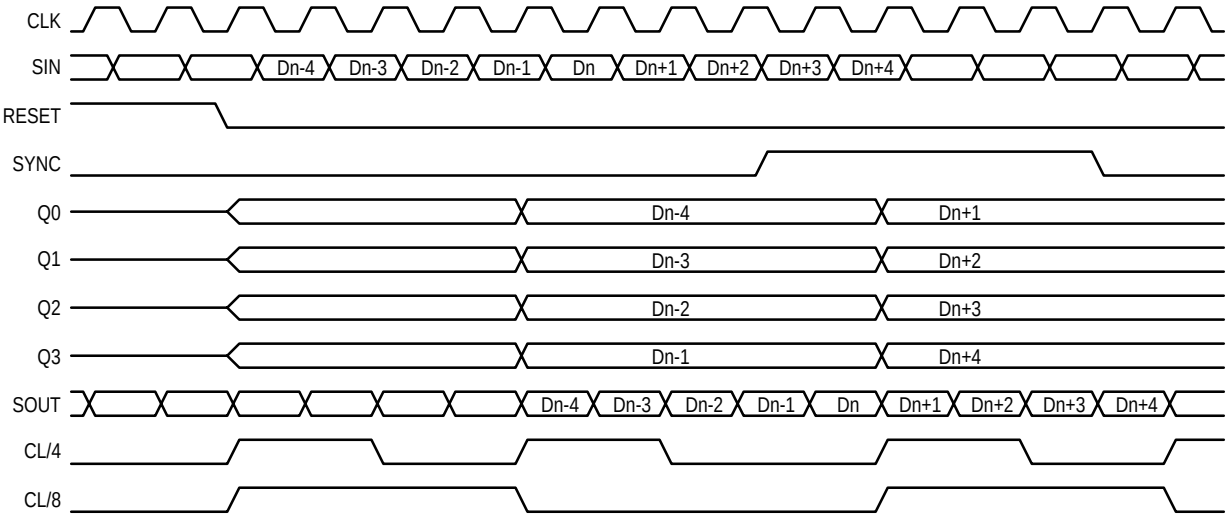
AC CHARACTERISTICS (V_{EE} = V_{EE}(min) to V_{EE}(max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Conversion Frequency	2.0			2.0			2.0			Gb/s NRZ	
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q CLK to SOUT CLK to CL/4 CLK to CL/8	 1500 800 1100 1100	 1800 975 1325 1325	 2100 1150 1550 1550	 1500 800 1100 1100	 1800 975 1325 1325	 2100 1150 1550 1550	 1500 800 1100 1100	 1800 975 1325 1325	 2100 1150 1550 1550	ps	
t_S	Setup Time SINA, SINB SEL	 –100 0	 –250 –200		 –100 0	 –250 –200		 –100 0	 –250 –200		ps	
t_h	Hold Time SINA, SINB, SEL	 450	 300		 450	 300		 450	 300		ps	
t_{RR}	Reset Recovery Time	500	300		500	300		500	300		ps	
t_{PW}	Minimum Pulse Width CLK, MR	 400			 400			 400			ps	
t_r t_f	Rise/Fall Times SOUT Other	 100 200	 225 425	 350 650	 100 200	 225 425	 350 650	 100 200	 225 425	 350 650	ps	20%–80%

Figure 3. Timing Diagrams



Timing Diagram A. 1:4 Serial to Parallel Conversion



Timing Diagram B. 1:4 Serial to Parallel Conversion With SYNC Pulse

APPLICATIONS INFORMATION

The MC10E/100E445 is an integrated 1:4 serial to parallel converter. The chip is designed to work with the E446 device to provide both transmission and receiving of a high speed serial data path. The E445, can convert up to a 2.0Gb/s NRZ data stream into 4-bit parallel data. The device also provides a divide by four clock output to be used to synchronize the parallel data with the rest of the system.

The E445 features multiplexed dual serial inputs to provide test loop capability when used in conjunction with the E446. Figure 4 illustrates the loop test architecture. The architecture allows for the electrical testing of the link without requiring actual transmission over the serial data path medium. The SINA serial input of the E445 has an extra buffer delay and thus should be used as the loop back serial input.

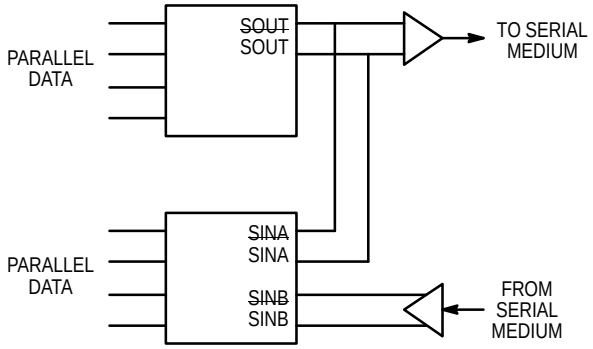
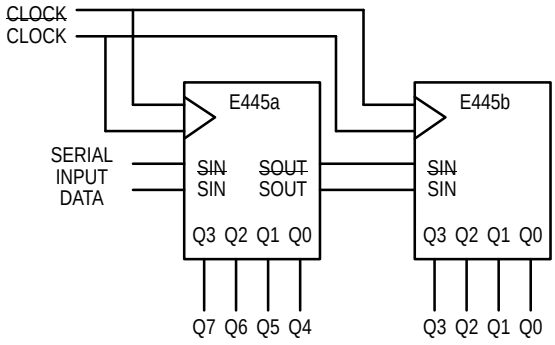


Figure 4. Loopback Test Architecture

The E445 features a differential serial output and a divide by 8 clock output to facilitate the cascading of two devices to build a 1:8 demultiplexer. Figure 5 illustrates the architecture for a 1:8 demultiplexer using two E445's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1150ps and tS for SIN = –100ps, yields a minimum period of 1050ps or a clock frequency of 950MHz.

The clock frequency is significantly lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E445. By delaying the clock feeding the second E445 relative to the clock of the first E445 the frequency of operation can be increased. The delay between the two clocks can be increased until the minimum delay of clock to serial out would potentially cause a serial bit to be swallowed (Figure 6).



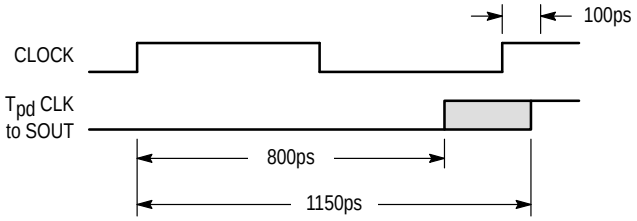


Figure 5. Cascaded 1:8 Converter Architecture

With a minimum delay of 800ps on this output the clock for the lower order E445 cannot be delayed more than 800ps relative to the clock of the first E445 without potentially missing a bit of information. Because the setup time on the serial input pin is negative coincident excursions on the data and clock inputs of the E445 will result in correct operation.

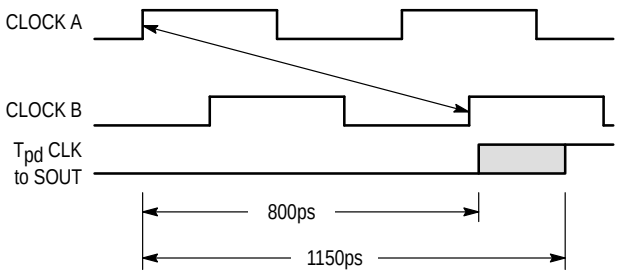


Figure 6. Cascade Frequency Limitation

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E445. By connecting the clock for the second E445 to the complimentary clock input pin the device will clock a half a clock period after the first E445 (Figure 7). Utilizing this simple technique will raise the potential conversion frequency up to 1.4GHz. The divide by eight clock of the second E445 should be used to synchronize the parallel data to the rest of the system as the parallel data of the two E445's will no longer be synchronized. This skew problem between the outputs can be worked around as the parallel information will be static for eight more clock pulses.

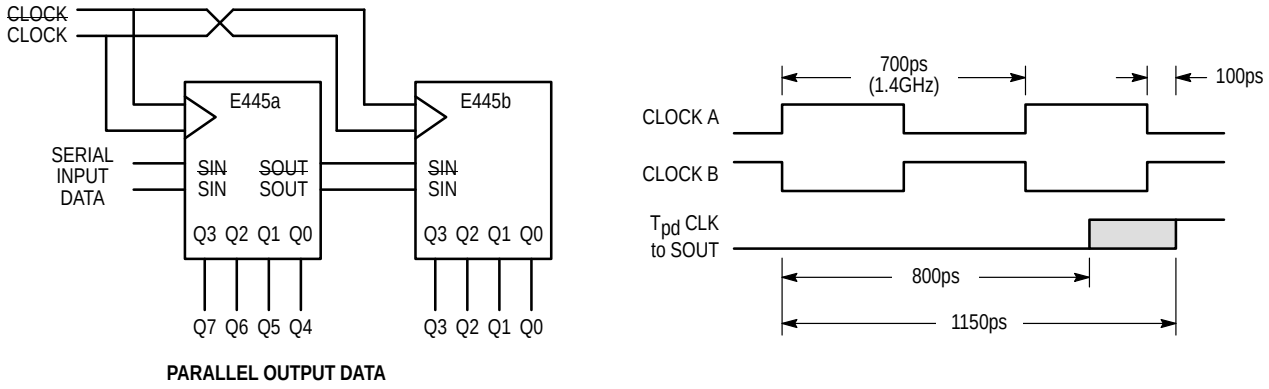


Figure 7. Extended Frequency 1:8 Demultiplexer

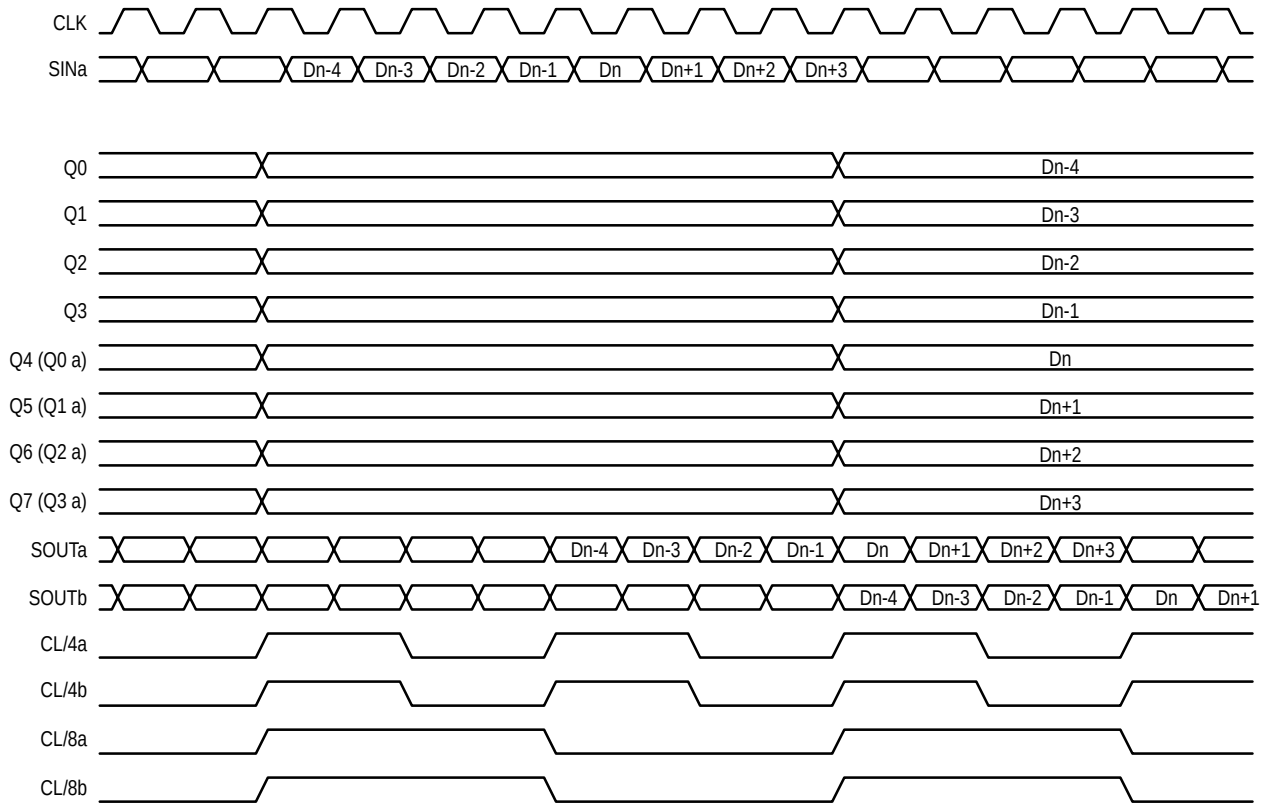


Figure 8. Timing Diagram A. 1:8 Serial to Parallel Conversion

OUTLINE DIMENSIONS

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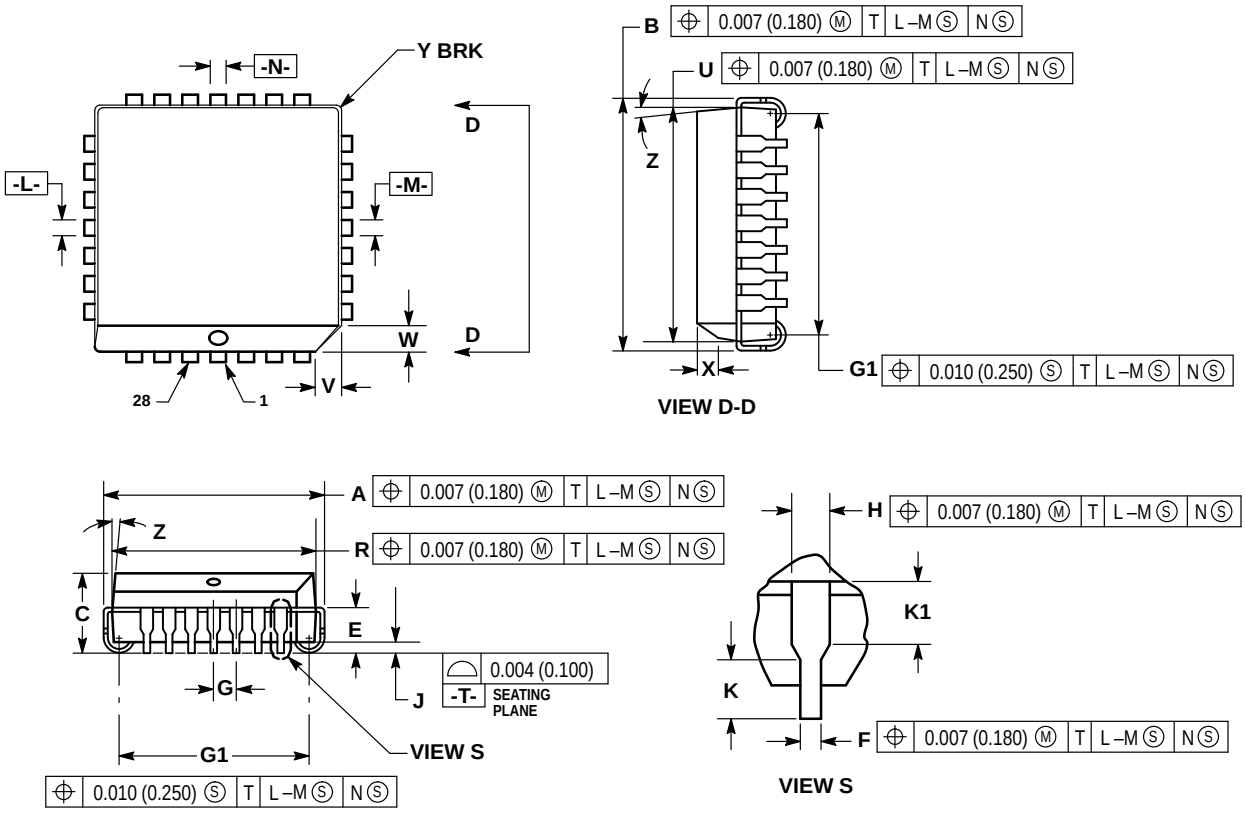

NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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