AN485
Application Note

HIGH POWER AUDIO AMPLIFIERS WITH SHORT CIRCUIT PROTECTION

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This application note describes a recommended circuit approach for high-performance audio amplifiers in the 35-W to 100-W rms power range. Circuitry is included which enables the amplifier to operate safely under any load condition including a continuous short.

MOTOROLA *Semiconductor Products Inc.*

HIGH POWER AUDIO AMPLIFIERS WITH SHORT CIRCUIT PROTECTION

INTRODUCTION

The development of Motorola's 200-W PNP silicon power transistors now allows the economical design of full complementary direct-coupled audio amplifiers capable of delivering 100 watts of rms power into an 8-ohm load at less than 0.2% distortion.

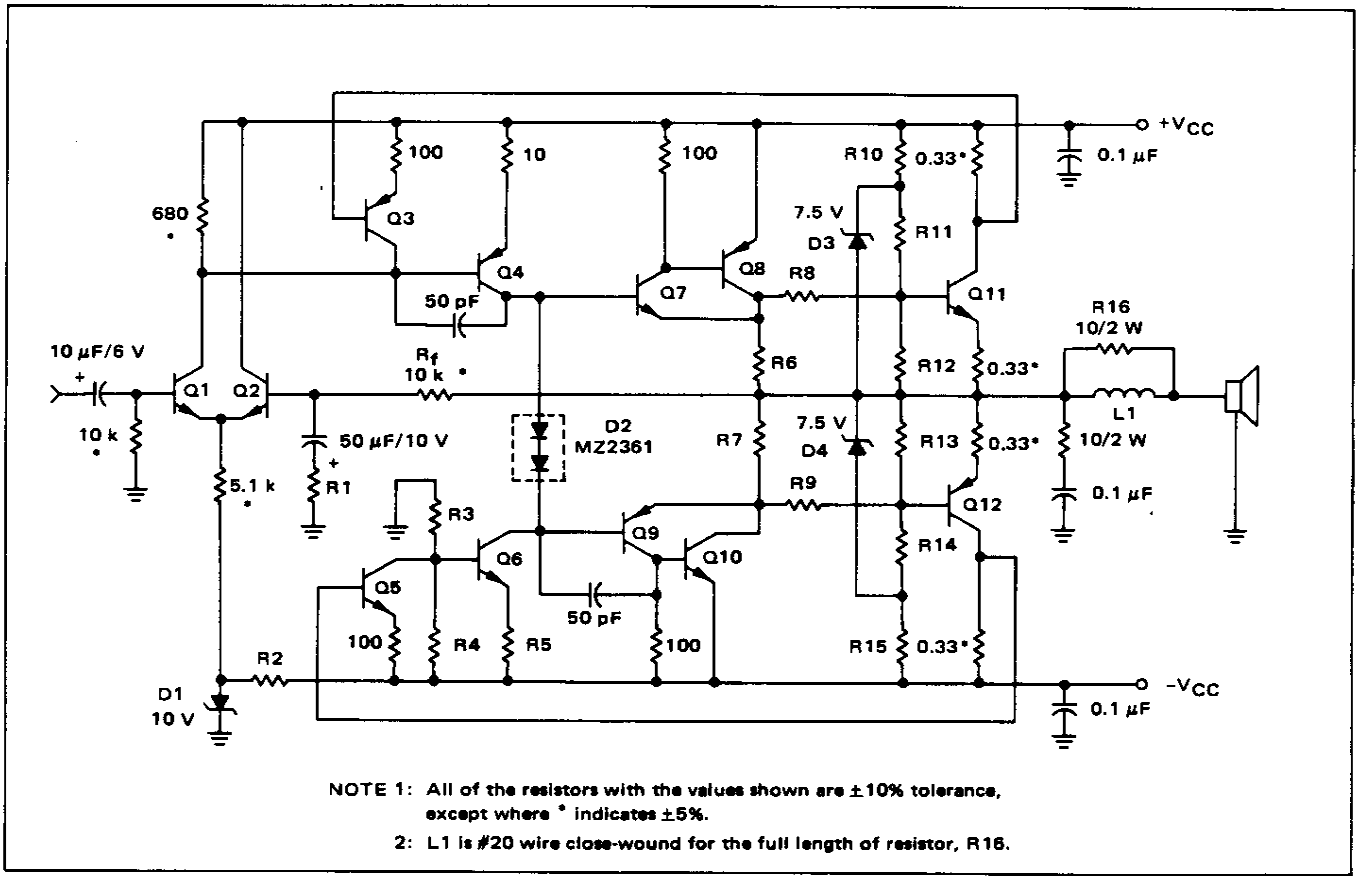
The circuit approach suggested in this paper allows the designer to make optimum use of economy transistors in amplifiers that will operate safely under any usable load condition, including a short.

Tables are included which provide the designer with the necessary information to design 35-, 50-, 60-, 75-, and 100-watt amplifiers at either 4 or 8 ohm load impedance. Detailed design information is included in the appendix for those who wish to design amplifiers for power outputs other than those shown.

CIRCUIT DESCRIPTION

The schematic diagram shown in Figure 1 is the recommended approach for the full-complementary amplifier with short-circuit protection.

Transistors Q1, Q2, Q4, Q6, Q7, Q8, Q9, and Q10, along with their associated components, comprise the standard full-complementary circuit. Transistors Q1 and Q2 are used in a differential amplifier configuration which, when used with a split power supply, provide a convenient means for setting the dc voltage level at the output at zero, enabling the amplifier to be direct coupled to the speaker. Resistor R_f provides 100% dc feedback from the output to the input, for excellent dc stability. The resistance ratio of R_f to R1 determines the closed-loop ac-voltage gain of the amplifier. Transistor Q4 functions as a high-gain, common-emitter driver. Since the output configura-



NOTE 1: All of the resistors with the values shown are ±10% tolerance, except where * indicates ±5%.

2: L1 is #20 wire close-wound for the full length of resistor, R16.

FIGURE 1 – Schematic Diagram of 35- to 100-W Amplifiers. Parts Values are Shown in Tables 1, 2 and 3.

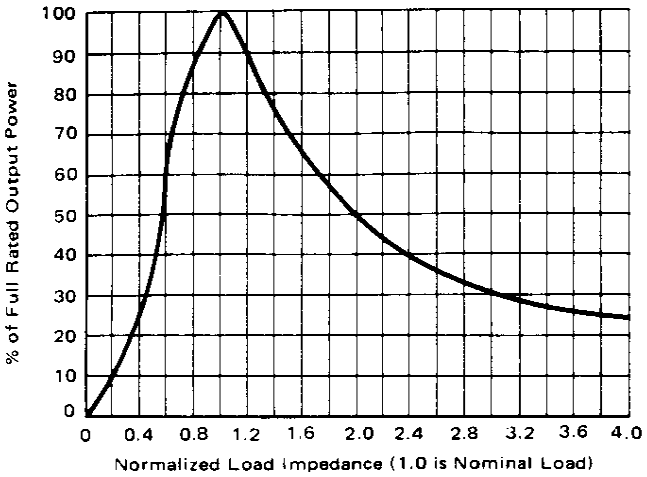


FIGURE 2 – Output Power versus Load Impedance

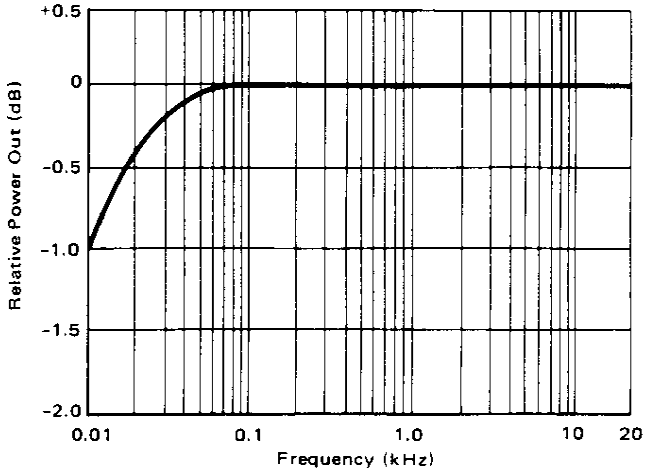


FIGURE 3 – Power Bandwidth (0 dB is Max Rated Power Output)

tion serves only as an emitter follower, this transistor must be capable of handling the full-load voltage swing. Transistor Q6 serves as a constant-current source for the dc bias current, which flows through Q4 and the dual bias diode, D2. This transistor, Q6, also eliminates the need for the large bootstrap electrolytic capacitor commonly used to provide ac current drive to the lower half of the output circuit during negative peak signal excursions. Transistors Q7 and Q8 form a compound pair which function as an emitter follower with high current gain and unity voltage gain for the positive portion of the output signal. Q9 and Q10 similarly function for the negative portion of the output signal. The zener diode, D1, is used to set the dc current through the differential amplifier and provide ac hum rejection from the negative power supply.

SHORT-CIRCUIT PROTECTION

Semiconductors Q3, Q5, Q11, Q12, D3, and D4, along with their associated resistors, comprise the short-circuit protection network.

The resistors R8, R10, R11, and R12, form a voltage-summing network. The voltage appearing at the base of transistor Q11 is thus determined by the collector current of Q8 flowing through resistor R6 and the voltage appearing from $+V_{CC}$ to the output. This summing network, since it detects both the voltage and current of Q8, effectively senses the peak power dissipation occurring in this transistor. At a predetermined power level in transistor Q8, the summing network can be chosen so that transistor Q11 conducts sufficiently to turn on transistor Q3. Transistor Q3 then steals the drive current from the base of transistor Q4, and hence limits the power dissipated in Q8. Diode D3 is used to prevent transistor Q11 from turning on, under normal load conditions, when the output signal swings negative. Resistors R9, R13, R14, R15, along with transistors Q12, Q5, and diode D4, similarly limit the power dissipation occurring in the output transistor Q10.

TABLE 1 – Semiconductor Complement

Output Power (Watts-rms)	Load Impedance (Ohms)	Output Transistors		Driver Transistors		Pre-Driver Transistors		Differential Amplifier Transistors
		NPN (Q10)	PNP (Q8)	NPN (Q7)	PNP (Q9)	NPN (Q6)	PNP (Q4)	(Q1 & Q2)
35	4	2N5877	2N5875	MPSU05	MPSU55	MPSA05	MPSA55	MD8001
	8	MJE2801T	MJE2901T	MPSU05	MPSU55	MPSA06	MPSA56	MD8001
50	4	2N5302	2N4399	MPSU05	MPSU55	MPSA06	MPSA56	MD8001
	8	2N5878	2N5876	MPSU06	MPSU56	MPSA06	MPSA56	MD8002
60	4	2N5302	2N4399	MPSU06	MPSU56	MPSA06	MPSA56	MD8001
	8	2N5878	2N5876	MPSU06	MPSU56	MPSA06	MPSA56	MD8002
75	4	MJ802	MJ4502	MPSU06	MPSU56	MPSA06	MPSA56	MD8001
	8	MJ802	MJ4502	MM3007	2N5679	MM3007	MM4007	MD8003
100	4	MJ802	MJ4502	MPSU06	MPSU56	MPSU06	MPSU56	MD8002
	8	MJ802	MJ4502	MM3007	2N5679	MM3007	MM4007	MD8003

The following semiconductors are used at all of the power levels:

Q11 – MPSL01
Q5 – MPSA20
Q12 – MPSL51
Q3 – MPSA70

D1 — 1N5240A or 1N968A (See Note 1)
D2 — MZ2361
D3 & D4 — 1N5236B (See Note 1)

NOTE 1: For a low-cost zener diode, an emitter-base junction of a silicon transistor can be substituted. A transistor similar to the MPS6512 can be used for the 7.5 V zener.

TABLE 2 – Resistor Values and Power Supply Voltages

Output Power (Watts-rms)	Load Impedance (Ohms)	R1 ±5%	R2 ±10%	R3 ±5%	R4 ±5%	R5 ±5%	R6, R7 ±5%	R8, R9 ±10%	R10, R15 ±5%	R11, R14 ±5%	R12, R13 ±5%	V_{CC}
35	4	820	2.7 k	18 k	1.2 k	120	0.39	390	2.7 k	1.5 k	470	±21 V
	8	560	3.9 k	22 k	1.2 k	180	0.47*	240	3.0 k	1.2 k	470	±27 V
50	4	680	3.3 k	22 k	1.2 k	100	0.33	360	3.3 k	1.5 k	470	±25 V
	8	470	4.7 k	27 k	1.2 k	150	0.43*	270	3.9 k	1.2 k	470	±32 V
60	4	620	3.9 k	22 k	1.2 k	120	0.33	430	3.9 k	1.5 k	470	±27 V
	8	430	5.6 k	33 k	1.2 k	120	0.39	300	4.7 k	1.2 k	470	±36 V
75	4	560	4.7 k	27 k	1.2 k	91	0.33	620	5.6 k	1.8 k	470	±30 V
	8	390	6.8 k	33 k	1.2 k	150	0.39	390	6.8 k	1.5 k	470	±40 V
100	4	470	5.6 k	33 k	1.2 k	68	0.39	1.0 k	8.2 k	2.2 k	470	±34 V
	8	330	8.2 k	39 k	1.2 k	100	0.39	510	9.1 k	1.8 k	470	±45 V

NOTE: All of the above resistor values are in ohms and are 1/2 W except for R6 and R7.

*R6 and R7 are 5 W resistors except where * indicates 2 W.

AMPLIFIER OUTPUT LOAD AND TRANSISTOR POWER DISSIPATION CONSIDERATIONS

High-fidelity speaker systems can appear capacitive or inductive as well as resistive. The current and voltage appearing in the amplifier will thus be out of phase when the load appears reactive. Evaluation of several speaker systems showed that nearly 60^{o} of phase shift can occur between the voltage and current. At 60^{o} phase shift, $1/2\ V_{CC}$ and the peak load current can appear simultaneously at the output transistor, or V_{CC} and 1/2 the peak load current can appear, depending on whether the load is capacitive or inductive. Since the short-circuit-protection network must not interfere with normal operating load conditions, the minimum peak power level to which the short-circuit dissipation can be limited is the product of the peak current and voltage appearing at the output transistor under the worst-case allowable phase shift. This means that if we want to allow normal operation into a $\pm 60^{o}$ reactive load, our short-circuit power dissipation will be determined by the following equation:

$$P_{PD(\text{short circuit})} = \frac{V_{CC} \times I_{peak}}{2} \qquad (1)$$

where P_{PD} is the peak dissipation for each output transistor; it is also the total average power dissipation for the amplifier.

The average power dissipation of each transistor is expressed by the equation:

$$P_{AD(\text{short circuit})} = \frac{1/2\ V_{CC} \times I_{peak}}{2} \qquad (2)$$

The worst-case average power dissipation in driver transistors Q7 and Q9 is the power dissipation expressed in Equation 2 divided by the current gain of the output tran-

TABLE 3 – Transistor Heat Sink Requirements

Output Power (Watts-rms)	Load Impedance (Ohms)	Minimum Heat Sinking Required for Safe Operation Under Shunted Load at 50°C Ambient Temperature: Output Transistor Heat Sink (θ_{CA}) (See Note 1)	Driver Transistor Heat Sink (θ_{CA}) (See Note 2)
35	4	4.2°C/W	None
	8	2.4°C/W	None
50	4	3.0°C/W	60°C/W
	8	2.4°C/W	60°C/W
60	4	2.5°C/W	60°C/W
	8	2.0°C/W	60°C/W
75	4	1.6°C/W	35°C/W
	8	1.6°C/W	70°C/W*
100	4	1.0°C/W	20°C/W
	8	1.0°C/W	50°C/W*

NOTE 1: All of the output transistors are in TO-3 packages with the exception of the MJE2801/2901 (35 W/8 Ω), which are in the Case 90 Thermopad† plastic package.

2: All of the driver transistors are in the plastic Uniwatt† package with the exception of those marked *, which are metal cased TO-5.

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sistor. Because of the nature of the short-circuit-protection network, the minimum 1-second safe-operating-area requirement for the output transistor occurs at V_{CC} and is the same as the peak dissipation as determined by Equation 1. The maximum thermal resistance, and consequently the minimum power dissipation rating, required for each output transistor is found by the following equations

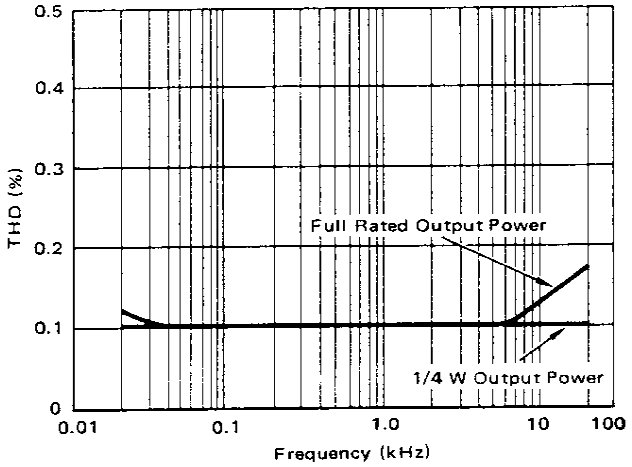

FIGURE 4 – Total Harmonic Distortion versus Frequency at 1/4 W and Full-Rated Output into Nominal Load Impedance

$$\theta_{JC(max)} = \frac{T_{J(max)} - T_A - \theta_{CA} \times P_{AD}}{P_{AD}} \qquad (3)$$

where $T_{J(max)}$ is the maximum junction temperature rating of the device,

T_A is the maximum ambient temperature, and

θ_{CA} is the thermal resistance of the heat sink including the mica insulating washer, if used.

The minimum power dissipation rating of the transistor is found by

$$P_{DM} = \frac{T_{J(max)}}{\theta_{JC(max)}}.$$

COMPONENT VALUES

Table 1 lists the specific resistor values for 4- and 8-ohm amplifiers at 35-, 50-, 60-, 75-, and 100-watt power levels. Table 2 lists the semiconductors required for the same amplifiers. The numbers given in this chart are the nearest standard parts available that will meet or exceed the minimum specifications required for the particular amplifier. Where large amplifier production quantities are involved, the transistor manufacturer should be consulted for the optimum transistor specifications to realize maximum cost savings.

Table 3 lists the minimum heat-sink requirements for the amplifier transistors.

PERFORMANCE

All of the amplifiers listed in Tables 1 and 2 will perform typically as shown as follows:

Output Power: Each amplifier will deliver its full rated rms output power into the nominal load impedance providing the power supply has adequate regulation. Figure 2 shows the power output versus load impedance.

Input Sensitivity: 1 V_{rms} into 10 kΩ for full rated output power.

Frequency Response: Less than 3-dB rolloff from 10 Hz to 100 kHz referenced to 1 kHz.

Power Bandwidth: Full rated output power ±1/2 dB from 20 Hz to 20 kHz. (See Figure 3)

Total Harmonic Distortion: Less than 0.2% at any power level between 100 mW and full rated output and at any frequency between 20 Hz and 20 kHz. (See Figure 4)

Intermodulation Distortion: Less than 0.2% at any power level from 100 mW to full rated output. (60 Hz and 7 kHz mixed 4 to 1)

Damping Factor: Over 150 at any frequency from 20 Hz to 20 kHz.

Square Wave Response: (See Figure 5)

Short Circuit Power Dissipation in Each Output Transistor: (See Figure 6)

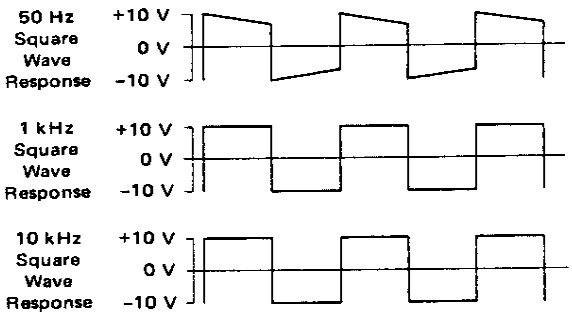

FIGURE 5 – Square Wave Response

Design Example

An electronics company has a requirement for a direct-coupled audio amplifier with the following specifications:

Power Output: 60 watts rms into 8 Ω with normal operation allowed into ±60° reactive load.

Short-Circuit Operation: Circuit has to operate safely at 50°C ambient temperature with the output shorted.

Total Distortion: Less than 0.2%.

Input Sensitivity: 1 V_{rms} (1.4 V_{peak}) input for 60 watts into 8 Ω.

The designer chooses a full-complementary circuit, similar to the circuit of Figure 1, due to its excellent ac and dc performance.

The circuit values are determined as follows:

R1: $R_1 \cong \frac{\text{peak input voltage}}{\text{peak load voltage}} \times R_f$.

R_f = 10 kΩ. The rms load voltage can be found by

$P = \frac{V_{rms}^2}{R_L}$. Since P = 60 W and R_L = 8 Ω,

$V_{rms} = \sqrt{60 \cdot 8}$ = 21 V, and

V_{peak} = 1.4 x V_{rms}

= 31 V.

Therefore $R1 = \frac{1.4}{31} \times 10\text{ k}$

= 450 Ω.

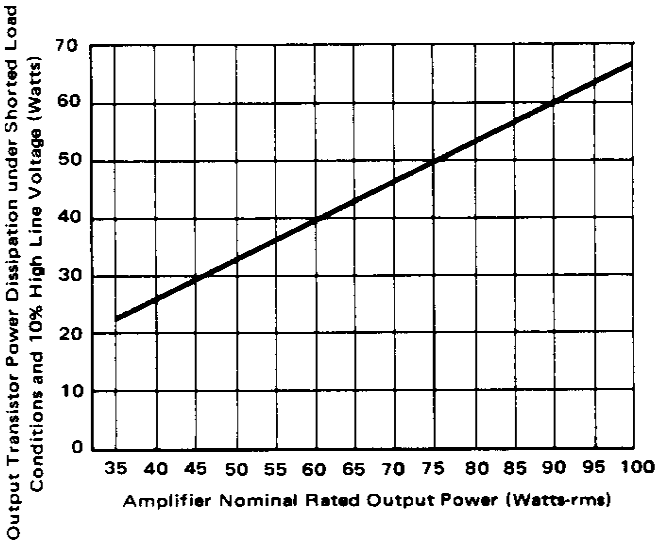

FIGURE 6 – Output Transistor Power Dissipation under Shorted Load Conditions versus Amplifier Nominal Rated Output Power

Choosing the nearest 5% value which gives 1-V sensitivity or better: R1 = 430 Ω.

V_{CC}: $V_{CC} = V_{peak\ load} + V_{R6}$ + saturation and voltage-drop losses.

The sum of V_{R6} and the saturation and voltage drop losses is approximately 5 V for this amplifier.

V_{CC} = 31 + 5 = 36 V

R2: $R2(max) = \frac{V_{CC} - V_{D1}}{I_{bias}(Q1 \text{ and } Q2) + I_{D1}}$

The differential amplifier must be biased for 2 mA through the emitter leg with 680 Ω in the collector circuit. 2 mA is sufficient for good zener diode regulation.

$$R2(max) = \frac{36-10}{0.004}$$

$$= 6.5\ \text{k}\Omega$$

The nearest standard value is 5.6 kΩ.

R3, R4, R5: The voltage at the base of Q6 with respect to the negative supply voltage should be kept under 2.0 V to prevent premature clipping of the negative portion of the output signal.

Therefore, if $\frac{R4}{R3 + R4} \times V_{CC}$ is set equal to 1.3 V, and letting

R4 = 1.2 kΩ,

$\frac{1.2\text{ k}}{(R3 + 1.2\text{ k})} \times 36 = 1.3$, and

R3 = 33 kΩ (Nearest standard value)

Now, $\frac{R4}{R3 + R4} \times V_{CC} = \frac{1.2\text{ k}}{33\text{ k} + 1.2\text{ k}} \times 36 = 1.26$ V

$R5(max) = \frac{1.26 - V_{BE(Q6)}}{\text{Max dc Bias Current of Q4} + 1\text{ mA}}$, and

1 mA extra current allows for resistor tolerances.

$\text{Max dc Bias Current} = \frac{I_{peak\ load}}{h_{FE}\ min(Q9) \times h_{FE}\ min(Q10)}$

$I_{peak\ load}$ is found by:

$I_{peak} = \frac{V_{peak}}{R_L}$

$= \frac{31}{8}$

= 3.9 A

$R5(max) = \frac{0.61}{\frac{3.9}{1000} + 1\text{ mA}} = \frac{0.61}{4.9\text{ mA}} = 125\ \Omega$

Choosing the nearest standard value, R5 = 120 Ω

R6, R7: Due to the nature of the short-circuit-protection network, the voltage appearing across R6 and R7, resulting from the peak load current, should be in the 1.5-to-2.0 V range.

$$R6 = R7 \approx \frac{1.5\ V}{3.9\ A} = 0.384\ \Omega$$

Let $R6 = R7 = 0.39\ \Omega$

Short Circuit Protection Network

Refer to Figures 1 and 7.

R8, R10, R11, R12:

V_{B11} has to be approximately 1.4 V for Q3 to conduct.

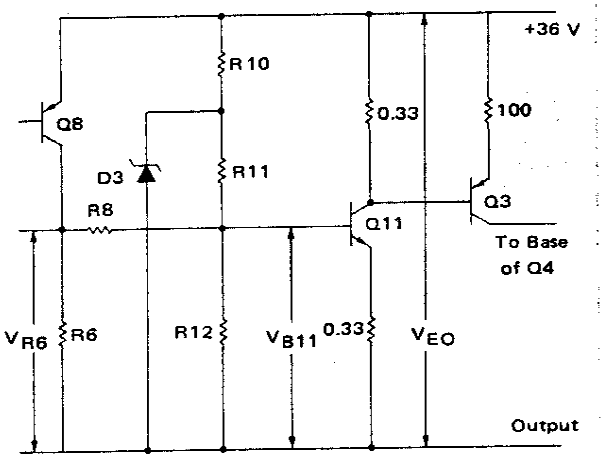

FIGURE 7 – Determining Values of Short-Circuit Network

The maximum current-voltage product appearing at Q8 under normal load conditions occurs at the $\pm 60^{o}$ phase shift limit of the reactive load.

For 60^{o} phase shift, the following equations can be derived for turning Q3 on during shorted output:

$$V_{B11} = 1/2\ K1\ V_{R6(max)} + K2\ V_{EO(max)} \qquad (a)$$

$$V_{B11} = K1\ V_{R6(max)} + 1/2\ K2\ V_{EO(max)} \qquad (b)$$

where $$K1 = \frac{R12}{R8 + R12}$$

$$K2 = \frac{\text{Eq. Resist. of R11 and R8 in Parallel}}{(\text{Eq. Resist. of R11 and R8 in Parallel}) + R11 + R10} \qquad (c)$$

Solving (a) and (b) simultaneously yields:

$$K1\ V_{R6(max)} = K2\ V_{EO(max)}.$$

Since $V_{B11} = 1.4$ V, and substituting equation (c) in equation (a) or (b), yields

$$K1\ V_{R6(max)} = K2\ V_{EO(max)} = 0.933. \qquad (d)$$

Now under shorted output,

$$V_{EO(max)} = V_{CC} = 36\ V, \text{ and}$$

$$V_{R6(max)} = I_{peak}\ R_E = 3.9\ A \times 0.39\ \Omega = 1.53\ V.$$

Therefore, $\frac{R12}{R8 + R12} \times 1.53 = 0.933$ from equation (d). (e)

If we let R12 = 470 Ω, a convenient value, then solving (e) yields:

$$R8 = 300\ \Omega$$

Let $R12' = \frac{R12 \times R8}{R12 + R8} = 183\ \Omega.$

Then, $K2\ V_{EO(max)} = \frac{R12'}{R12' + R11 + R10} \times V_{EO(max)} = 0.933 \qquad (f)$

Also $\frac{R12'}{R12' + R11} \times V_{D3} = 0.933$ in order for the zener diode to conduct.

Let $V_{D3} = 7.5$ V, a convenient value for an economical zener diode.

For equation (f), $\frac{183}{183 + 1.2\ k + R10} \times 36 = 0.933$, so

$R10 = 5.67\ k\Omega.$

To allow V_{D3} to turn on at 10%-high line voltage, R10 should be reduced by 10% so let $R10 = 4.7\ k\Omega$.

Thus the values for the resistors in the short circuit network are:

$R6 = R7 = 0.39\ \Omega$

$R8 = R9 = 300\ \Omega$

$R10 = R15 = 5.6\ k\Omega$

$R11 = R14 = 1.2\ k\Omega$

$R12 = R13 = 470\ \Omega$

TRANSISTOR BASIC REQUIREMENTS

Output Transistors

Q11, Q12: $V_{(BR)CEO} \geq 80$ V at $I_C = 200$ mA (allowing for 10% high line voltage)

$h_{FE} = 20$ minimum at $I_C = 4.0$ A and $V_{CE} = 2.0$ V

The Motorola 2N5876 and 2N5878 meet these specs. The power dissipation rating is 150 watts and the maximum junction temperature is 200°C.

$$\theta_{JC} = \frac{200^{o}C - 25^{o}C}{150} = 1.17^{o}C/W,$$

where θ_{JC} = thermal resistance from junction to case for the transistor.

From equation (2), the power dissipation occurring in each output transistor during shorted load conditions is

$$P_D = \frac{1/2\ V_{CC} \times 3.9\ A}{2} = 35.1\ \text{watts}$$

Allowing for a 30% increase in P_D due to high line voltage, dc idling-power and component tolerance, $P_{D}max$ is:

$$P_{D(max)} = 46 \text{ watts.}$$

Allowing for 50°C ambient temperature:

$$\theta_{CA} \text{ of heat sink} = \frac{T_J - T_A - P_{D(max)}\,\theta_{JC}}{P_{D(max)}}$$

$$= \frac{200 - 50 - 46 \times 1.17}{46} \text{ °C/W}$$

$$\theta_{CA} = 2.0\text{°C/W}$$

Driver Transistors

Q7 and Q9: $V_{(BR)CEO} \geq 80$ V at $I_C = 10$ mA

$h_{FE} \geq 50$ at $I_C = 100$ mA.

The Motorola MPS-U06 and MPS-U56 transistors meet these requirements.

The maximum power dissipation rating of these devices is 5.0 watts and $T_{J(max)} = 135°C$.

$$\theta_{JC} = \frac{135 - 25}{5} = 22\text{°C/W}$$

The maximum power dissipation in the driver transistor is:

$$\frac{P_{D(max)}}{h_{FE} \text{ of output}}$$

The h_{FE} of the output is now the current gain at the short-circuit current level:

$$I_{\text{short circuit}} = \frac{46 \text{ W}}{40 \text{ V}} \times 2 = 2.3 \text{ A (at high line voltage).}$$

The 2N5876 and 2N5878 have $h_{FE} \geq 45$ at 2.3 A.

$$\text{Therefore, } P_{D(driver)} = \frac{46}{45} = 1.03 \text{ W.}$$

$$\theta_{CA} \text{ of heat sink} = \frac{135 - 50 - 22 \times 1.03}{1.03} = 60\text{°C/W}$$

$$\theta_{CA} = 60\text{°C/W}$$

Pre-Driver Transistor

Q4 and Q9: $V_{(BR)CEO} \geq 80$ V

$h_{FE} \geq 75$ at $I_C = 10$ mA and

$V_{CE} = 1$ V

The Motorola MPS-A06 and MPS-A56 meet these requirements. The maximum power dissipation rating on this device is 500 mW and $T_{J(max)} = 135°C$.

$$P_{D(pre\text{-}driver)} = \frac{P_{D(driver)}}{h_{FE} \text{ of driver}} + P_{DC}$$

P_{DC} is due to the bias current used in the calculation of R5 and is:

$$\frac{1030}{50} \text{ mW} + 40 \text{ V} \times 5 \text{ mA} = 220 \text{ mW}$$

$P_{D(max)}$ at 50°C for the transistor is:

$$500 \text{ mW} - \frac{500 \text{ mW}}{135°C} \times 50°C = 315 \text{ mW}$$

Since this is greater than the worst-case dissipation, $P_{D(pre\text{-}driver)}$, Q4 and Q9 do not require any heat sink.

SHORT-CIRCUIT PROTECTION TRANSISTORS

Q11, Q12, Q4, Q5:

All of these transistors operate at low current levels and can be TO-92 type plastic transistors.

Q11 and Q12 should have $h_{FE} \geq 40$ at 2 mA and $V_{(BR)CEO} \geq 80$ V.

The MPS-L01 and MPS-L51 meet these specifications.

Q4 and Q5 should have $h_{FE} \geq 25$ at 1 mA and $V_{(BR)CEO} \geq 10$ V. The MPS-A20 and MPS-A70 meet these specifications.

Now the designer has all of the component values and semiconductor types required for the 60-watt amplifier.

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