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SEMICONDUCTOR TECHNICAL DATA

Document order number: MC33999
Rev 1.0, 01/2004

Preliminary Information

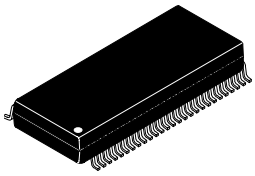
16-Output Switch with SPI and PWM Control

33999

POWER DUAL OCTAL SERIAL SWITCH WITH SERIAL PERIPHERAL INTERFACE I/O

The 33999 is a 16-output low-side switch with a 24-bit serial input control. It is designed for a variety of applications including inductive, incandescent, and LED loads. The Serial Peripheral Interface (SPI) provides both input control and diagnostic readout. Eight parallel inputs are also provided for direct Pulse Width Modulation (PWM) control of eight dedicated outputs. Additionally, an output-programmable PWM input provides PWM of any combination of outputs. A dedicated reset input provides the ability to clear all internal registers and turn all outputs off.

The 33999 directly interfaces with microcontrollers and is compatible with both 3.3 V and 5.0 V CMOS logic levels. The 33999, in effect, serves as a bus expander and buffer with fault management features that reduces the MCU's fault management burden.



EK (Pb-FREE) SUFFIX
CASE 1390-01
54-LEAD SOICW EXPOSED PAD

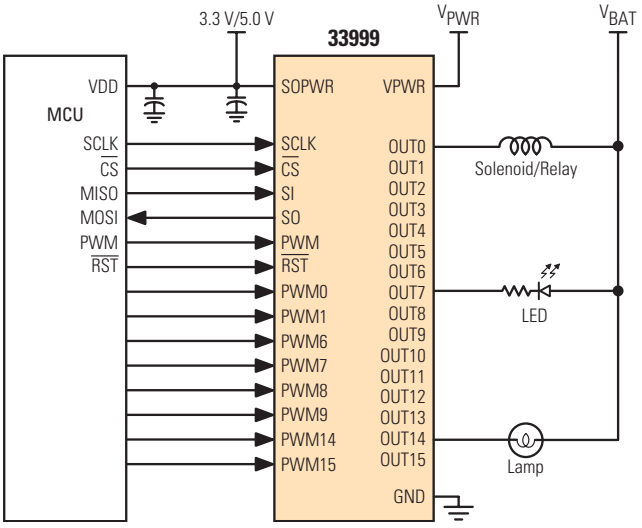
Features

- Designed to Operate 5.0 V ≤ V_{PWR} ≤ 27 V
- 24-Bit SPI for Control and Fault reporting, 3.3 V/5.0 V Compatible
- Outputs Are Current Limited (0.9 A to 2.5 A) to Drive Incandescent Lamps
- Output Voltage Clamp of +50 V During Inductive Switching
- On/Off Control of Open Load Detect Current (LED Application)
- V_{PWR} Standby Current < 10 μA
- $R_{DS(ON)}$ of 0.55 Ω at 25°C Typical
- Independent Overtemperature Protection
- Output Selectable for PWM Control
- Output ON Short-to-V_{BAT} and OFF Short-to-Ground/Open Detection
- 54-Pin Exposed Pad Package for Thermal Performance
- Pb-Free Packaging Designated by Suffix Code EK

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33999EK/R2	-40°C to 125°C	54 SOICW-EP

33999 Simplified Application Diagram



PRELIMINARY

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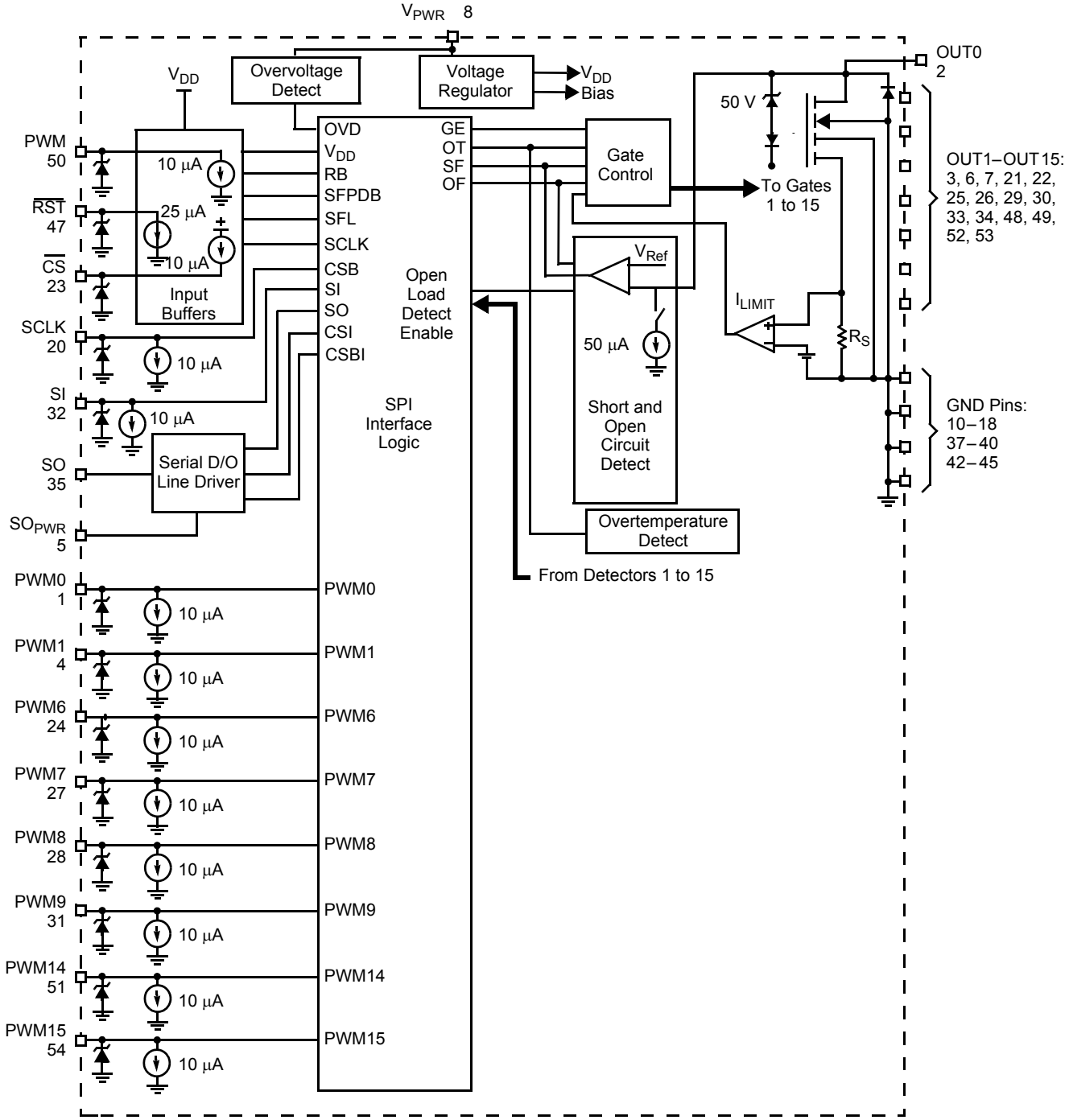

Figure 1. 33999 Simplified Internal Block Diagram

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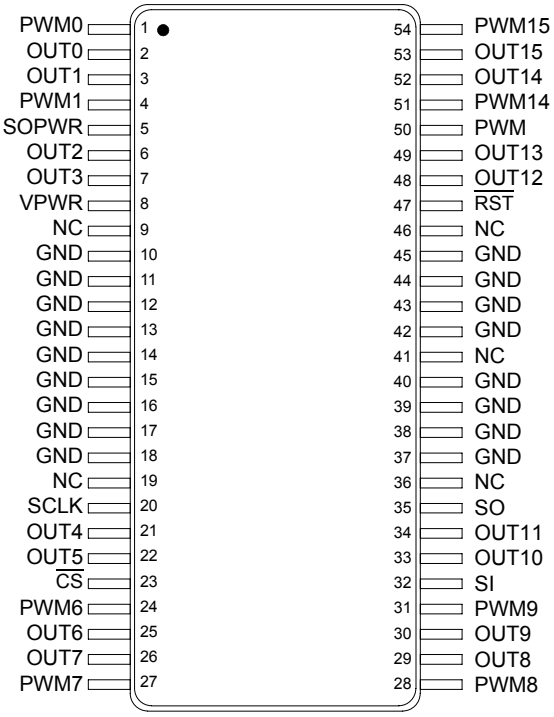

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1, 4, 24, 27, 28, 31, 51, 54	PWM0, PWM1, PWM6–PWM9, PWM14, PWM15	PWMn Input	Parallel PWM control Input pins. Allows direct PWM control of eight outputs.
2, 3, 6, 7, 21, 22, 25, 26, 29, 30, 33, 34, 48, 49, 52, 53	OUT0–OUT15	Output 0–Output 15	Low-side driver outputs.
5	SOPWR	SO_{PWR} Supply Pin	Power supply pin to the SO output driver.
8	VPWR	Battery Input	Battery supply input pin.
9, 19, 36, 41, 46	NC	No Connect	These pins have no connection.
10–18, 37–40, 42–45	GND	Ground	Ground for logic, analog, and power output devices.
20	SCLK	System Clock	System Clock for internal shift registers of the 33999.
23	$\overline{CS}$	Chip Select	SPI control chip select input pin from MCU to 33999.
32	SI	Serial Input	Serial data input pin to the 33999.
35	SO	Serial Output	Serial data output pin
47	$\overline{RST}$	Reset	Active low reset input pin.
50	PWM	PWM Control Pin	PWM control input pin. Supports PWM on any combination of outputs.

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MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
VPWR Supply Voltage (Note 1)	V_{PWR}	-1.5 to 50	V
SPI Interface Logic Supply Voltage (Note 1)	SO_{PWR}	-0.3 to 7.0	V
SPI Interface Logic Input Voltage ($\overline{CS}$, PWM, SI, SO, SCLK, $\overline{RST}$, PWMn) (Note 1)	V_{IN}	-0.3 to 7.0	V
Output Drain Voltage	V_{DS}	-0.3 to 45	V
Frequency of SPI Operation (Note 2)	f_{SPI}	6.0	MHz
Output Clamp Energy (Note 3)	E_{CLAMP}	50	mJ
ESD Voltage (Note 4) Human Body Model (Note 5) Machine Model (Note 6)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Case Temperature	T_C	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Power Dissipation (T_A = 25°C) (Note 7)	P_D	2.0	W
Lead Soldering Temperature (Note 8)	T_{SOLDER}	260	°C
Thermal Resistance Junction-to-Ambient (Note 9) Junction-to-Case (Note 10) Junction-to-Board	 $R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JB}$	 60 1.2 8.0	°C/W

Notes

1. Exceeding these limits may cause malfunction or permanent damage to the device.
2. This parameter is guaranteed by design but not production tested.
3. Maximum output clamp energy capability at 150°C junction temperature using single non-repetitive pulse method.
4. ESD data is available upon request.
5. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
6. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
7. Maximum power dissipation with no heat sink used.
8. Lead soldering temperature limit is for 10 seconds maximum duration. Not designed of immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Tested per JEDEC test JESD52-2 (single-layer PWB).
10. Tested per JEDEC test JESD51-8 (two-layer PWB).

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STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 3.1 V ≤ SO_{PWR} ≤ 5.5 V, 5.0 V ≤ V_{PWR} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range Fully Operational	$V_{PWR(FO)}$	 5.0	 –	 27	V
Supply Current All Outputs ON, I_{OUT} = 0.3 A	$I_{PWR(ON)}$	 –	 4.0	 8.0	mA
Sleep State Supply Current at $\overline{RST}$ ≤ 0.2 SO_{PWR} and/or SO_{PWR} ≤ 0.5 V	$I_{PWR(SS)}$	-10	1.0	10	µA
Overvoltage Shutdown	V_{OV}	27.5	31.5	35	V
Overvoltage Shutdown Hysteresis	$V_{OV\ (HYS)}$	0.8	1.4	2.3	V
VPWR Undervoltage Shutdown	$V_{PWR(UV)}$	–	3.2	3.5	V
SPI Interface Logic Supply Voltage	SO_{PWR}	3.1	–	5.5	V
SPI Interface Logic Supply Current ($\overline{RST}$ Pin High)	$I_{SOPWR(\overline{RST}H)}$	100	–	500	µA
SPI Interface Logic Supply Current ($\overline{RST}$ Pin Low)	$I_{SOPWR(\overline{RST}L)}$	-10	–	10	µA
SPI Interface Logic Supply Undervoltage Lockout Threshold	$SO_{PWR(UNVOL)}$	2.0	2.5	3.0	V
POWER OUTPUT					
Drain-to-Source ON Resistance (I_{OUT} = 0.35 A, V_{PWR} = 13 V) T_J = 125°C T_J = 25°C T_J = -40°C	$R_{DS(ON)}$	 – – –	 0.75 0.55 0.45	 1.2 1.2 1.2	Ω
Output Self-Limiting Current Outputs Programmed ON	$I_{OUT(lim)}$	 0.9	 1.2	 2.5	A
Output Fault Detect Threshold (Note 11) Outputs Programmed OFF	$V_{OUTth(F)}$	 2.5	 3.0	 3.5	V
Output OFF Open Load Detect Current (Note 12) Outputs Programmed OFF (V_{PWR} = 5.0 V) Outputs Programmed OFF (V_{PWR} = 13 V, 18 V)	 $I_{OCO(5)}$ $I_{OCO(13,18)}$	 25 30	 50 50	 100 100	µA
Output Clamp Voltage 2.0 mA ≤ I_{OUT} ≤ 200 mA	V_{CL}	 45	 50	 55	V
Output Leakage Current SO_{PWR} ≤ 2.0 V	$I_{OUT(lkg)}$	 -10	 2.0	 10	µA
Overtemperature Shutdown (Outputs OFF) (Note 13)	T_{LIM}	155	165	180	°C
Overtemperature Shutdown Hysteresis (Note 13)	$T_{LIM(hys)}$	5.0	10	20	°C

Notes

11. Output Fault Detect Thresholds with outputs programmed OFF. Output Fault Detect Thresholds are the same for output open and shorts.
12. Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded to be OFF.
13. This parameter is guaranteed by design but is not production tested.

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STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions of 3.1 V ≤ SO_{PWR} ≤ 5.5 V, 5.0 V ≤ V_{PWR} ≤ 18 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic Voltage Thresholds (Note 14)	$V_{INLOGIC}$	0.8	–	2.2	V
Input Logic Voltage Thresholds for $\overline{RST}$	$V_{IN\overline{RST}}$	SO_{PWR}/2-0.7	SO_{PWR}/2	SO_{PWR}/2+0.7	V
SI Pull-Down Current SI = 5.0 V	I_{SI}	2.0	10	30	µA
$\overline{CS}$ Pull-Up Current $\overline{CS}$ = 0 V	$I_{\overline{CS}}$	-30	-10	-2.0	µA
SCLK Pull-Down Current SCLK = 5.0 V	I_{SCLK}	2.0	10	30	µA
$\overline{RST}$ Pull-Down Current $\overline{RST}$ = 5.0 V	$I_{\overline{RST}}$	5.0	25	50	µA
PWM and PWMn Pull-Down Current	I_{PWM}	2.0	10	30	µA
SO High-State Output Voltage $I_{SO\text{-}high}$ = -1.6 mA	V_{SOH}	SO_{PWR}-0.4	SO_{PWR}-0.2	–	V
SO Low-State Output Voltage $I_{SO\text{-}low}$ = 1.6 mA	V_{SOL}	–	–	0.4	V
Input Capacitance on SCLK, SI, Tri-State SO, $\overline{RST}$ (Note 15)	C_{IN}	–	–	20	pF

Notes

14. Upper and lower logic threshold voltage levels apply to SI, $\overline{CS}$, SCLK, PWM, and PWMn.
15. This parameter is guaranteed by design but is not production tested.

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DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of 3.1 V ≤ SO_{PWR} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, -40°C ≤ T_C ≤ 125°C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with V_{PWR} = 13 V, T_A = 25°C.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Slew Rate R_L = 56 Ω (Note 16)	SR	1.0	2.0	10	V/μs
Output Turn ON Delay Time (Note 17)	$t_{DLY(on)}$	1.0	15	50	μs
Output Turn OFF Delay Time (Note 17)	$t_{DLY(off)}$	1.0	15	50	μs
Output ON Short Fault Disable Report Delay (Note 18)	$t_{DLY(short)}$	100	–	450	μs
Output OFF Open Fault Delay Time (Note 18)	$t_{DLY(open)}$	100	–	450	μs
Output PWM Frequency	t_{FREQ}	–	–	2.0	kHz
DIGITAL INTERFACE TIMING					
Required Low State Duration on V_{PWR} for Reset V_{PWR} ≤ 0.2 V (Note 19)	$t_{\overline{RST}}$	–	–	10	μs
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)	t_{LAG}	50	–	–	ns
SI to Falling Edge of SCLK (Required Setup Time)	$t_{SI(su)}$	16	–	–	ns
Falling Edge of SCLK to SI (Required Setup Time)	$t_{SI(hold)}$	20	–	–	ns
SI, $\overline{CS}$, SCLK Signal Rise Time (Note 20)	$t_{r(SI)}$	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time (Note 20)	$t_{f(SI)}$	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low Impedance (Note 21)	$t_{SO(en)}$	–	–	50	ns
Time from Rising Edge of $\overline{CS}$ to SO High Impedance (Note 22)	$t_{SO(dis)}$	–	–	50	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 23)	t_{VALID}	–	25	80	ns

Notes

16. Output slew rate measured across a 56 Ω resistive load.
17. Output turn ON and OFF delay time measured from 50% rising edge of $\overline{CS}$ to 90% and 10% of initial voltage.
18. Duration of fault before fault bit is set. Duration between access times must be greater than 450 μs to read faults.
19. This parameter is guaranteed by design but is not production tested.
20. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
21. Time required for valid output status data to be available on SO pin.
22. Time required for output status data to be terminated at SO pin.
23. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

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Timing Diagram

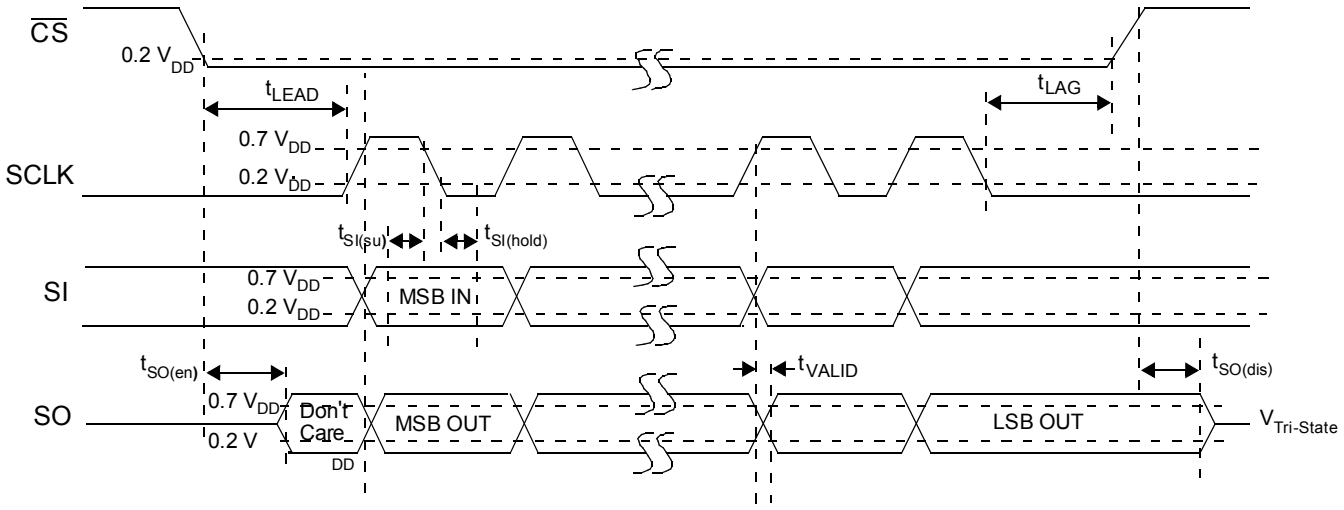

Figure 2. SPI Timing Characteristics

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SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33999 is designed and developed for automotive and industrial applications. It is a 16-output power switch having 24-bit serial control. The 33999 incorporates SMARTMOS technology having CMOS logic, bipolar/MOS analog circuitry, and independent DMOS power output transistors. Many benefits are realized as a direct result of using this mixed technology. Figure 1, page 2, illustrates a simplified internal block diagram of the 33999.

MCU INTERFACE DESCRIPTION

In operation the 33999 functions as a 16-output serial switch serving as a microcontroller unit (MCU) bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions.

The 33999 directly interfaces to an MCU, operating at system clock serial frequencies up to 6.0 MHz using a Serial Peripheral Interface (SPI) for control and diagnostic readout.

Figure 3 illustrates the basic SPI configuration between an MCU and one 33999.

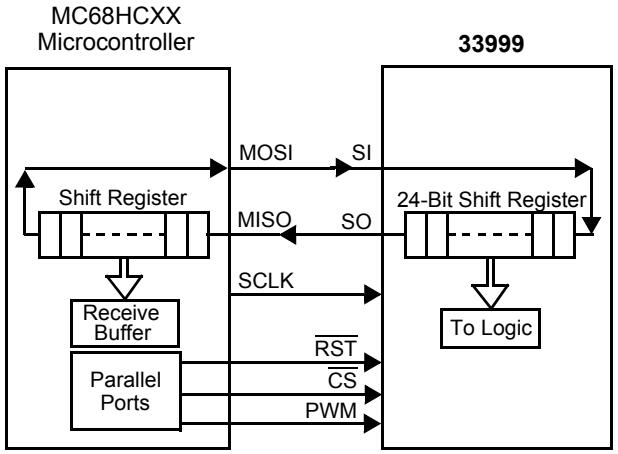

Figure 3. 33999 SPI Interface with Microcontroller

All inputs are compatible with 3.3 V/5.0 V CMOS logic levels and incorporate positive logic. An input programmed to a logic low state (< 0.8 V) has the corresponding output OFF. Conversely, an input programmed to a logic high state (> 2.2 V) has the output being controlled ON. Diagnostics is treated in a similar manner—outputs with a fault will feed back (via SO) to the microcontroller a logic [1], while normal operating outputs will provide a logic [0].

The 33999 may be controlled and provide diagnostics using a daisy chain configuration or in parallel mode. Figure 4 shows the daisy chain configuration using the 33999. Data from the MCU is clocked daisy chain through each device while the Chip Select bit ($\overline{CS}$) is commanded low by the MCU. During each clock cycle, output status from the daisy-chained 33999s is being transferred back to the MCU via the Master In Slave Out (MISO) line. On rising edge of $\overline{CS}$, data stored in the input register is then transferred to the output driver. Daisy chain control of the 33999 requires 24 bits per device.

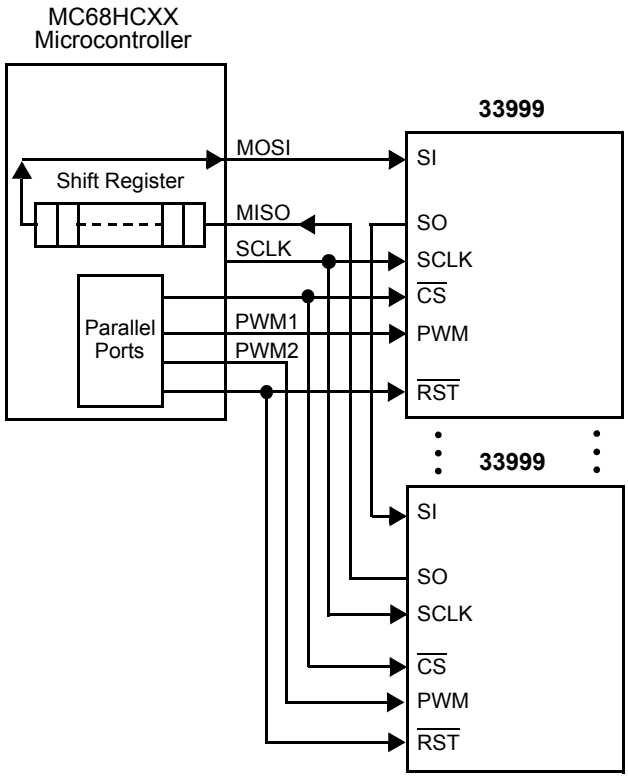

Figure 4. 33999 SPI System Daisy Chain

Multiple 33999 devices can be controlled in a parallel input fashion using the SPI. Figure 5, page 10, illustrates potentially 32 loads being controlled by two dedicated parallel MCU ports used for chip select.

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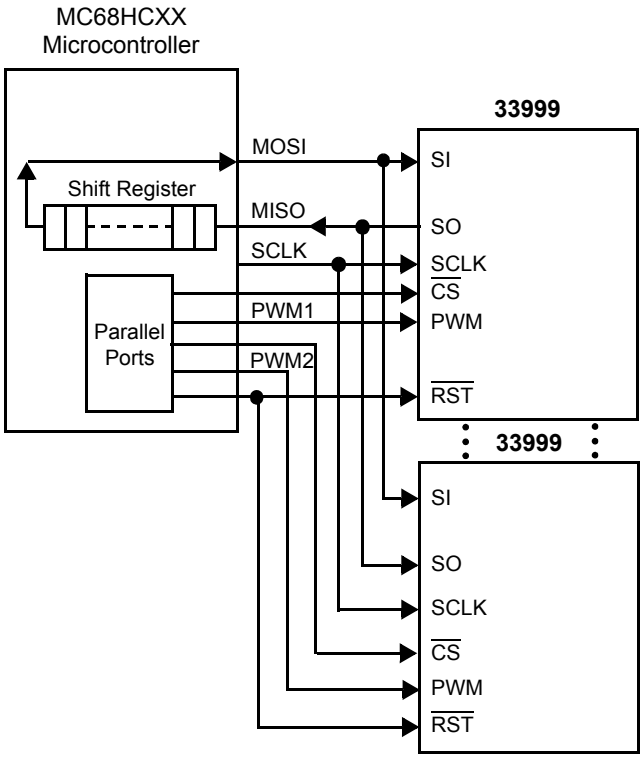

Figure 5. Parallel Inputs SI Control

FUNCTIONAL PIN DESCRIPTION

Chip Select ($\overline{CS}$) Pin

The system MCU selects which 33999 is to be communicated with through the use of the Chip Select ($\overline{CS}$) pin. When the $\overline{CS}$ pin is in a logic low state, data can be transferred from the MCU to the 33999 and vise versa. Clocked-in data from the MCU is transferred from the 33999 Shift register and latched into the power outputs on the rising edge of the $\overline{CS}$ signal. On the falling edge of the $\overline{CS}$ signal, output fault status information is transferred from the Power Outputs Status register into the device's SO Shift register. The SO pin output driver is enabled when $\overline{CS}$ is low, allowing information to be transferred from the 33999 to the MCU. To avoid any spurious data, it is essential the high-to-low transition of the $\overline{CS}$ signal occur only when SCLK is in a logic low state.

System Clock (SCLK) Pin

The System Clock (SCLK) pin clocks the Internal Shift register of the 33999. The Serial Input (SI) pin accepts data into the Input Shift register on the falling edge of the SCLK signal while the Serial Output (SO) pin shifts data information out of the Shift register on the rising edge of the SCLK signal. False clocking of the Shift register must be avoided to guarantee validity of data. It is essential the SCLK pin be in a logic low state whenever the Chip Select ($\overline{CS}$) pin makes any transition. For this reason, it is recommended, though not necessary, that the SCLK pin is commanded to a low logic state as long as the device is not accessed ($\overline{CS}$ in logic high state). When the $\overline{CS}$ is in a logic high state, any signal at the SCLK and SI pins is ignored and the SO is tri-stated (high impedance).

Serial Input (SI) Pin

The Serial Input (SI) pin is used to enter one of seven serial instructions into the 33999. SI SPI bits are latched into the Input Shift register on each falling edge of SCLK. The Shift register is full after 24 bits of information are entered. The 33999 operates on the command word on the rising edge of $\overline{CS}$. To preserve data integrity, exercise care to not transition SI as the SCLK transitions from high-to-low state (see Figure 2, page 8).

Serial Output (SO) Pin

The Serial Output (SO) pin transfers fault status data from the 33999 to the MCU. The SO pin remains tri-state until the $\overline{CS}$ pin transitions to a logic low state. All faults on the 33999 are reported to the MCU as logic [1]. Conversely, normal operating outputs with nonfaulted loads are reported as logic [0]. On the falling edge of the $\overline{CS}$ signal, output fault status information is transferred from the Power Outputs Status register into the device's SO Shift register. The first eight positive transitions of SCLK will provide Any Fault (bit 23), Overvoltage Fault (bit 22), followed by six logic [0]s (bits 21 to 16). The next 16 successive positive clock provides fault status for output 15 to output 0. The SI/SO shifting of data follows a first-in, first-out protocol with

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both input and output words transferring the Most Significant Bit (MSB) first.

SO Output driver Power Supply (SOPWR) Pin

The SOPWR pin is used to supply power to the 33999 SO output driver and Power-ON Reset (POR) circuit. To achieve low standby current on VPWR supply, power must be removed from the SOPWR pin. The 33999 will be in reset with all drivers OFF when SO_{PWR} is below 2.5 V. The 33999 does not detect overvoltage on the SOPWR supply pin.

Output/Input (OUT0–OUT15) Pins

These pins are low-side output switches controlling the load.

Reset ($\overline{RST}$) Pin

The Reset ($\overline{RST}$) pin is the active low reset input pin used to turn OFF all outputs, thereby clearing all internal registers.

Battery Input (VPWR) Pin

The VPWR pin is used as the input power source for the 33999. The voltage on VPWR is monitored for overvoltage protection and shutdown. An overvoltage condition (> 50 μs) on the VPWR pin causes the 33999 to shut down all outputs until the overvoltage condition is removed. Upon return to normal input voltage, the outputs respond as programmed by the overvoltage bit in the Global Shutdown/Retry Control register. The overvoltage threshold on the VPWR pin is specified as 27.5 V to 35 V with 1.4 V typical hysteresis. Following an overvoltage shutdown of output drivers, the Overvoltage Fault and the Any Fault bits in the SO bit stream will be logic [1].

PWM Pin

The PWM Control pin is provided to support PWM of any combination of outputs. Logic for PWM control is provided in the LOGIC OPERATION section (below).

Pulse Width Module (PWMn) Pins

PWM0, PWM1, PWM6, PWM7, PWM8, PWM9, PWM14, and PWM15 input pins allow direct PWM control of OUT0, OUT1, OUT6, OUT7, OUT8, OUT9, OUT14, and OUT15, respectively. Logic for PWM control is provided in the LOGIC OPERATION section.

LOGIC OPERATION

Introduction

The 33999 provides flexible control of 16 low-side driver outputs. The device allows PWM and ON/OFF control through the use of several input command words. This section describes the logic operation and command registers of the 33999.

The 33999 message set consists of seven messages as shown in Table 1. Bits 23 through 18 determine the specific command and bits 15 through 0 determine how a specific output will operate. The 33999 operates on the command word on the rising edge of $\overline{CS}$.

Note Upon Power-ON Reset all bits are defined as shown in Table 1.

Table 1. SPI Control Commands

	MSB																							LSB
Commands	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ON/OFF Control Register 0 = off, 1 = on	0	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Open Load Current Enable 0 = disable, 1 = enable	0	0	0	0	0	1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Global Shutdown/Retry Control 0 = shutdown, 1 = retry	0	0	0	0	1	0	Thermal Bit 0	Over-voltage 0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SFPD Control 1 = therm only, 0 = V_{DS}	0	0	0	0	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
PWM Enable 0 = SPI only, 1 = PWM	0	0	0	1	0	0	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AND/OR Control 0 = PWM pin AND with SPI 1 = PWM pin OR with SPI	0	0	0	1	0	1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Reset	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
SO Response 0 = No Fault, 1 = Fault	Any Fault	Over-voltage	0	0	0	0	0	0	OUT 15	OUT 14	OUT 13	OUT 12	OUT 11	OUT 10	OUT 9	OUT 8	OUT 7	OUT 6	OUT 5	OUT 4	OUT 3	OUT 2	OUT 1	OUT 0

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ON/OFF Control Register

To program the 16 outputs of the 33999 ON or OFF, a 24-bit serial stream of data is entered into the SI pin. The first 8 bits of the control word are used to identify the on/off command and the remaining 16 bits are used to turn ON or OFF the specific output driver.

Open Load Current Enable Control Register

The Open Load Enable Control register is provided to enable or disable the 50 μA open load detect pull-down current. This feature allows the device to be used in LED applications. Power-ON Reset (POR) or the $\overline{RST}$ pin or the RESET command disables the 50 μA pull-down current. No open load fault will be reported with the pull-down current disabled. For open load to be active, the user must program the Open Load Current Enable Control register with logic [1].

Global Shutdown/Retry Control Register

The Global Shutdown/Retry Control register allows the user to select the global fault strategy for the outputs. The Overvoltage control bit (bit 16) sets the operation of the outputs when returning from overvoltage. Setting the Overvoltage bit to logic [0] will force all outputs to remain OFF when V_{PWR} returns to normal level. Setting the Overvoltage bit to logic [1] will command outputs to resume their previous state when V_{PWR} returns to normal level. Bit 17 is the global thermal bit. When bit 17 is set to logic [0], all outputs will shut down when thermal limit is reached and remain off even after cooled. With bit 17 set to logic [1], all outputs will shut down when thermal limit is reached and will retry when cooled.

Short Fault Protect Disable (SFPD) Control Register

All outputs contain a current limit and thermal shutdown with programmable retry. The SFPD control bits are used for fast shutdown of the output when an overcurrent condition is detected but thermal shutdown has not been achieved.

The SFPD Control register allows selection of specific outputs for incandescent lamp loads and specific outputs for inductive loads. By programming the specific SFPD bit as logic [1], output will rely on Overtemperature Shutdown only. Programming the specific SFPD bit as logic [0] will shut down the output after 100 μs to 450 μs during turn on into short circuit. The decision for shutdown is based on output drain-to-source voltage (V_{DS}) > 2.7 V. This feature is designed to provide protection to loads that experience more than expected currents and require fast shutdown. The 33999 is designed to operate in both modes with full device protection.

PWM Enable Register

The PWM Enable register determines the outputs that are PWM controlled. The first 8 bits of the 24 bit SPI message word are used to identify the PWM enable command, and the remaining 16 bits are used to enable or disable the PWM of the output drivers.

A logic [1] in the PWM Enable register allows the user to OR/AND the PWM input with SPI Control bit and disables the specific parallel control input (PWM0, PWM1, PWM6, PWM7, PWM8, PWM9, PWM14, and PWM15).

A logic [0] in the PWM Enable register will disable the PWM to a specific output and allow the user to use the parallel PWM control inputs (PWM0, PWM1, PWM6, PWM7, PWM8, PWM9, PWM14, and PWM15) and the SPI ON/OFF Control bits. Power-ON Reset (POR) or the $\overline{RST}$ pin or the RESET command will set the PWM enable register to logic[0].

AND/OR Control Register

The AND/OR Control register describes the condition by which the PWM pin controls the output driver. A logic [0] in the AND/OR Control register will AND the PWM pin with the control bit in the SPI Control register. Likewise, a logic [1] in the AND/OR Control register will OR the PWM pin with the control bit in the ON/OFF Control register (see Figure 6).

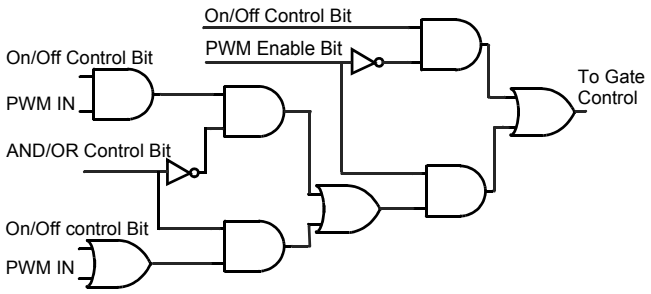

Figure 6. PWM Control Logic Diagram

Serial Output (SO) Response Register

Fault reporting is accomplished through the SPI interface. All logic [1]s received by the MCU via the SO pin indicate fault. All logic [0]s received by the MCU via the SO pin indicate no fault. All fault bits are cleared on the positive edge of $\overline{CS}$. SO bits 15 to 0 represent the fault status of outputs 15 to 0. SO bits 21 to 16 will always return logic [0]. Bit 22 provides overvoltage condition status, and bit 23 is set when any fault is present in the IC. The timing between two write words must be greater than 450 μs to allow adequate time to sense and report the proper fault status.

Reset Command

The RESET command turns all outputs OFF and sets all internal registers to their Power-ON Reset state (refer to Table 1).

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FAULT OPERATION

On each SPI communication, a 24-bit command word is sent to the 33999 and a 24-bit fault word is received from the 33999.

The Most Significant Bit (MSB) is sent and received first.

Command Register Definition:
0 = Output Command Off
1 = Output Command On

SO Definition:
0 = No fault
1 = Fault

Table 2. Fault Operation

Serial Output (SO) Pin Reports	
Overtemperature	Fault reported by Serial Output (SO) pin.
Overcurrent	SO pin reports short-to-battery/supply or overcurrent condition.
Output ON Open Load Fault	Not reported.
Output OFF Open Load Fault	SO pin reports output “OFF” open load condition.
Device Shutdowns	
Overvoltage	Total device shutdown at V_{PWR} = 27.5 V to 35 V. Resumes normal operation with proper voltage. Upon recovery all outputs assume previous state or OFF based on the Overvoltage bit in the Global Shutdown/Retry Control register.
Overtemperature	Only the output experiencing an overtemperature shuts down. Output may auto-retry or remain OFF according to the control bits in the Global Shutdown/Retry Control register.
Overcurrent	Output will remain in current limit 0.9 A to 2.5 A until thermal limit is reached. When thermal limit is reached, device will enter overtemperature shutdown. Output will operate as programmed in the Global Shutdown/Retry Control register. Fault flag in SO Response word will be set.

APPLICATIONS

Power Consumption

The 33999 is designed with one Sleep mode and one Operational mode. In Sleep mode ($SO_{PWR} \leq 2.0$ V), the current consumed by the VPWR pin is less than 50 μA.To place the 33999 in Sleep mode, turn all outputs OFF and remove power from the SOPWR pin. During normal operation, 500 μA is drawn from the SO_{PWR} supply and 8.0 mA from the V_{PWR} supply.

Paralleling of Outputs

Using MOSFETs as output switches allows the connection of any combination of outputs together. The $R_{DS(ON)}$ of MOSFETs has an inherent positive temperature coefficient providing balanced current sharing between outputs without destructive operation. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(ON)}$, while the Output Current Limit increases correspondingly. Output OFF Open Load Detect current may increase based on how the Output OFF Open Load Detect is programmed. Paralleling outputs from two or more different IC devices is possible but not recommended.

Care must be taken when paralleling outputs for inductive loads. The Output Voltage Clamp of the output drivers may not match. One MOSFET output must be capable of the inductive energy from the load turn OFF.

SPI Integrity Check

Checking the integrity of the SPI communication is recommended upon initial power-up of the SOPWR pin. After initial system startup or reset, the MCU writes one 48-bit pattern to the 33999.

The first 24 bits read by the MCU is the fault status of the outputs, while the second 24 bits is the first bit pattern sent. By the MCU receiving the same bit pattern it sent, bus integrity is confirmed. Please note the second 24 bits the MCU sends to the 33999 are the command bits to program registers or activate outputs on the rising edge of $\overline{CS}$.

Output OFF Open Load Fault

An Output OFF Open Load Fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load Fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

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Each 33999 output has an internal 50 μA pull-down current source. The pull-down current is disabled on power-up and must be enabled for Open Load Detect to function. Once enabled, the 33999 will only shut down the pull-down current in Sleep mode or when disabled via SPI.

During output switching, especially with capacitive loads, a false Output OFF Open Load Fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 μs to 450 μs is incorporated. The duration for which a false fault may be reported is a function of the load impedance, $R_{DS(ON)}$, C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR}. The rising edge of $\overline{CS}$ triggers the built-in fault delay timer. The timer must time out before the fault comparator is enabled to detect a faulted threshold. Once the condition causing the Open Load Fault is removed, the device resumes normal operation. The Open Load Fault, however, will be latched in the output SO Response register for the MCU to read.

Shorted Load Fault

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply, or by an output experiencing a current greater than the current limit.

Three safety circuits progressively in operation during load short conditions afford system protection:

1. The device's output current is monitored in an analog fashion using a SENSEFET approach and is current limited.
2. With the output in current limit, the drain-to-source voltage increases. By setting the SFPD bit to 0, the output shuts down on V_{DS} > 2.7 V typical after 450 μs.
3. The output thermal limit of the device is sensed and, when attained, causes only the specific faulted output to shut down. The device remains OFF until cooled. The device then operates as programmed by the shutdown/retry bit. The cycle continues until the fault is removed or the command bit instructs the output OFF.

All three protection schemes set the Fault Status bit (bit 23 in the SO Response register) to logic [1].

Undervoltage Shutdown

An undervoltage SO_{PWR} condition results in the global shutdown of all outputs and reset of all control registers. The undervoltage threshold is between 2.0 V and 3.0 V.

An undervoltage condition at the VPWR pin results in an output shutdown and reset. The undervoltage threshold is between 3.2 V and 3.5 V. When V_{PWR} is between 5.0 V and 3.5 V, the output may operate per the command word and the status is reported on SO pin, though this is not guaranteed.

Output Voltage Clamp

Each output of the 33999 incorporates an internal voltage clamp to provide fast turn-OFF and transient protection of each output. Each clamp independently limits the drain-to-source voltage to 50 V. The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) (see Figure 7).

Characterization of the output clamps, using a single pulse non-repetitive method at 0.3 A, indicates the maximum energy to be 50 mJ at 150°C junction temperature per output.

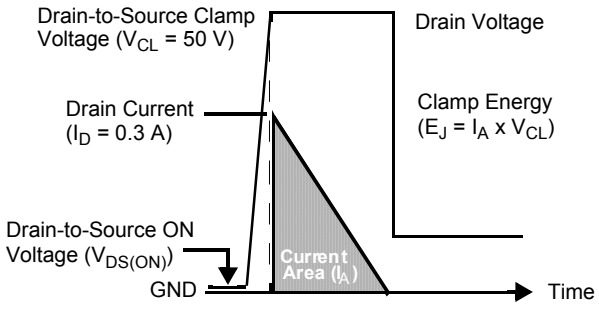

Figure 7. Output Voltage Clamping

Reverse Battery Protection

The 33999 device requires external reverse battery protection on the VPWR pin.

All outputs consist of a power MOSFET with an integral substrate diode. During reverse battery condition, current will flow through the load via the substrate diode. Under this circumstance relays may energize and lamps will turn on. If load reverse battery protection is desired, a diode must be placed in series with the load.

Overtemperature Fault

Overtemperature Detect circuits are specifically incorporated for each individual output. The shutdown following an overtemperature condition depends on the control bit set in the Retry/Shutdown Control register. Each independent output shuts down at 155°C to 180°C. When an output shuts down due to an Overtemperature Fault, no other outputs are affected. The MCU recognizes the fault by a logic [1] in the Fault Status bit (bit 23 in the SO Response register). After the 33999 has cooled below the switch point temperature and 10°C hysteresis, the output functions as defined by the retry/shutdown bit 17 in the Global Shutdown/Retry Control register.

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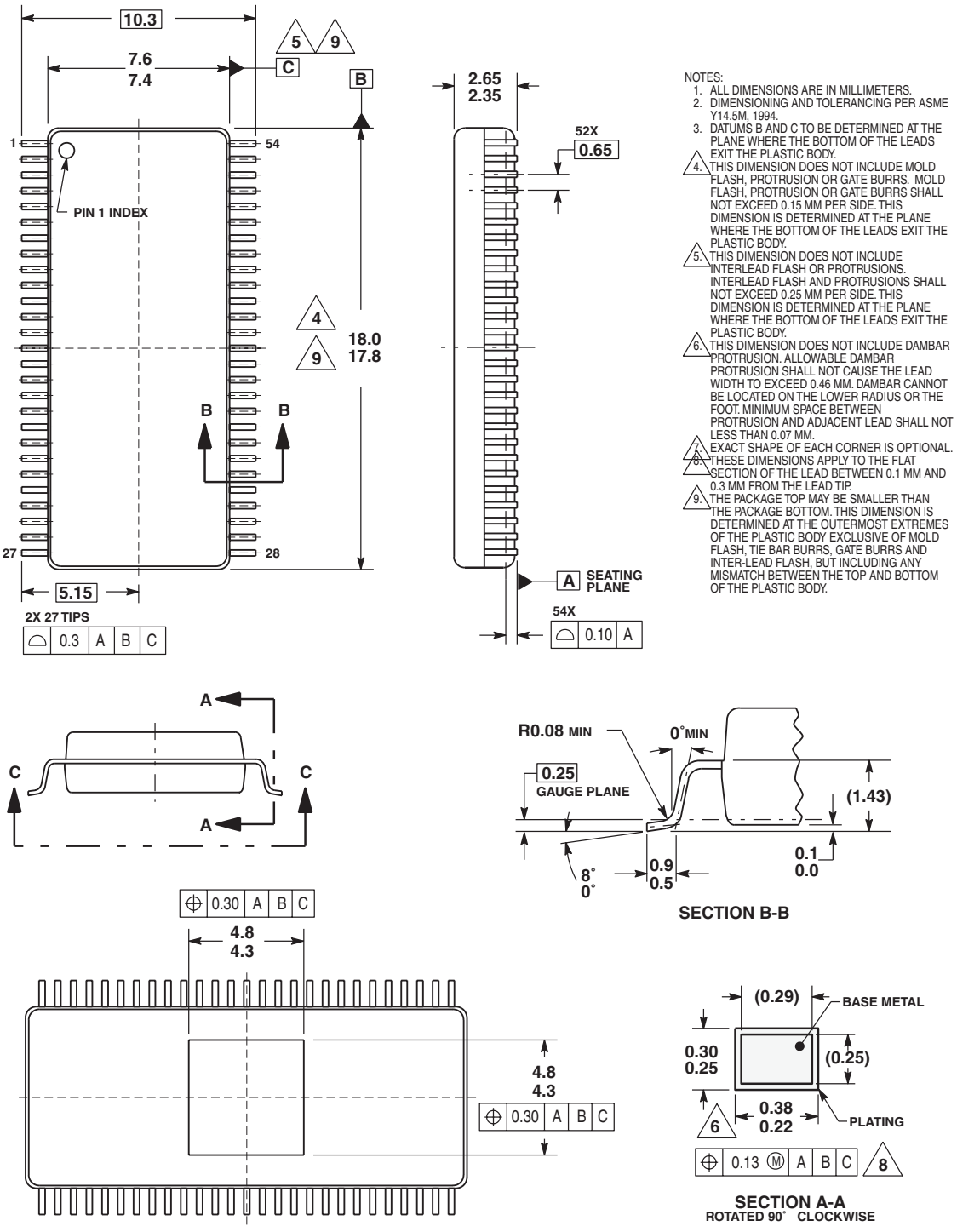

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