

Preliminary Information

Configurable Octal Serial Switch with Open Load Detect Current Disable

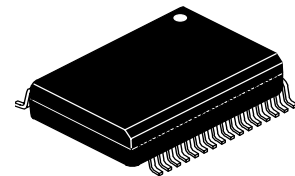
The 33879 device is an 8-output hardware-configurable, high-side/low-side switch with 16-bit serial input control. Two of the outputs may be controlled directly via microprocessor for PWM applications. The 33879 incorporates SMARTMOS technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. The 33879 controls various inductive, incandescent, or LED loads by directly interfacing with a microcontroller. The circuit's innovative monitoring and protection features include very low standby currents, cascade fault reporting, internal +45 V clamp voltage for low-side configuration, -20 V high-side configuration, output-specific diagnostics, and independent overtemperature protection.

Features

- Designed to Operate $5.5\text{ V} \leq V_{PWR} \leq 26.5\text{ V}$
- 16-Bit SPI for Control and Fault Reporting, 3.3 V/5.0 V Compatible
- Outputs Are Current Limited (0.5 A to 1.0 A) to Drive Incandescent Lamps
- Output Voltage Clamp, +45 V (Low Side) and -20 V (High Side) During Inductive Switching
- On/Off Control of Open Load Detect Current (LED Application)
- Internal Reverse Battery Protection on V_{PWR}
- Loss of Ground or Supply Will Not Energize Loads or Damage IC
- Maximum $5.0\text{ }\mu\text{A}$ I_{PWR} Standby Current at 13.0 V V_{PWR}
- $R_{DS(ON)}$ of $1.0\text{ }\Omega$ at 25°C Typical
- Short Circuit Detect and Current Limit with Automatic Retry
- Independent Overtemperature Protection
- Motorola Now Offers Pb-Free Packaging with the Suffix EK

33879

**CONFIGURABLE OCTAL SERIAL
SWITCH WITH OPEN LOAD
DETECT CURRENT DISABLE**

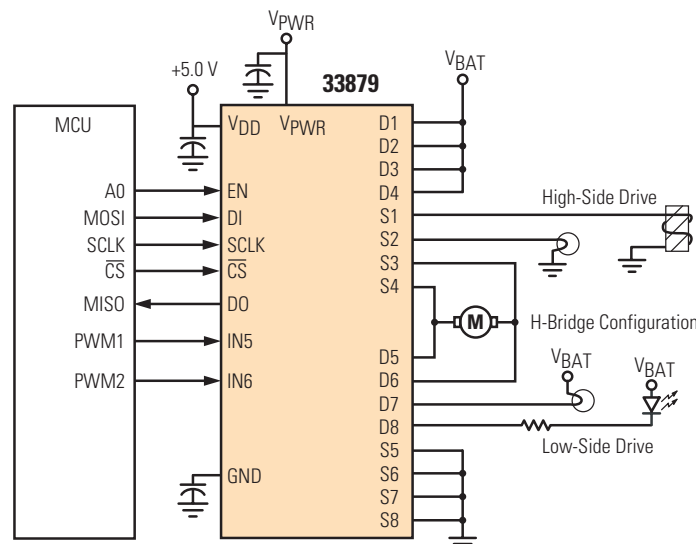


**EK (Pb-FREE) SUFFIX
DWB SUFFIX
CASE 1437-01
32-LEAD SOICW-EP**

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33879DWB/R2	-40°C to 125°C	32 SOICW-EP
PC33879EK/R2		

33879 Simplified Application Diagram



This document contains information on a product under development.
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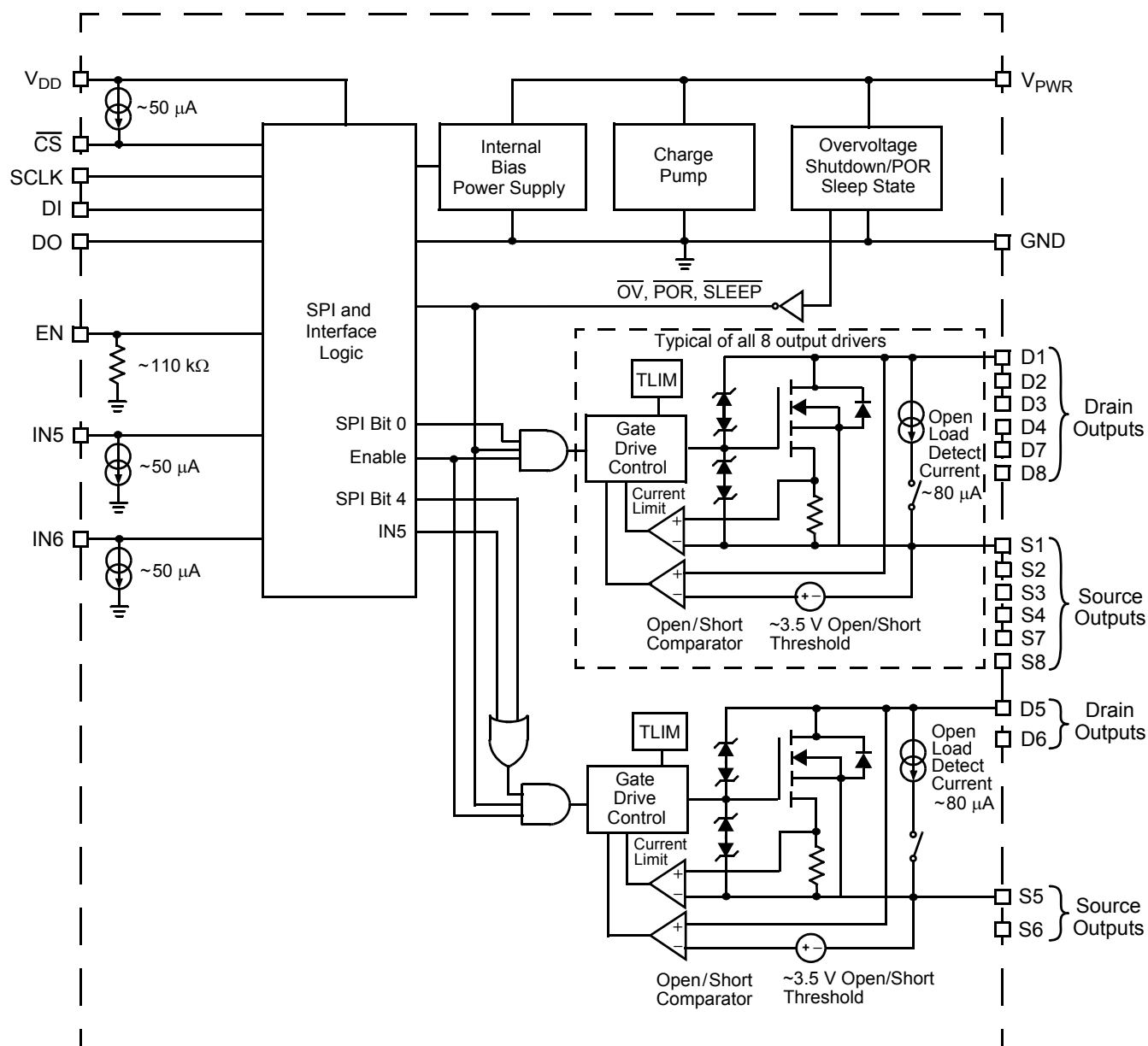
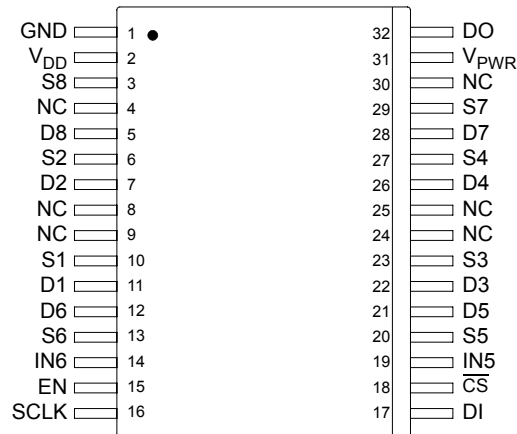


Figure 1. 33879 Simplified Internal Block Diagram



PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1	GND	Ground	Digital ground.
2	V _{DD}	Logic Supply Voltage	Logic supply for SPI interface. With V _{DD} low the device will be in sleep mode.
3	S8	Source Output 8	Output eight MOSFET source pins.
4, 8, 9, 24, 25, 30	NC	Not Connected	No internal connection to this pin.
5	D8	Drain Output 8	Output eight MOSFET drain pin.
6	S2	Source Output 2	Output two MOSFET source pin.
7	D2	Drain Output 2	Output two MOSFET drain pin.
10	S1	Source Output 1	Output one MOSFET source pin.
11	D1	Drain Output 1	Output one MOSFET drain pin.
12	D6	Drain Output 6	Output six MOSFET drain pin.
13	S6	Source Output 6	Output six MOSFET source pin.
14	IN6	Command Input 6	PWM direct control input pin for output 6. IN6 is "OR" with SPI bit.
15	EN	Enable Input	IC Enable. Active high. With EN low, the device is in sleep mode.
16	SCLK	SPI Clock	SPI control clock input pin.
17	DI	Serial Data Input	SPI control data input pin from MCU to the 33879. Logic [1] activates output.
18	$\overline{\text{CS}}$	SPI Chip Select	SPI control chip select input pin from MCU to the 33879. Logic [0] allows data to be transferred in.
19	IN5	Command Input 5	PWM direct control input pin for output 5. IN5 is "OR" with SPI bit.
20	S5	Source Output 5	Output five MOSFET source pin.
21	D5	Drain Output 5	Output five MOSFET drain pin.
22	D3	Drain Output 3	Output three MOSFET drain pin.
23	S3	Source Output 3	Output three MOSFET source pin.
26	D4	Drain Output 4	Output four MOSFET drain pin.
27	S4	Source Output 4	Output four MOSFET source pin.
28	D7	Drain Output 7	Output seven MOSFET drain pin.
29	S7	Source Output 7	Output seven MOSFET source pin.
31	V _{PWR}	Battery Input	Power supply pin to the 33879. V _{PWR} has internal reverse battery protection.
32	DO	Serial Data Output	SPI control data output pin from the 33879 to the MCU. DO=0 no fault, DO=1 specific output has fault.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
V _{DD} Supply Voltage (Note 1)	V _{DD}	-0.3 to 7.0	V _{DC}
$\overline{\text{CS}}$, DI, DO, SCLK, IN5, IN6, and EN (Note 1)	–	-0.3 to 7.0	V _{DC}
V _{PWR} Supply Voltage (Note 1)	V _{PWR}	-16 to 40	V _{DC}
Output Clamp Energy (Note 2)	E _{CLAMP}	50	mJ
ESD Voltage Human Body Model (Note 3) Machine Model (Note 4)	V _{ESD1} V _{ESD2}	±2000 ±200	V
Storage Temperature	T _{STG}	-55 to 150	°C
Operating Case Temperature	T _C	-40 to 125	°C
Operating Junction Temperature	T _J	-40 to 150	°C
Maximum Junction Temperature	T _J	-40 to 150	°C
Power Dissipation (Note 5)	P _D	1.7	W
Thermal Resistance Junction-to-Ambient Between the Die and the Exposed Die Pad	R _{θJA} R _{θJC}	71 1.2	°C/W

Notes

- Exceeding these limits may cause malfunction or permanent damage to the device.
- Maximum output clamp energy capability at 150°C junction temperature using single non-repetitive pulse method with I = 350 mA.
- ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
- ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
- Maximum power dissipation at T_A = 25°C with no heatsink used.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $5.5\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 13\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range Fully Operational	$V_{PWR(fo)}$	5.5	–	26.5	V
Supply Current	$I_{PWR(on)}$	–	14	24	mA
Sleep State Supply Current V_{DD} or $EN \leq 0.8\text{ V}$, $V_{PWR} = 13\text{ V}$	$I_{PWR(ss)}$	–	2.0	5.0	μA
Sleep State Supply Current $EN \leq 0.8\text{ V}$, $V_{DD} = 5.5\text{ V}$	$I_{VDD(ss)}$	–	2.0	5.0	μA
V_{PWR} Overvoltage Shutdown Threshold Voltage	$V_{PWR(OV)}$	27	28.5	32	V
V_{PWR} Overvoltage Shutdown Hysteresis Voltage	$V_{PWR(OV-hys)}$	0.2	1.5	2.5	V
V_{PWR} Undervoltage Shutdown Threshold Voltage	$V_{PWR(UV)}$	3.0	4.0	5.0	V
V_{PWR} Undervoltage Shutdown Hysteresis Voltage	$V_{PWR(UV-hys)}$	300	500	700	mV
Logic Supply Voltage	V_{DD}	3.1	–	5.5	V
Logic Supply Current	I_{DD}	250	400	700	μA
Logic Supply Sleep State Threshold Voltage	$V_{DD(SS)}$	0.8	2.5	3.0	V
Logic Supply Sleep State Hysteresis (Note 6)	$V_{DD(SS-hys)}$	0.3	–	1.5	V

Notes

6. This parameter is guaranteed by design but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions of $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $5.5\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$ unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 13\text{ V}$, $T_A = 25^\circ\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT					
Drain-to-Source ON Resistance $I_{OUT} = 0.350\text{ A}$, $T_J = 125^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ $I_{OUT} = 0.350\text{ A}$, $T_J = 25^\circ\text{C}$, $V_{PWR} = 13\text{ V}$ $I_{OUT} = 0.350\text{ A}$, $T_J = -40^\circ\text{C}$, $V_{PWR} = 13\text{ V}$	$R_{DS(ON)}$	–	– 1.0 –	1.4 – –	Ω
Output Self Limiting Current High-Side and Low-Side Configurations	$I_{OUT(LIM)}$	0.5	–	1.0	A
Output Fault Detection Voltage Threshold (Note 7) Outputs Programmed OFF	$V_{OUT(flt-th)}$	2.5	3.5	4.2	V
Output Fault Detection Current @ Threshold, High-Side Configuration Outputs Programmed OFF	$I_{OUT(flt-th)}$	35	55	70	μA
Output Fault Detection Current @ Threshold, Low-Side Configuration Outputs Programmed OFF	$I_{OUT(flt-th)}$	20	30	50	μA
Output OFF Open Load Detection Current, High-Side Configuration $V_{Drain} = 16\text{ V}$, $V_{Source} = 0\text{ V}$, Outputs Programmed OFF	I_{OCO}	65	100	160	μA
Output OFF Open Load Detection Current, Low-Side Configuration $V_{Drain} = 16\text{ V}$, $V_{Source} = 0\text{ V}$, Outputs Programmed OFF	I_{OCO}	40	75	135	μA
Output Clamp Voltage Low-Side Drive $I_D = 10\text{ mA}$	$V_{OC(LSD)}$	40	45	55	V
Output Clamp Voltage High-Side Drive $I_S = -10\text{ mA}$	$V_{OC(HSD)}$	-15	-20	-25	V
Output Leakage Current High-Side and Low-Side Configurations $V_{DD} = 0\text{ V}$, $V_{Drain} = 16\text{ V}$, $V_{Source} = 0\text{ V}$	$I_{OUT(LKG)}$	–	–	7.0	μA
Output Leakage Current Low-Side Configuration $V_{DD} = 5.0\text{ V}$, $V_{Drain} = 16\text{ V}$, $V_{Source} = 0\text{ V}$, Open Load Detection Current Disabled	$I_{OUT(LKG)}$	–	–	5	μA
Output Leakage Current High-Side Configuration $V_{DD} = 5.0\text{ V}$, $V_{Drain} = 16\text{ V}$, $V_{Source} = 0\text{ V}$, Open Load Detection Current Disabled	$I_{OUT(LKG)}$	–	–	20	μA
Overtemperature Shutdown (Note 8)	T_{LIM}	155	–	185	$^\circ\text{C}$
Overtemperature Shutdown Hysteresis (Note 8)	$T_{LIM(hys)}$	5.0	10	15	$^\circ\text{C}$

Notes

7. Output fault detection thresholds with outputs programmed OFF. Output fault detect thresholds are the same for output open and shorts.
8. This parameter is guaranteed by design but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions of $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $5.5\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, unless otherwise noted. Typical values, where applicable, reflect the parameter's approximate average value with $V_{PWR} = 13\text{ V}$, $T_A = 25^{\circ}\text{C}$

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic High-Voltage Thresholds (Note 9)	V_{IH}	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V
Input Logic Low-Voltage Thresholds (Note 9)	V_{IL}	$\text{GND} - 0.3$	—	$0.2 \times V_{DD}$	V
IN5, IN6, EN Input Logic Current IN5, IN6, EN = 0 V	I_{IN5}, I_{IN6}, I_{EN}	-10	—	10	μA
IN5, IN6 Pull-Down Current 0.8 V to 5.0 V	I_{IN5}, I_{IN6}	30	45	100	μA
EN Pull-Down Current EN = 5.0 V	I_{EN}	30	45	100	μA
SCLK, DI Input, Tri-State DO Output 0 V to 5.0 V	$I_{SCK}, I_{DI}, I_{TriDO}$	-10	—	10	μA
$\overline{\text{CS}}$ Input Current $\overline{\text{CS}} = V_{DD}$	$I_{\overline{\text{CS}}}$	-10	—	10	μA
$\overline{\text{CS}}$ Pull-Up Current $\overline{\text{CS}} = 0\text{ V}$	$I_{\overline{\text{CS}}}$	-30	—	-100	μA
$\overline{\text{CS}}$ Leakage Current to V_{DD} $\overline{\text{CS}} = 5.0\text{ V}$, $V_{DD} = 0\text{ V}$	$I_{\overline{\text{CS}}}(\text{LKG})$	—	—	10	μA
DO High-State Output Voltage $I_{DO-HIGH} = -1.6\text{ mA}$	V_{DOHIGH}	$V_{DD} - 0.4$	—	V_{DD}	V
DO Low-State Output Voltage $I_{DO-LOW} = 1.6\text{ mA}$	V_{DOLOW}	—	—	0.4	V
Input Capacitance on SCLK, DI, Tri-State DO, IN5, IN6, EN (Note 10)	C_{IN}	—	—	20	pF

Notes

9. Upper and lower logic threshold voltage levels apply to DI, $\overline{\text{CS}}$, SCLK, IN5, IN6, and EN.
10. This parameter is guaranteed by design but not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions of $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $5.5\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$ unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 13\text{ V}$, $T_A = 25^\circ\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Units
POWER OUTPUT TIMING					
Output Slew Rate Low-Side Configuration (Note 11) $R_{LOAD} = 620\ \Omega$, $C_L = 200\text{ pF}$	$t_{SR(rise)}$	0.1	0.5	1.0	V/ μs
Output Slew Rate Low-Side Configuration (Note 11) $R_{LOAD} = 620\ \Omega$, $C_L = 200\text{ pF}$	$t_{SR(fall)}$	0.1	0.5	1.0	V/ μs
Output Rise Time High-Side Configuration (Note 11) $R_{LOAD} = 620\ \Omega$, $C_L = 200\text{ pF}$	$t_{SR(rise)}$	0.1	0.3	1.0	V/ μs
Output Fall Time High-Side Configuration (Note 11) $R_{LOAD} = 620\ \Omega$, $C_L = 200\text{ pF}$	$t_{SR(fall)}$	0.1	0.3	1.0	V/ μs
Output Turn ON Delay Time, High-Side and Low-Side Configuration (Note 12)	$t_{DLY(on)}$	1.0	15	50	μs
Output Turn OFF Delay Time, High-Side and Low-Side Configuration (Note 12)	$t_{DLY(off)}$	1.0	30	100	μs
Output Fault Delay Time (Note 13)	t_{FAULT}	100	–	300	μs
Power-ON Reset Delay Delay Time Required from Rising Edge of EN and V_{DD} to SPI Active	t_{POR}	100	–	–	μs
Low-State Duration on V_{DD} or EN for Reset V_{DD} or EN $\leq 0.2\text{ V}$	t_{RESET}	100	–	–	μs

Notes

11. Output slew rate respectively measured across a $620\ \Omega$ resistive load at 10 to 90 percent and 90 to 10 percent voltage points. C_L Capacitor is connected from Drain or Source output to Ground.
12. Output turn ON and OFF delay time measured from 50 percent rising edge of \overline{CS} to the beginning of the 10 and 90 percent transition points.
13. Duration of fault before fault bit is set. Duration between access times must be greater than $300\ \mu\text{s}$ to read faults.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions of $3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $5.5\text{ V} \leq V_{PWR} \leq 18\text{ V}$, $-40^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$ unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with $V_{PWR} = 13\text{ V}$, $T_A = 25^{\circ}\text{C}$.

Characteristic	Symbol	Min	Typ	Max	Units
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DIGITAL INTERFACE TIMING (Note 14)

Recommended Frequency of SPI Operation (Note 14)	f_{SPI}	–	4.0	–	MHz
Falling Edge of \overline{CS} to Rising Edge of SCLK (Required Setup Time)	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of \overline{CS} (Required Setup Time)	t_{LAG}	50	–	–	ns
DI to Falling Edge of SCLK (Required Setup Time)	$t_{DI(su)}$	16	–	–	ns
Falling Edge of SCLK to DI (Required Hold Time)	$t_{DI(HOLD)}$	20	–	–	ns
DI, \overline{CS} , SCLK Signal Rise Time (Note 15)	$t_{r(DI)}$	–	5.0	–	ns
DI, \overline{CS} , SCLK Signal Fall Time (Note 15)	$t_{f(DI)}$	–	5.0	–	ns
Time from Falling Edge of \overline{CS} to DO Low Impedance (Note 16)	$t_{DO(EN)}$	–	–	55	ns
Time from Rising Edge of \overline{CS} to DO High Impedance (Note 17)	$t_{DO(DIS)}$	–	–	55	ns
Time from Rising Edge of SCLK to DO Data Valid (Note 18)	t_{VALID}	–	25	55	ns

Notes

14. This parameter is guaranteed by design. Production test equipment uses 4.16 MHz, 5.5V/3.1V SPI interface.
15. Rise and Fall time of incoming DI, \overline{CS} , and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
16. Time required for output status data to be available for use at DO pin.
17. Time required for output status data to be terminated at DO pin.
18. Time required to obtain valid data out from DO following the rise of SCLK.

Timing Diagrams

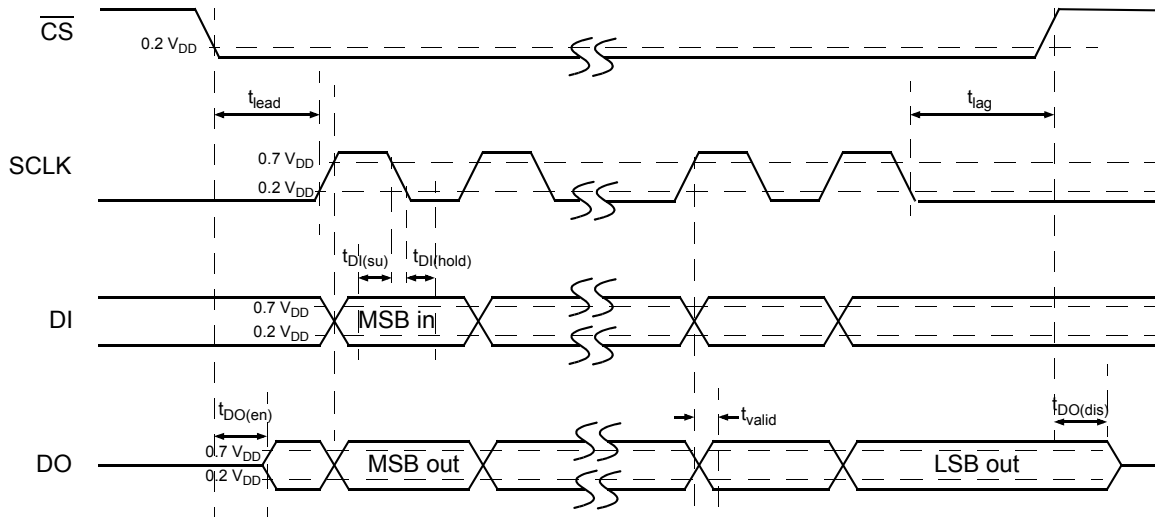
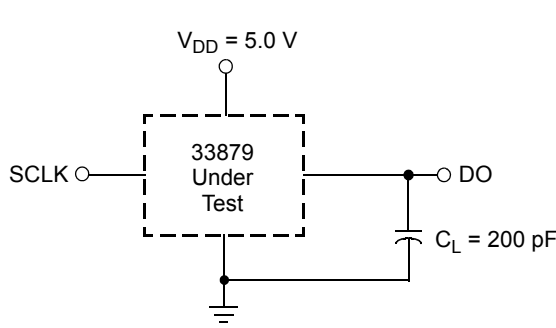


Figure 2. SPI Timing Diagram



NOTE: C_L represents the total capacitance of the test fixture and probe.

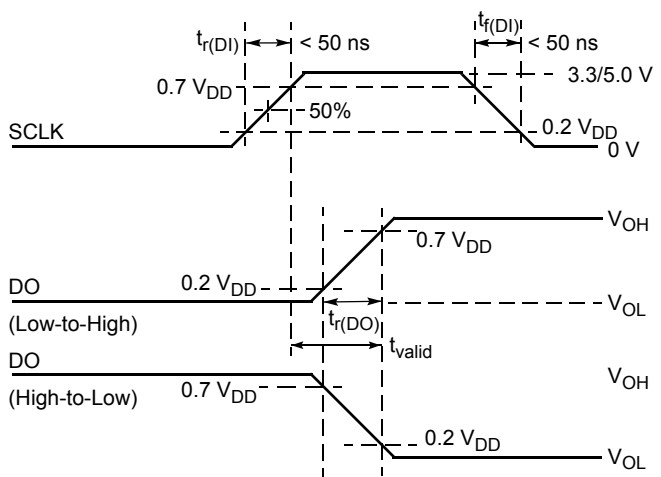


Figure 4. Valid Data Delay Time and Valid Time Waveforms

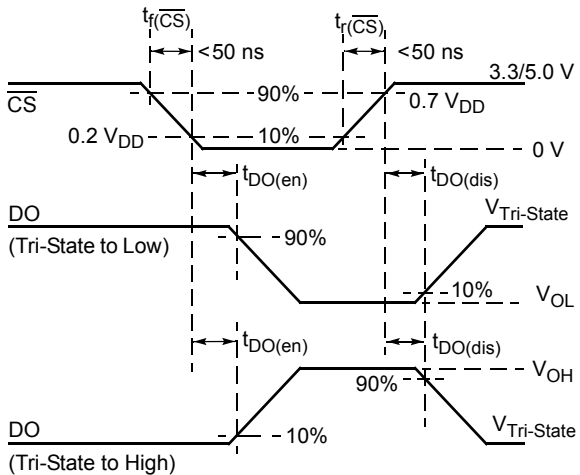


Figure 5. Enable and Disable Time Waveforms

Typical Electrical Characteristics

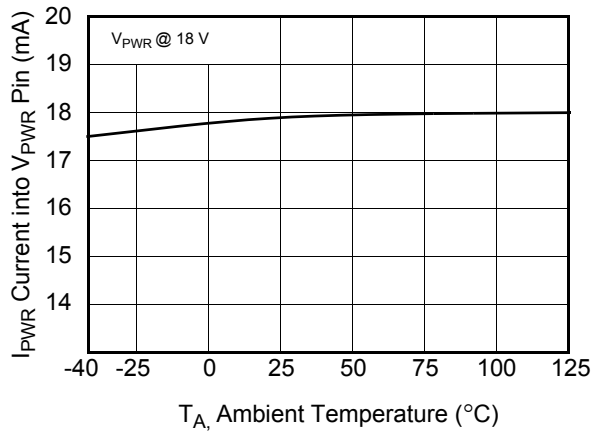


Figure 6. I_{PWR} vs. Temperature

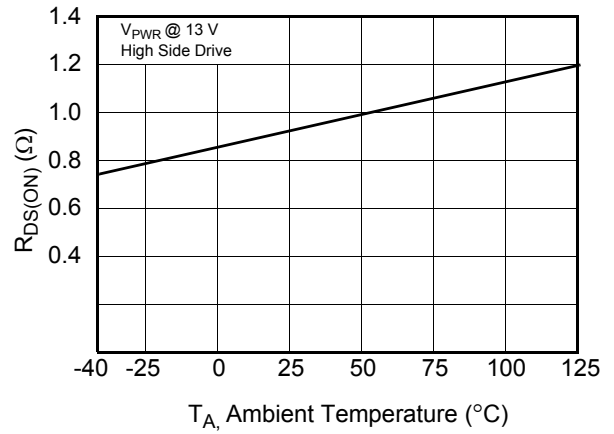


Figure 9. $R_{DS(ON)}$ vs. Temperature at 350 mA

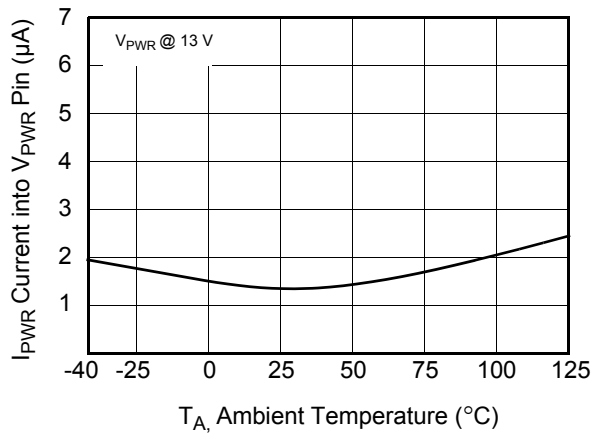


Figure 7. Sleep State I_{PWR} vs. Temperature

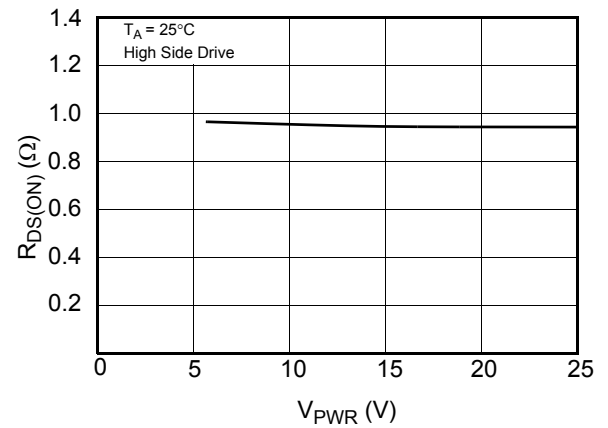


Figure 10. $R_{DS(ON)}$ vs. V_{PWR} at 350 mA

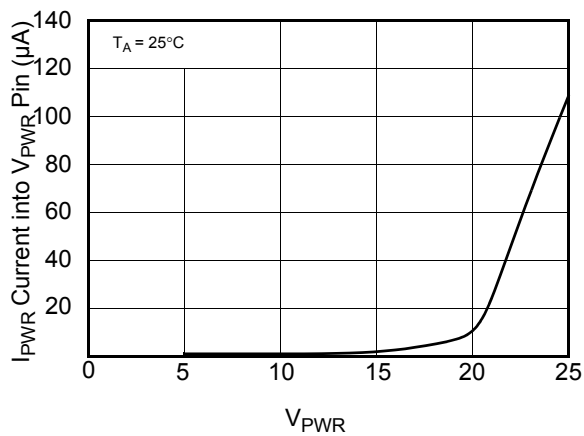


Figure 8. Sleep State I_{PWR} vs. V_{PWR}

Typical Electrical Characteristics (continued)

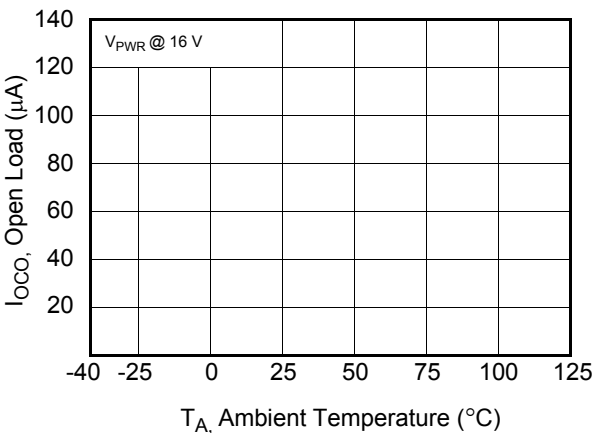


Figure 11. Open Load Detection Current at Threshold

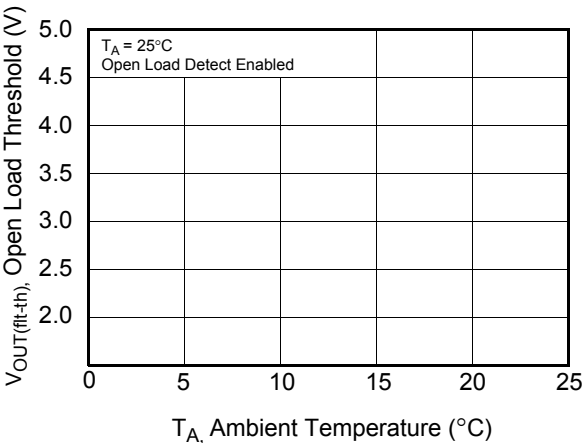


Figure 12. Open Load Detection Threshold vs. Temperature

SYSTEM/APPLICATION INFORMATION

FUNCTIONAL PIN DESCRIPTION

$\overline{\text{CS}}$ Pin

The system MCU selects the 33879 with which to communicate through the use of the chip select $\overline{\text{CS}}$ pin. Logic low on $\overline{\text{CS}}$ enables the data output (DO) driver and allows data to be transferred from the MCU to the 33879 and vice versa. Data clocked into the 33879 is acted upon on the rising edge of $\overline{\text{CS}}$.

To avoid any spurious data, it is essential the high-to-low transition of the $\overline{\text{CS}}$ signal occur only when SPI clock (SCLK) is in a logic low state.

SCLK Pin

The SCLK pin clocks the internal shift registers of the 33879. The serial data input (DI) pin is latched into the input shift register on the falling edge of the SCLK. The serial data output (DO) pin shifts data out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to ensure validity of data. It is essential that the SCLK pin be in a logic low state when the $\overline{\text{CS}}$ pin makes any transition. For this reason, it is recommended the SCLK pin is commanded to a logic low state when the device is not accessed ($\overline{\text{CS}}$ in logic high state). With $\overline{\text{CS}}$ in a logic high state, signals present on SCLK and DI are ignored and the DO output is tri-state.

DI Pin

The DI pin is used for serial instruction data input. DI information is latched into the input register on the falling edge of SCLK. A logic high state present on DI will program a specific output *on*. The specific output will turn on with the rising edge of the $\overline{\text{CS}}$ signal. Conversely, a logic low state present on the DI pin will program the output *off*. The specific output will turn *off* with the rising edge of the $\overline{\text{CS}}$ signal. To program the eight outputs and Open Load Detection Current *on* or *off*, send the DI data beginning with the Open Load Detection Current bits, followed by output eight, output seven, and so on to output one. For each falling edge of the SCLK while $\overline{\text{CS}}$ is logic low, a data bit instruction (*on* or *off*) is loaded into the shift register per the data bit DI state. Sixteen bits of entered information is required to fill the input shift register.

DO Pin

The DO pin is the output from the shift register. The DO pin remains tri-state until the $\overline{\text{CS}}$ pin is in a logic low state. All faults on the 33879 device are reported as logic [1] through the DO data pin. Regardless of the configuration of the driver, open loads and shorted loads are reported as logic [1]. Conversely, normal operating outputs with non-faulted loads are reported as logic [0]. Outputs programmed with Open Load Detection Current disabled will report logic [0] in the off state. The first eight positive transitions of SCLK will report logic [0] followed by the status of the eight output drivers. The DI/DO shifting of data

follows a first-in, first-out protocol with both input and output words transferring the most significant bit (MSB) first.

EN Pin

The EN pin on the 33879 enables the device. With the EN pin high, output drivers may be activated and open/short fault detection performed and reported. With the EN pin low, all outputs become inactive, Open Load Detection Current is disabled, and the device enters sleep mode. The 33879 will perform Power-ON Reset on rising edge of the enable signal.

IN5 and IN6 Pins

The IN5 and IN6 command inputs allow outputs five and six to be used in PWM applications. The IN5 and IN6 pins are OR-ed with the Serial Peripheral Interface (SPI) command input bits. For SPI control of outputs five and six, the IN5 and IN6 pins should be grounded or held low by the microprocessor. When using IN5 or IN6 to PWM the output, the control SPI bit must be logic [0]. Maximum PWM frequency for each output is 2.0 kHz.

V_{DD} Pin

The V_{DD} input pin is used to determine logic levels on the microprocessor interface (SPI) pins. Current from V_{DD} is used to drive DO output and the pull-up current for $\overline{\text{CS}}$. V_{DD} must be applied for normal mode operation. The 33879 device will perform Power-ON Reset with the application of V_{DD} .

V_{PWR} Pin

The V_{PWR} pin is battery input and Power-ON Reset to the 33879 IC. The V_{PWR} pin has internal reverse battery protection. All internal logic current is provided from the V_{PWR} pin. The 33879 will perform Power-ON Reset with the application of V_{PWR} .

D1–D8 Pins

The D1 to D8 pins are the open-drain outputs of the 33879. For high-side drive configurations, the drain pins are connected to battery supply. In low-side drive configurations, the drain pins are connected to the low side of the load. All outputs may be configured individually as desired. When configured as low-side drive, the 33879 limits the positive inductive transient to 45 V.

S1–S8 Pins

The S1 to S8 pins are the source outputs of the 33879. For high-side drive configurations, the source pins are connected directly to the load. In low-side drive configurations, the source is connected to ground. All outputs may be configured individually as desired. When high-side drive is used, the 33879 will limit the negative inductive transient to negative 20 V.

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MCU INTERFACE DESCRIPTION

Introduction

The 33879 is an 8-output hardware-configurable power switch with 16-bit serial control. A simplified block diagram of the 33879 is shown in [Figure 1](#) on page 2.

The 33879 device uses high-efficiency up-drain power DMOS output transistors exhibiting low drain-to-source ON resistance ($R_{DS(ON)} = 1.0 \Omega$ at 25°C typical) and dense CMOS control logic. All outputs have independent voltage clamps to provide fast inductive turn-off and transient protection.

In operation, the 33879 functions as an 8-output serial switch serving as a MCU bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. This device directly interfaces to an MCU using a SPI for control and diagnostic readout. [Figure 13](#) illustrates the basic SPI configuration between an MCU and one 33879.

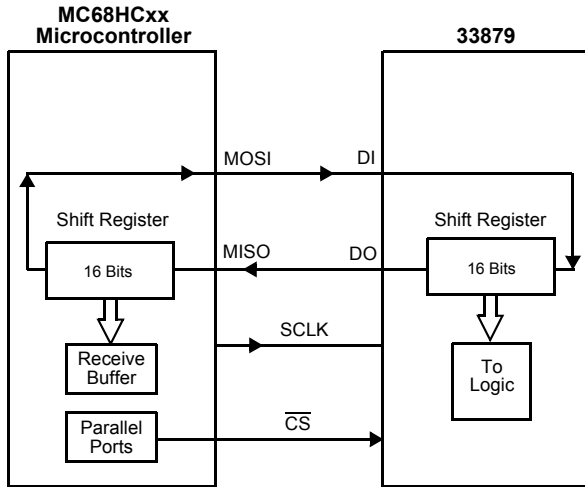


Figure 13. SPI Interface with Microcontroller

All inputs are compatible with 5.0 V and 3.3 V CMOS logic levels and incorporate positive logic. When a SPI bit is programmed to a logic [0], the corresponding output will be OFF. Conversely, when a SPI bit is programmed to logic [1] the output being controlled will be ON. Diagnostics are treated in a similar manner. Outputs with a fault will feed back (via DO) a logic [1] to the microcontroller, while normal operating outputs will provide a logic [0].

[Figure 14](#) illustrates the daisy chain configuration using the 33879. Data from the MCU is clocked daisy chain through each device while the \overline{CS} bit is commanded low by the MCU. During each clock cycle, output status from the daisy chain is transferred to the MCU via the Master In Slave Out (MISO) line. On rising edge of \overline{CS} , command data stored in the input register is then transferred to the output driver.

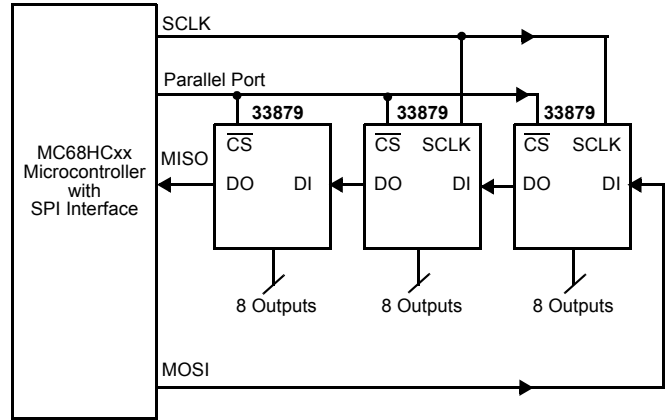


Figure 14. 33879 SPI System Daisy Chain

Multiple 33879 devices can be controlled in a parallel input fashion using the SPI. [Figure 15](#) illustrates the control of 24 loads using three dedicated parallel MCU ports for chip select.

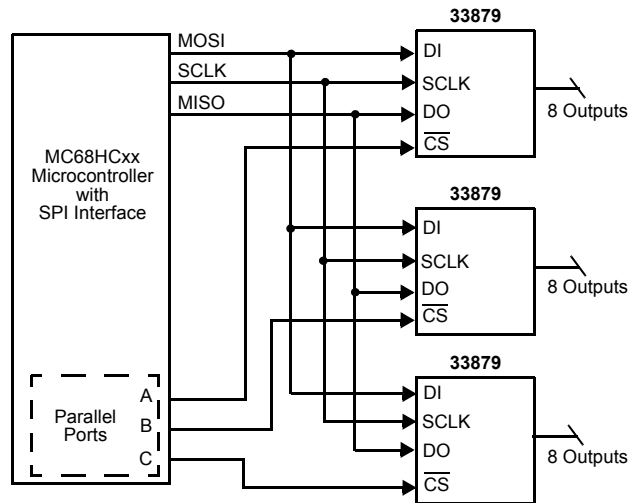


Figure 15. Parallel Input SPI Control

SPI DEFINITION

On each SPI communication, a 16-bit command word is sent to the 33879 and a 16-bit status word is received from the 33879. The MSB is sent and received first. As [Table 1](#) shows, the Command Register defines the position and operation the

33879 will perform on rising edge of \overline{CS} . The Fault Register, shown in [Table 2](#), defines the previous state status of the output driver. [Table 3](#) identifies the type of fault and the method by which the fault is communicated to the microprocessor.

Table 1. Command Register Definition

MSB								LSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ON/OFF Open Load Detect 8	ON/OFF Open Load Detect 7	ON/OFF Open Load Detect 6	ON/OFF Open Load Detect 5	ON/OFF Open Load Detect 4	ON/OFF Open Load Detect 3	ON/OFF Open Load Detect 2	ON/OFF Open Load Detect 1	ON/OFF OUT 8	ON/OFF OUT 7	ON/OFF OUT 6	ON/OFF OUT 5	ON/OFF OUT 4	ON/OFF OUT 3	ON/OFF OUT 2	ON/OFF OUT 1

0 = Bits 0 to 7, Output commanded OFF.

1 = Bits 0 to 7, Output commanded ON.

0 = Bits 8 to 15, Open Load Detection Current OFF.

1 = Bits 8 to 15 Open Load Detection Current ON.

Table 2. Fault Register Definition

MSB								LSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0	OUT 8 Status	OUT 7 Status	OUT 6 Status	OUT 5 Status	OUT 4 Status	OUT 3 Status	OUT 2 Status	OUT 1 Status

0 = Bits 0 to 7, No Fault at Output.

Bits 8 to 15 will always return "0".

1 = Bits 0 to 7, Output Short-to-Battery, Short-to-GND, Open Load, or T_{LIM} .

Table 3. Fault Operation

Serial Output (DO) Pin Reports

Overtemperature	Fault reported by serial output (DO) pin.
Overcurrent	DO pin reports short to battery/supply or overcurrent condition.
Output ON Open Load Fault	Not reported.
Output OFF Open Load Fault	DO pin reports output OFF open load condition only with Open Load Detection Current enabled. DO pin will report "0" for Output OFF Open Load Fault with Open Load Detection Current disabled.

Device Shutdowns

Overvoltage	Total device shutdown at $V_{PWR} = 27\text{ V} - 30\text{ V}$. Resumes normal operation with proper voltage. All outputs assuming the previous state upon recovery from overvoltage.
Overtemperature	Only the output experiencing an overtemperature shuts down. Output assumes previous state upon recovery from overtemperature.

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DEVICE OPERATION

Power Supply

The 33879 device has been designed with ultra-low sleep mode currents. The device may enter sleep mode via the EN pin or the V_{DD} pin. In the sleep mode (EN or $V_{DD} \leq 0.8$ V), the current consumed by the V_{PWR} pin is less than 5.0 μ A.

Placing the 33879 in sleep mode resets the internal registers to the Power-ON Reset state. The reset state is defined as all outputs off and Open Load Detection Current disabled.

To place the 33879 in the sleep mode, either command all outputs off and apply logic low to the EN input pin or remove power from the V_{DD} supply pin. Prior to removing V_{DD} from the device, it is recommended that all control inputs from the MCU be low.

Paralleling of Outputs

Using MOSFETs as an output switch conveniently allows the paralleling of outputs for increased current capability. $R_{DS(ON)}$ of MOSFETs have an inherent positive temperature coefficient that provides balanced current sharing between outputs without destructive operation. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(ON)}$ while the output OFF Open Load Detection Currents and the output current limits increase correspondingly. Paralleling outputs from two or more different IC devices is possible but not recommended.

Fault Logic Operation

Fault logic of the 33879 device has been greatly simplified over other devices using SPI communications. As command word one is being written into the shift register, a fault status word is being simultaneously written out and received by the MCU. Regardless of the configuration, with no outputs faulted and Open Load Detection Current enabled, all status bits being received by the MCU will be zero. When outputs are faulted (off state open circuit or on state short circuit/overtemperature), the status bits being received by the MCU will be one. The distinction between open circuit fault and short/overtemperature is completed via the command word. For example, when a zero command bit is sent and a one fault is received in the following word, the fault is open/short-to-battery for high-side drive or open/short-to-ground for low-side drive. In the same manner, when a one command bit is sent and a one fault is received in the following word, the fault is a short-to-ground/overtemperature for high-side drive or short-to-battery/overtemperature for low-side drive. The timing between two write words must be greater than 300 μ s to allow adequate time to sense and report the proper fault status.

SPI Integrity Check

Checking the integrity of the SPI communication with the initial power-up of the V_{DD} and EN pins is recommended. After initial system start-up or reset, the MCU will write one 32-bit pattern to the 33879. The first 16 bits read by the MCU will be 8 logic [0]s followed by the fault status of the outputs. The second 16 bits will be the same bit pattern sent by the MCU. By the MCU receiving the same bit pattern it sent, bus integrity is confirmed. Please note the second 16-bit pattern the MCU sends to the device is the command word and will be transferred to the outputs with rising edge of \overline{CS} .

Important A SCLK pulse count strategy has been implemented to ensure integrity of SPI communications. SPI messages consisting of 16 SCLK pulses and multiples of 8 clock pulses thereafter will be acknowledged. SPI messages consisting of other than 16 + multiples of 8 SCLK pulses will be ignored by the device.

Overtemperature Fault

Overtemperature detection and shutdown circuits are specifically incorporated for each individual output. The shutdown following an overtemperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155°C to 185°C. When an output shuts down owing to an overtemperature fault, no other outputs are affected. The MCU recognizes the fault by a one in the fault status register. After the 33879 device has cooled below the switch point temperature and 15°C hysteresis, the output will activate unless told otherwise by the MCU via SPI to shut down.

Overvoltage Fault

An overvoltage condition on the V_{PWR} pin will cause the device to shut down all outputs until the overvoltage condition is removed. When the overvoltage condition is removed, the outputs will resume their previous state. This device does not detect an overvoltage on the V_{DD} pin. The overvoltage threshold on the V_{PWR} pin is specified as 27 V to 30 V, with 1.0 V typical hysteresis. A V_{PWR} overvoltage detection is *global*, causing all outputs to be turned OFF.

Output OFF Open Load Fault

An output OFF open load fault is the detection and reporting of an *open* load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

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An output OFF open load fault is indicated when the drain-to-source voltage is less than the output threshold voltage ($V_{OUT(FLT-TH)}$) of 2.5 V to 4.0 V. Hence, the 33879 will declare the load *open* in the OFF state when the output drain-to-source voltage is less than $V_{OUT(FLT-TH)}$.

This device has an internal 80 μ A current source connected from drain to source of the output MOSFET. The current source may be programmed on or off via SPI. The Power-ON Reset state for the current source is "off" and must be enabled via SPI. To achieve low sleep mode quiescent currents, the Open Load Detection Current source of each driver is switched off when V_{DD} or EN is removed.

During output switching, especially with capacitive loads, a false output OFF open load fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 μ s to 300 μ s is incorporated. A false fault reporting is a function of the load impedance, $R_{DS(ON)}$, C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR} . The rising edge of \overline{CS} triggers the built-in fault delay timer. The timer will time out before the fault comparator is enabled and the fault is detected. Once the condition causing the open load fault is removed, the device will resume normal operation. The open load fault, however, will be latched in the output DO register for the MCU to read.

Shorted Load Fault

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply, or an output experiencing a current greater than the current limit.

There are two safety circuits progressively in operation during load short conditions that provide system protection:

1. The device's output current is monitored in an analog fashion using SENSEFET approach and current limited.
2. The device's output thermal limit is sensed and when attained causes only the specific faulted output to shut down. The output will remain off until cooled. The device will then reassert the output automatically. The cycle will continue until fault is removed or the command bit instructs the output off. Shorted load faults will be reported properly through SPI regardless of Open Load Detection Current enable bits.

Undervoltage Shutdown

An undervoltage condition on V_{DD} or V_{PWR} will result in the shutdown of all outputs. The V_{DD} undervoltage threshold is between 0.8 V and 3.0 V. V_{PWR} undervoltage threshold is between 3.0 V and 5.0 V. When the supplies fall below their respective thresholds, all outputs are turned OFF. As both supplies returns to normal levels, internal logic is reset and the device resumes normal operation.

Output Voltage Clamp

Each output of the 33879 incorporates an internal voltage clamp to provide fast turn-off and transient protection of each output. Each clamp independently limits the drain-to-source voltage to 45 V for low-side drive configurations and -20 V for high-side drive configurations. The total energy clamped (E_J) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (V_{CL}) (see [Figure 16](#)).

Characterization of the output clamps, using a single pulse non-repetitive method at 0.35 A, indicates the maximum energy per output to be 50 mJ at 150°C junction temperature.

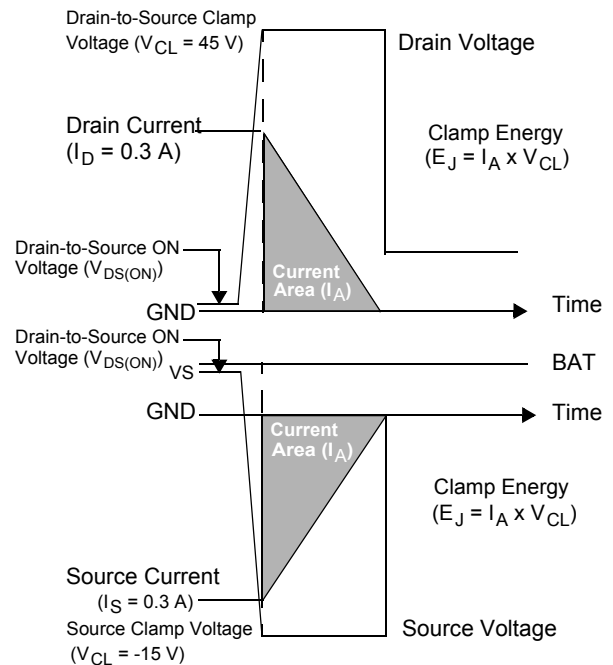


Figure 16. Output Voltage Clamping

SPI Configurations

The SPI configuration on the 33879 device is consistent with other devices in the Octal Serial Switch (OSS) family. This device may be used in serial SPI or parallel SPI with the 33298 and 33291. Different SPI configurations may be provided. For more information, contact Motorola Analog Products Division or local Motorola representative.

Reverse Battery

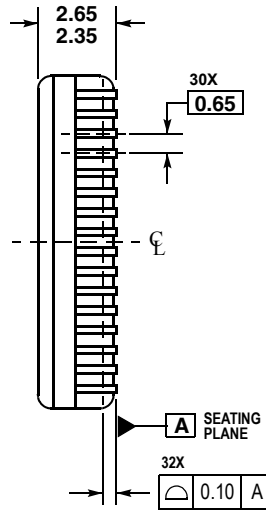
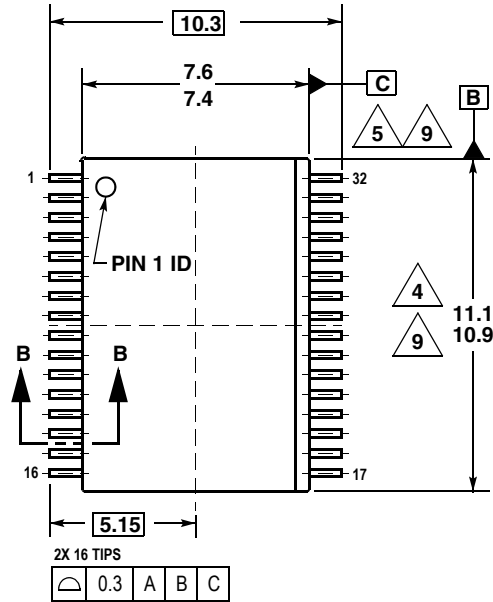
The 33879 has been designed with reverse battery protection on the V_{PWR} pin.

All outputs consist of a power MOSFET with an integral substrate diode. During the reverse battery condition, current will flow through the load via the substrate diode. Under this circumstance, relays may energize and lamps will turn on. Where load reverse battery protection is desired, a reverse battery blocking diode must be placed in series with the load.

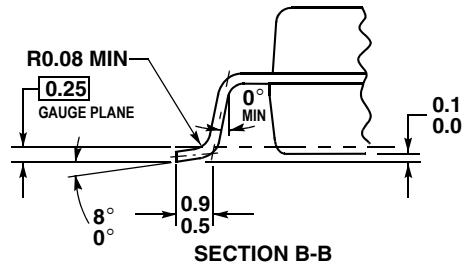
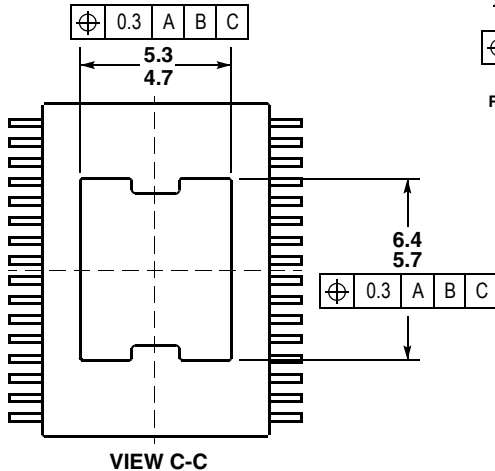
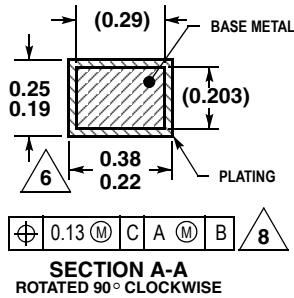
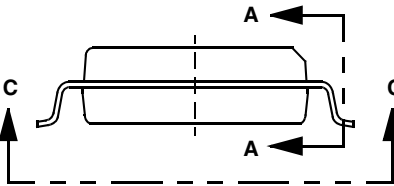
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PACKAGE DIMENSIONS

EK (Pb-FREE) SUFFIX
DWB SUFFIX
 32-LEAD SOIC WIDE BODY EXPOSED PAD
 PLASTIC PACKAGE
 CASE 1437-01
 ISSUE O



- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
 4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
 5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
 6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm PER SIDE. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
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