



## 32K x 32 EEPROM MODULE

PUMA 2E1000-70/90/12/X405

Issue 4.0 : June 1997

### Description

The PUMA 2E1000/X405 is a 1Mbit CMOS High Speed EEPROM organised as 32K x 32. This is available in a 66 pin PGA package which is suitable for thermal ladder applications. Access times are 70ns, 90ns or 120ns. It has a user configurable output width. There is facility for both Byte and Page write operation with the X405 having a Page Write Cycle time of 3ms (Max.). Included is both hardware and software data protection and a data retention time of 10 years.

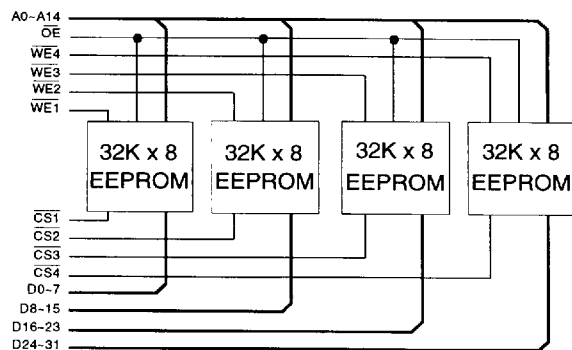
It may be screened in accordance with MIL-STD-883.

1,048,576 bit CMOS High Speed EEPROM

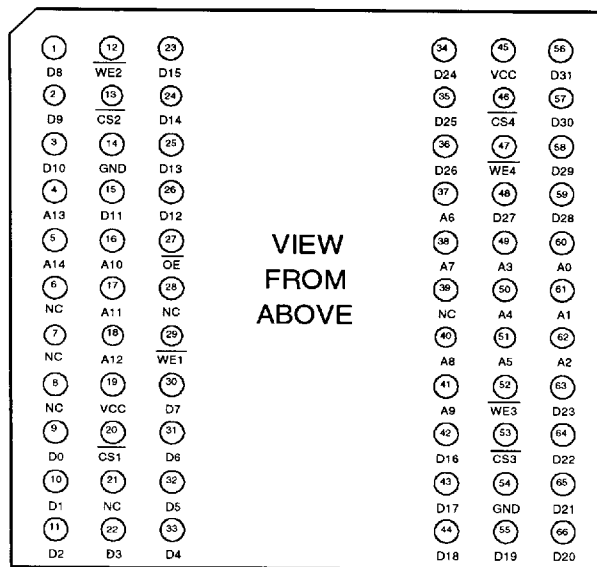
### Features

Very Fast access times of 70/90/120 ns.  
User Configurable as 8 / 16 / 32 bit wide.  
Operating Power 1760 mW (max).  
Standby Power 1320 mW (max).  
Package Suitable for Thermal Ladder Applications.  
Single byte and Page Write operation.  
DATA Polling and Toggle Bit for End of Write Detection.  
Hardware and Software Data Protection.  
Endurance :  $10^4$  Cycles and Data retention : 10 years.  
May be screened in accordance with MIL-STD-883.

### Block Diagram



### Pin Definition



### Pin Functions

**A0-14** Address Inputs  
**CS1-4** Chip Select  
**WE1-4** Write Enable  
**V<sub>CC</sub>** Power (+5V)

**D0-31** Data Inputs/Outputs  
**OE** Output Enable  
**NC** No Connect  
**GND** Ground

6353379 0002719 075

**DC OPERATING CONDITIONS****Absolute Maximum Ratings <sup>(1)</sup>**

Temperature Under Bias	$T_{BIAS}$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-65 to +150	°C
All input voltages (including N.C. pins) with Respect to GND	$V_T$	-0.6 to +6.25	V
All output voltages with respect to GND	$V_{OUT}$	-0.6 to $V_{CC}+0.6$	V
Voltage on $\overline{OE}$ and A9 with Respect to GND	$V_{OEA}$	-0.6 to +13.5	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated below is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	Symbol	min	typ	max	
DC Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input Low Voltage	$V_{IL}$	-0.1	-	0.8	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{CC}+1$	V
Operating Temp Range	$T_A$	0	-	70	°C
	$T_{AI}$	-40	-	85	°C (2E1000I)
	$T_{AM}$	-55	-	125	°C (2E1000M, MB)

**DC Electrical Characteristics ( $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$  to  $+125^\circ\text{C}$ )**

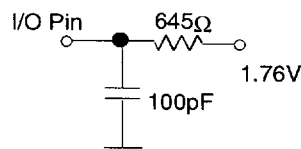
Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current Address, $\overline{OE}$	$I_{LI1}$	$0V \leq V_{IN} \leq V_{CC}+1V$	-	-	40	$\mu\text{A}$
CS1~4, WE1~4	$I_{LI2}$	As above.	-	-	10	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	CS1~4= $V_{IH}$ , $V_{IO}=\text{GND to } V_{CC}$	-	-	40	$\mu\text{A}$
Operating Supply Current	$I_{CC32}$	$f=5\text{MHz}$ , $I_{IO}=0\text{mA}$	-	-	320	$\text{mA}$
Standby Supply Current	$I_{SB1}$	$2.0V \leq \text{CS1} \sim 4 \leq V_{CC}+1V$	-	-	240	$\text{mA}$
-L Version (CMOS) -90, -12	$I_{SB2}$	$-3.0V \leq \text{CS1} \sim 4 \leq V_{CC}+1V$	-	-	1.2	$\text{mA}$
Output Low Voltage	$V_{OL}$	$I_{OL} = 6.0\text{mA}$	-	-	0.45	V
Output High Voltage	$V_{OH}$	$I_{OH} = -4.0\text{mA}$	2.4	-	-	V

**Capacitance ( $V_{CC}=5V\pm10\%$ ,  $T_A=25^\circ\text{C}$ )**

Parameter	Symbol	Test Condition	typ	max	Unit
Input Capacitance:	$C_{IN}$	$V_{IN}=0V$	26	34	$\text{pF}$
I/O Capacitance:	$C_{IO}$	$V_{IO}=0V$ , 8 bit mode	42	58	$\text{pF}$

**AC Test Conditions****Output Test Load**

- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 5ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: 1 TTL gate + 100pF
- \*  $V_{CC}=5V\pm10\%$



**AC READ CHARACTERISTICS****Read Cycle**

Parameter	Symbol	-70		-90		-12		Unit
		min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	-	70	-	90	-	120	ns
Address to Output Delay	$t_{ACC}$	-	70	-	90	-	120	ns
CS1~4 to Output Delay <sup>(1)</sup>	$t_{CS}$	-	70	-	90	-	120	ns
OE to Output Delay <sup>(2)</sup>	$t_{OE}$	0	40	0	45	0	50	ns
CS1~4 or OE to Output Float <sup>(3,4)</sup>	$t_{DF}$	0	40	0	45	0	50	ns
Output Hold from OE, CS1~4 or Address, (whichever occurred first)	$t_{OH}$	0	-	0	-	0	-	ns

- Notes: (1) CS1~4 may be delayed up to  $t_{ACC} - t_{CS}$  after the address transition without impact on  $t_{ACC}$ .  
 (2) OE may be delayed up to  $t_{CS} - t_{OE}$  after the falling edge of CS1~4 without impact on  $t_{CS}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .  
 (3)  $t_{DF}$  is specified from OE or CS1~4 whichever occurs first ( $C_L = 5pF$ ).  
 (4) This parameter is only sampled and is not 100% tested.

**Write Cycle**

Parameter	Symbol	min	typ	max	Unit
Address, OE Set-up Time	$t_{AS}, t_{OES}$	0	-	-	ns
Address Hold Time	$t_{AH}$	50	-	-	ns
Chip Select Set-up Time	$t_{CS}$	0	-	-	ns
Chip Select Hold Time	$t_{CH}$	0	-	-	ns
Write Pulse Width (WE1~4 or CS1~4)	$t_{WP}$	100	-	-	ns
Data Set-up Time	$t_{DS}$	50	-	-	ns
Data, OE Hold Time	$t_{DH}, t_{OEH}$	0	-	-	ns
Time to Data Valid	$t_{DV}$	NR <sup>(1)</sup>	-	-	ns

Note: (1) NR = No Restriction

**Page Mode Write Cycle**

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	$t_{WC}$	-	2	3	ms
Address Set-up Time	$t_{AS}$	0	-	-	ns
Address Hold Time	$t_{AH}$	50	-	-	ns
Data Set-up Time	$t_{DS}$	50	-	-	ns
Data Hold Time	$t_{DH}$	0	-	-	ns
Write Pulse Width	$t_{WP}$	100	-	-	ns
Byte/Word Load Cycle Time	$t_{BLC}$	-	-	150	μs
Write Pulse Width High	$t_{WPH}$	50	-	-	ns

See notes on page 6, Mode Write Waveform.

**DATA Polling Characteristics**

Parameter	Symbol	min	typ	max	Unit
Data Hold Time	$t_{DH}$	0	-	-	ns
OE Hold Time	$t_{OEH}$	0	-	-	ns
OE to Output Delay <sup>(1)</sup>	$t_{OE}$	-	-	-	ns
Write Recovery Time	$t_{WR}$	0	-	-	ns

Note: (1) See AC Read Characteristics.

**Toggle Bit Characteristics (1,2,3,4)**

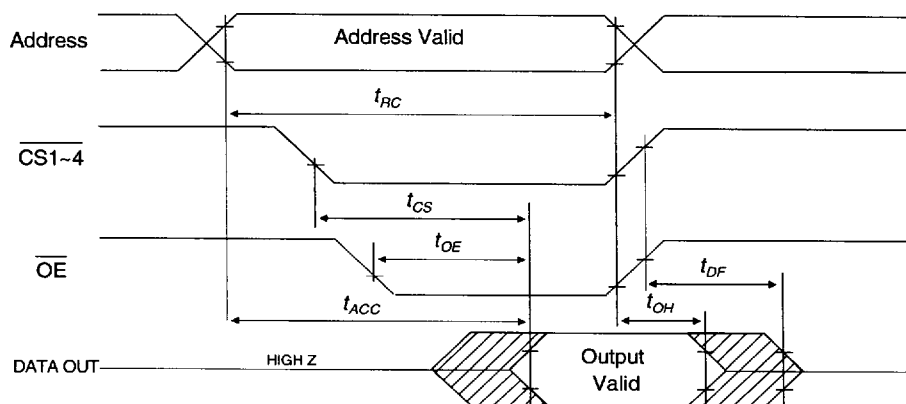
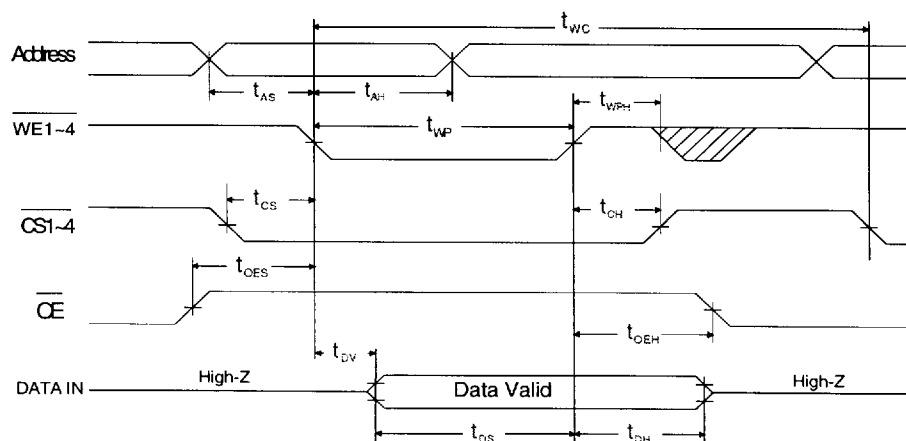
Parameter	Symbol	min	typ	max	Unit
Data Hold Time	$t_{DH}$	10	-	-	ns
$\overline{OE}$ Hold Time	$t_{OE H}$	10	-	-	ns
$\overline{OE}$ to Output Delay <sup>(1)</sup>	$t_{OE}$				ns
$\overline{OE}$ High Pulse	$t_{OEHP}$	150	-	-	ns
Write Recovery Time	$t_{WR}$	0	-	-	ns

Note : (1) See AC Read Characteristics.

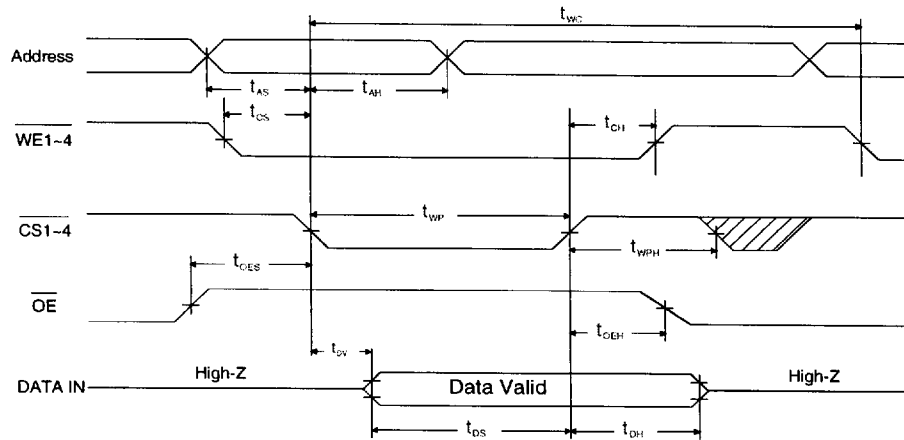
(2) Toggling either  $\overline{OE}$  or  $\overline{CS1-4}$ , or both  $\overline{OE}$  and  $\overline{CS1-4}$  will operate toggle bit.

(3) Beginning and ending state of D6 will vary.

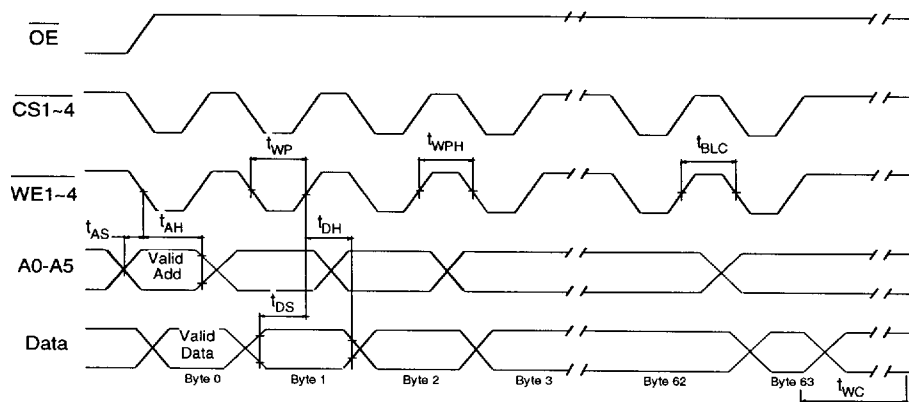
(4) Any address location may be used but the address should not vary.

**Read Cycle Timing Waveform (1,2,3,4)****AC Write Waveform -  $\overline{WE1-4}$  Controlled**

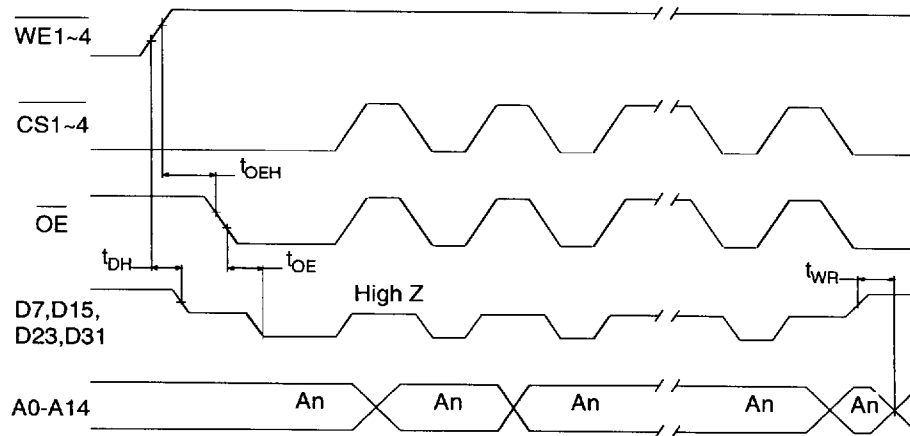
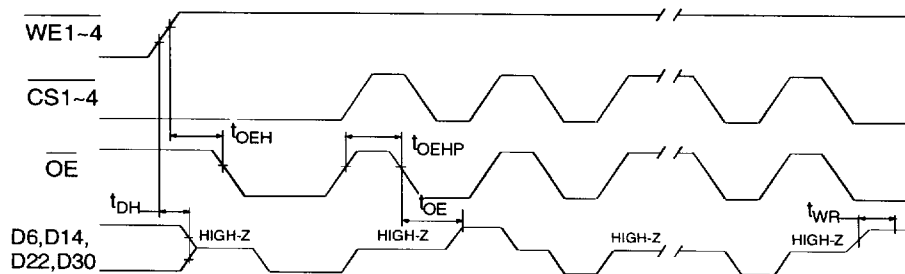
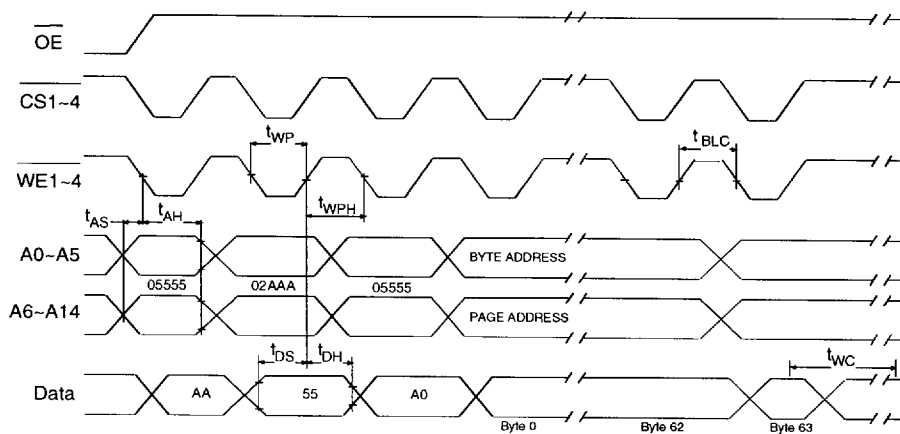
# AC Write Waveform - CS1~4 Controlled



## Page Mode Write Waveform (1,2)

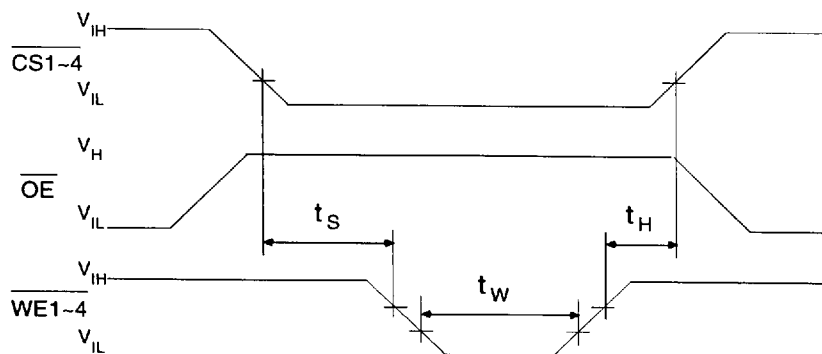


- Note: (1) A6 through A14 must specify the page address during each high to low transition of WE1~4 (or CS1~4).  
 (2) OE must be high only when WE1~4 and CS1~4 are both low.

**DATA Polling Waveform <sup>(1)</sup>****Toggle Bit Waveform <sup>(1,2,3,4)</sup>****Software Protected Write Waveform <sup>(1,2)</sup>**

Notes: (1) A6 through A14 must specify the page address during each high to low transition of WE1~4 (or CS1~4).  
 (2) OE must be high only when WE1~4 and CS1~4 are both low.

# Chip Erase Waveform



$$t_S = t_H = 5\mu s \text{ (min)} \quad t_W = 10 \text{ ms (min)} \quad V_H = 12V \pm 0.5V$$

## Device Operation

Where references are made to byte/word operations, the user will control the memory configuration of 8, 16, or 32 bits wide using CS1~4.

### Read

The PUMA 2E1000 read operations are initiated by both Output Enable and Chip Select(s) LOW, while Write Enable(s) is HIGH. The read operation is terminated by either Chip Select(s) or Output Enable returning HIGH. This dual-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either Output Enable or Chip Select is HIGH.

### Write

Write operations are initiated when both Chip Select(s) and Write Enable(s) are LOW and Output Enable is HIGH. The PUMA 2E1000 supports both a Chip Select(s) and Write Enable(s) controlled write cycle. That is, the address is latched by the falling edge of either Chip Select(s) or Write Enable(s), whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select(s) or Write Enable(s), whichever occurs first. A byte/word write operation, once initiated, will automatically continue to completion, within 10 ms max.

### Page Mode Write

The page write feature of the PUMA 2E1000 allows the entire memory to be written in typically 2.05 seconds. Page Write allows 1 to 64 bytes/words of data to be written into the device during a single programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A6 through A14) for each subsequent valid write cycle to the part, during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte/word write cycle, the host can write up to 63 bytes/words in the same manner as the first byte/word written. Each successive byte/word load cycle, started by the Write Enable(s) HIGH to LOW transition, must begin within 150  $\mu$ s of the falling edge of the preceding Write Enable(s). If a subsequent Write Enable(s) HIGH to LOW transition is not detected within 150  $\mu$ s, the internal automatic programming cycle will commence.

The A0 to A5 inputs are used to specify which bytes/words within the page are to be written. The bytes/words may be loaded in any order and altered within the same load period. Only bytes/words which are specified for writing will be written; unnecessary cycling of other bytes/words within the page does not occur.

### DATA Polling

The PUMA 2E1000 features DATA Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte/word written will produce the complement of that data on D7. Once the programming is complete, D7 will reflect the true data. Note: If the PUMA 2E1000 is in a protected state and an illegal write operation is attempted DATA Polling will not operate. DATA Polling may begin at any time during the write cycle.

### TOGGLE bit

In addition to DATA polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.



### Hardware Data Protection

The PUMA 2E1000 provides hardware features to protect non-volatile data from inadvertent writes.

- $V_{CC}$  Sense - If  $V_{CC}$  is below 3.8V (typical) the write function is inhibited.
- $V_{CC}$  Power-on-Delay - Once  $V_{CC}$  has reached 3.8V the device will automatically time out 5ms (typical) before allowing a write.
- Write Inhibit - Holding any one of  $\overline{OE}$  Low,  $\overline{CS}$  High,  $\overline{WE}$  High inhibits write cycles
- Noise Filter - Pulses of less than 15ns (typical) on the  $\overline{WE}$  or  $\overline{CS}$  inputs will not initiate a write cycle.

### Software Data Protection

The PUMA 2E1000 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the PUMA 2E1000 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

### Operating Modes

The table below shows the logic inputs required to control the operation of the PUMA 2E1000.

MODE	$\overline{CS1-4}$	$\overline{OE}$	$\overline{WE1-4}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	1	0	Data in
Standby/Write inhibit	1	X	X	High-Z
Write Inhibit	X	X	1	
	X	0	X	
Output Disable	X	1	X	High-Z
Chip Erase <sup>(1)</sup>	0	1	0	High-Z

$$0 = V_{IL} : 1 = V_{IH} : X = V_{IH} \text{ or } V_{IL}$$

Notes : (1)  $\overline{OE}$  must be 12.0V  $\pm$  0.5V

### Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification, accessed by placing 12V $\pm$ 0.5V on A9 and using locations 7FC0<sub>H</sub> to 7FFF<sub>H</sub>. These locations can be used during the initial programming of each EEPROM to record data such as issue number and release date, and subsequent reprogramming can change these locations to record the alterations performed.

### Chip Erase

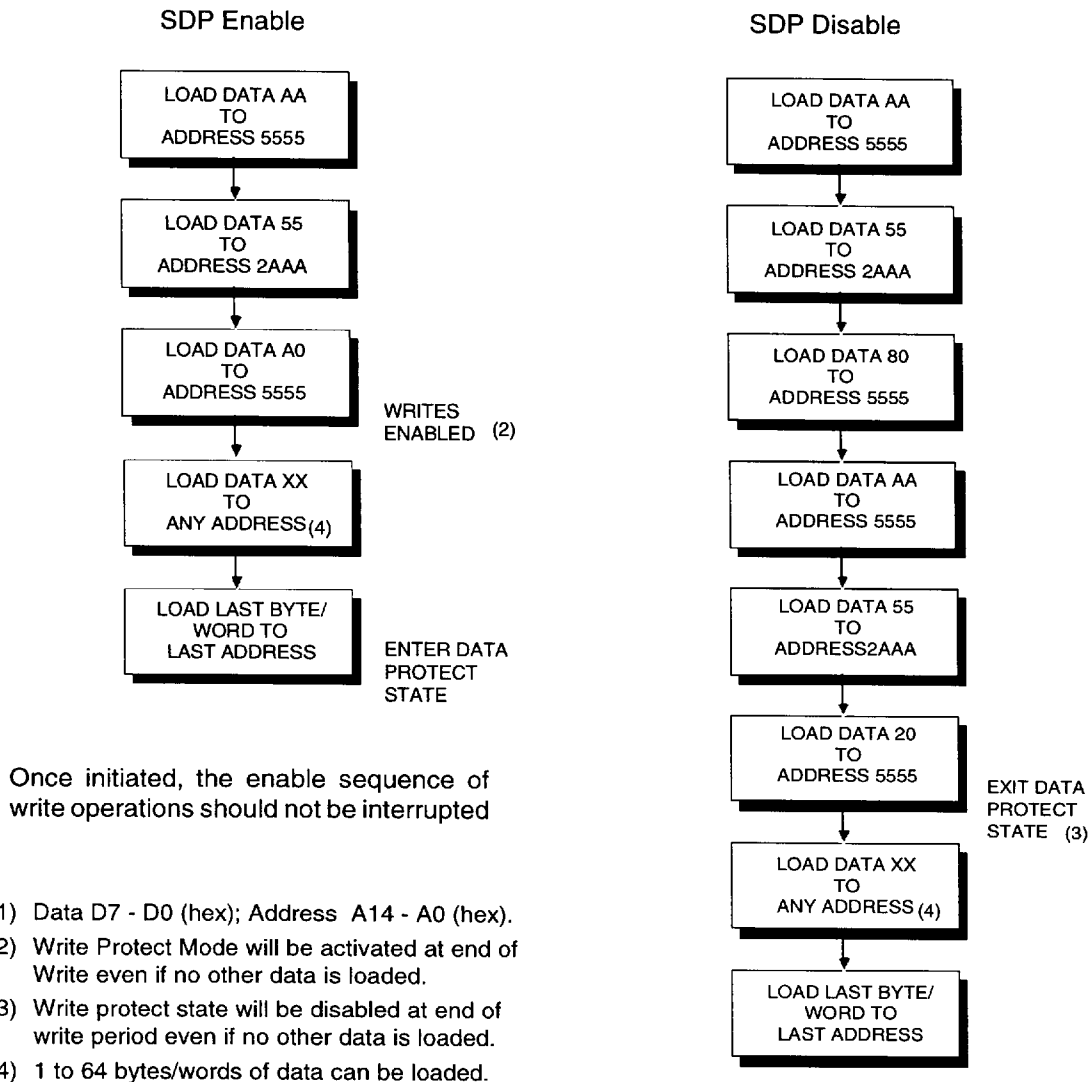
All of the memory locations on the PUMA 2E1000 can be erased in 10 ms by placing 12.0V $\pm$ 0.5V onto  $\overline{OE}$  and controlling  $\overline{WE1-4}$  and  $\overline{CS1-4}$  to follow the Chip Erase timing characteristics. This function will operate even if the module is in Software Data Protection Mode as explained later.

## Software Data Protection

Software controlled data protection, once enabled by the user, necessitates the use of a software algorithm before any Write can be performed. To enable this feature a special sequence of 3 Writes to 3 specific addresses must be performed, and must be reused for each subsequent Write cycle. Once set the data protection remains operational until it is disabled by using a second algorithm; power transitions will not reset this feature.

Note that the PUMA 2E1000 is supplied with the Software data Protection feature **disabled**.

The algorithms to enable and disable the protection are shown below:

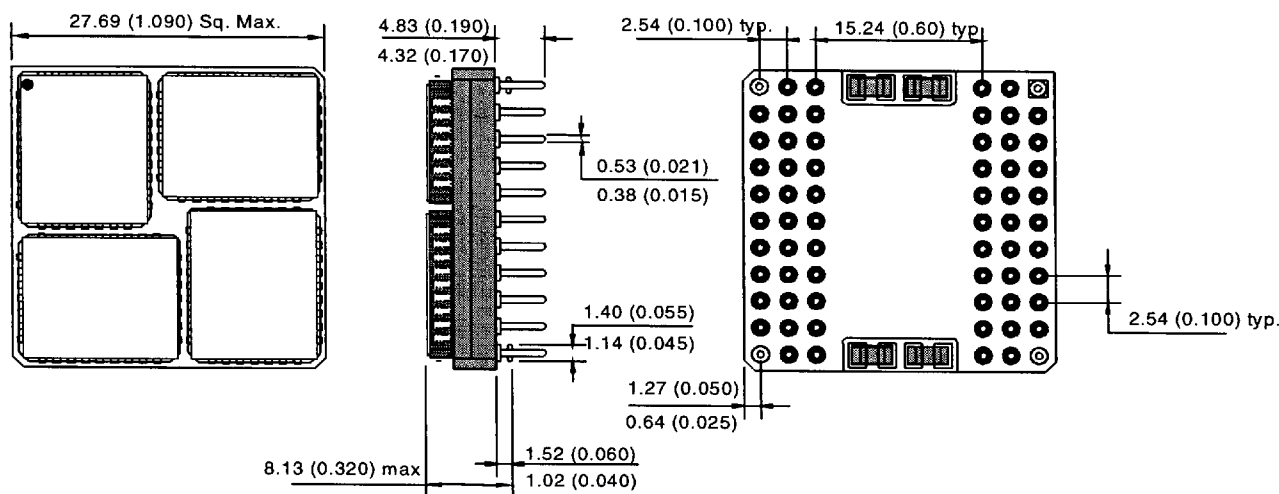


**Note:** Load Data above represents 8 bit mode. For 16 or 32 bit mode, place the load data in the 2 bytes or all 4 bytes on the data lines, respectively. Eg/ 8 bit load data = 55<sub>HEX</sub>, 16 bit load data = 5555<sub>HEX</sub>.

**All software write commands must obey the Page Write timing specifications.**

The process of disabling the Data Protection mode is very similar to that described for enable, except 6 bytes/words must be loaded to specific locations in the EEPROM as shown.

Note here the use of the word 'load' to describe enabling and disabling the protection modes in preference to 'write'. Although it may seem that if the Write command sequence is performed to enable protection then the three bytes/words at those addresses will be overwritten with AA,55,A0, this is not the case.

**Package Details** Dimensions in mm (inches).**Military Screening Procedure**

**Module Screening Flow** for high reliability product is in accordance with MIL-STD-883 method 5004 Level B and is detailed below:

<b>MB MODULE SCREENING FLOW</b>		
<b>SCREEN</b>	<b>TEST METHOD</b>	<b>LEVEL</b>
<b>Visual and Mechanical</b>		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
<b>Burn-In</b>		
Pre Burn-in Electrical	Per Applicable device Specifications at $T_A = +25^\circ\text{C}$ (optional)	100%
Burn-In	Method 1015, Condition D, $T_A = +125^\circ\text{C}$	100%
<b>Final Electrical Tests</b>	Per applicable Device Specification	
Static (dc)	a) @ $T_A = +25^\circ\text{C}$ and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ $T_A = +25^\circ\text{C}$ and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ $T_A = +25^\circ\text{C}$ and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
<b>Percent Defective Allowable (PDA)</b>	Calculated at Post Burn-in at $T_A = +25^\circ\text{C}$	10%
<b>Quality Conformance</b>	Per applicable Device Specification	Sample
<b>External Visual</b>	2009 Per HMP or customer specification	

Ordering Information
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**PUMA 2E1000LMB-70/X405**

			Speed	70	= 70 ns
				90	= 90 ns
				12	= 120 ns
			Temp. range/screening	Blank	= Commercial Temp.
				I	= Industrial Temp.
				M	= Military Temp.
				MB	= Screened in accordance with MIL-STD-883
			Power Consumption	Blank	= Standard Part
				L	= Low Power Part (-90, -12 Only)
			Memory Type	E1000	= EEPROM (Configurable as 32Kx32, 64Kx16 or 128Kx8)

**NOTES: 1. X405 indicates customer specific part.**

**X405 is designed for Fast Page Write applications.  $t_{wc} = 3ms$  (Max.).**

**If not specified when ordered only a  $t_{wc}$  of 10ms (Max.) can be guaranteed.**