

PM100RSE060

FLAT-BASE TYPE
INSULATED PACKAGE

PM100RSE060



FEATURE

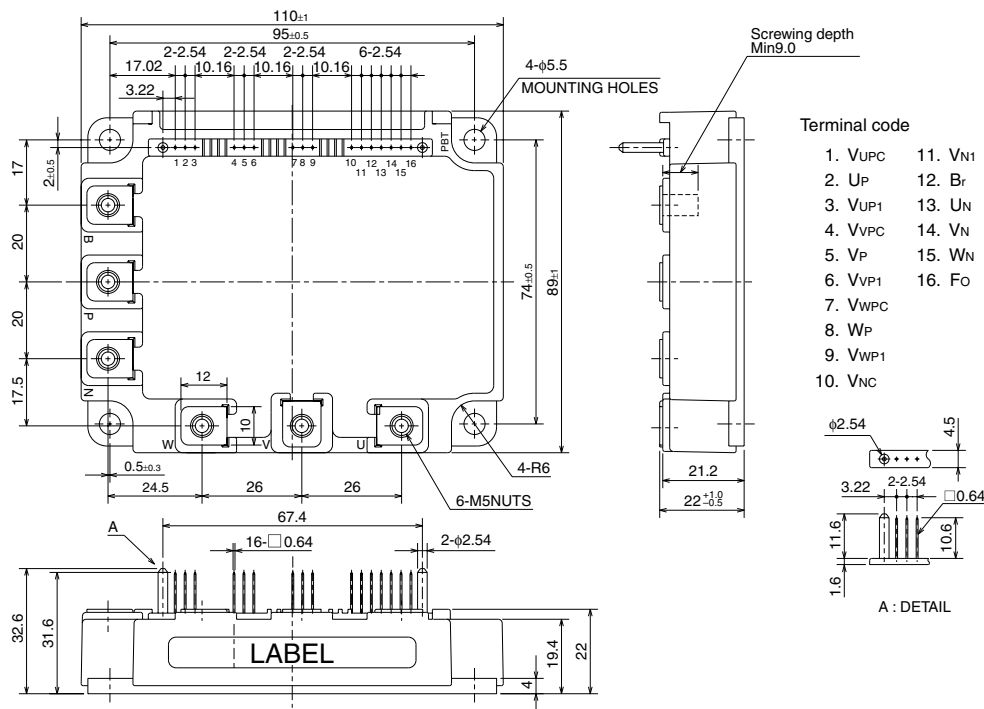
- a) Adopting new 4th generation planar IGBT chip, which performance is improved by 1μm fine rule process.
For example, typical $V_{CE(sat)}=1.7V$
- b) Using new Diode which is designed to get soft reverse recovery characteristics.
- 3φ 100A, 600V Current-sense IGBT for 15kHz switching
- 30A, 600V Current-sense regenerative brake IGBT
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage
- Acoustic noise-less 11kW class inverter application

APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES

Dimensions in mm



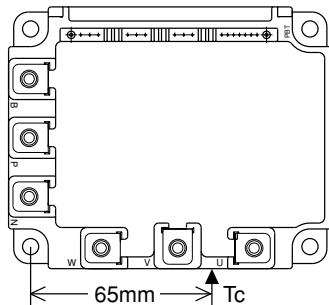
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TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Supply Voltage Protected by OC & SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = 125°C Start	400	V
V _{CC(surge)}	Supply Voltage (Surge)	Applied between : P-N, Surge value or without switching	500	V
T _c	Module Case Operating Temperature	(Note-1)	-20 ~ +100	°C
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

(Note-1) T_c measurement point is as shown below. (Base plate depth 3mm)



THERMAL RESISTANCES

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element), (Note-1)	—	—	0.38	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1 element), (Note-1)	—	—	0.70	
R _{th(j-c)Q}		Brake IGBT part, (Note-1)	—	—	0.71	
R _{th(j-c)F}		Brake FWDi part, (Note-1)	—	—	1.66	
R _{th(j-c')Q}		Inverter IGBT part (per 1 element), (Note-2)	—	—	0.23	
R _{th(j-c')F}		Inverter FWDi part (per 1 element), (Note-2)	—	—	0.36	
R _{th(j-c')Q}		Brake IGBT part, (Note-2)	—	—	0.45	
R _{th(j-c')F}		Brake FWDi part, (Note-2)	—	—	0.96	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, Thermal grease applied (per 1 module)	—	—	0.027	

(Note-2) T_c measurement point is just under the chips.

If you use this value, R_{th(f-a)} should be measured just under the chips.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 100A	T _j = 25°C	—	1.7	2.3	V
		V _{CIN} = 0V, Pulsed (Fig. 1)	T _j = 125°C	—	1.7	2.3	
V _{EC}	FWDi Forward Voltage	-I _C = 100A, V _D = 15V, V _{CIN} = 15V (Fig. 2)		—	2.2	3.3	V
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 15V↔0V		0.8	1.2	2.4	μs
t _{rr}		V _{CC} = 300V, I _C = 100A		—	0.15	0.3	
t _{c(on)}		T _j = 125°C		—	0.4	1.0	
t _{off}		Inductive Load (upper and lower arm) (Fig. 3)		—	2.4	3.3	
t _{c(off)}				—	0.6	1.2	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _{CIN} = 15V (Fig. 4)	T _j = 25°C	—	—	1	mA
			T _j = 125°C	—	—	10	

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BRAKE PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 30A V _{CIN} = 0V, Pulsed (Fig. 1)	T _J = 25°C	—	1.8	2.5	V
		T _J = 125°C	—	1.9	2.6		
V _{FM}	FWDi Forward Voltage	I _F = 30A (Fig. 2)		—	2.5	3.5	V
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _{CIN} = 15V (Fig. 4)	T _J = 25°C	—	—	1	mA
			T _J = 125°C	—	—	10	

CONTROL PART

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
Id	Circuit Current	VD = 15V, Vcin = 15V	VN1-VNC	—	44	60	mA
			VXP1-VXPC	—	13	18	
Vth(ON)	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN • Br-VNC		1.2	1.5	1.8	V
Vth(OFF)	Input OFF Threshold Voltage			1.7	2.0	2.3	
OC	Over Current Trip Level	Inverter part VD = 15V (Fig. 5,6)	Tj = -20°C	—	—	520	A
			Tj = 25°C	264	311	430	
			Tj = 125°C	158	—	—	
		Break part -20 ≤ Tj ≤ 125°C, VD = 15V (Fig. 5,6)		39	53	—	
SC	Short Circuit Trip Level	-20≤ Tj ≤ 125°C, VD = 15V (Fig. 5,6)	Inverter part	—	360	—	A
			Brake part	—	79	—	
toff(OC)	Over Current Delay Time	VD = 15V (Fig. 5,6)		—	10	—	μs
OT	Over Temperature Protection	Base-plate Temperature detection, VD = 15V	Trip level	111	118	125	°C
OTr			Reset level	—	100	—	
UV	Supply Circuit Under-Voltage Protection	-20 ≤ Tj ≤ 125°C	Trip level	11.5	12.0	12.5	V
UVr			Reset level	—	12.5	—	
IFO(H)	Fault Output Current	VD = 15V, VFO = 15V (Note-3)	—	—	0.01	mA	
IFO(L)			—	10	15		
tFO	Minimum Fault Output Pulse Width	VD = 15V (Note-3)	1.0	1.8	—	ms	

(Note-3) Fault output is given only when the internal OC, SC, OT & UV protection.

Fault output of OT protection operate by lower arm.

Fault output of OC, SC protection given pulse.

Fault output of OT, UV protection given pulse while over level.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	560	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 400	V
V _D	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC (Note-4)	15 ± 1.5	V
V _{CIN(ON)}	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN • Br-VNC	≤ 0.8	V
V _{CIN(OFF)}	Input OFF Voltage		≥ 4.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit input signal of IPM, 3φ sinusoidal PWM VVVF inverter (Fig. 8)	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 2.5	μs

(Note-4) Allowable Ripple rating of Control Voltage : dv/dt ≤ ±5V/μs, 2Vp-p

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PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "OC" and "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

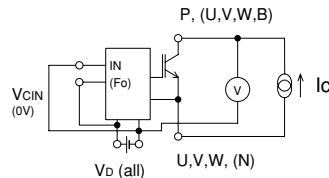


Fig. 1 $V_{CE(sat)}$ Test

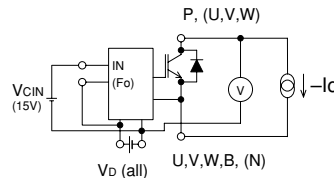
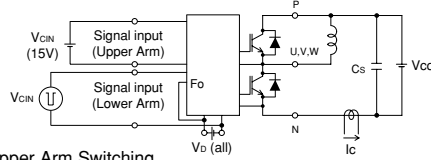


Fig. 2 V_{EC} , (V_{FM}) Test

a) Lower Arm Switching



b) Upper Arm Switching

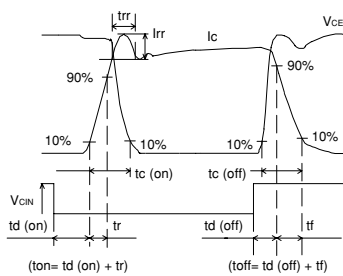
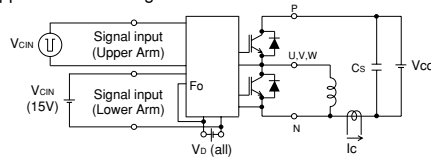


Fig. 3 Switching time Test circuit and waveform

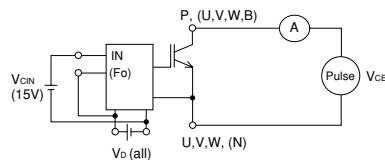


Fig. 4 I_{CES} Test

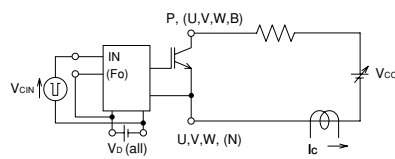


Fig. 5 OC and SC Test

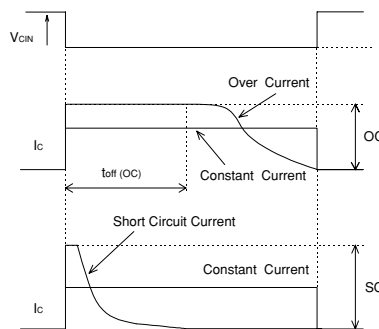


Fig. 6 OC and SC Test waveform

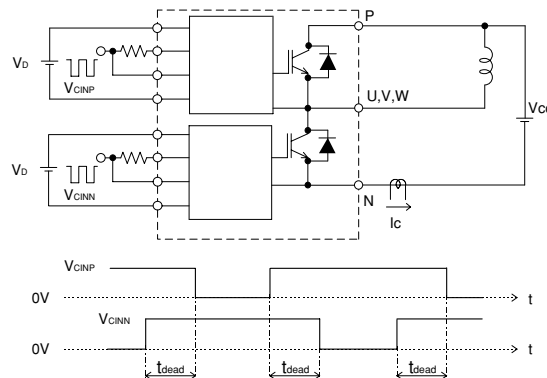
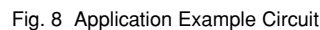


Fig. 7 Dead time measurement point example



- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Quick opto-couplers: TPLH, $TPLH \leq 0.8\mu s$. Use High CMR type. The line between opto-coupler and intelligent module should be shortened as much as possible to minimize the floating capacitance.
- Slow switching opto-coupler: recommend to use at CTR = 100 ~ 200%, Input current = 8 ~ 10mA, to work in active.
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.