

(Rev. 1.1)

MITSUBISHI LSIS

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

The M5M467400/465400BJ,BTP is organized 16777216-word by 4-bit, M5M467800/465800BJ,BTP is organized 8388608-word by 8-bit, and M5M465160BJ,BTP is organized 4194304-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and are suitable for large-capacity memory systems with high speed and low power dissipation.

The use of double-layer aluminum process combined with CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M467400BXX-5,5S M5M467800BXX-5,5S	50	13	25	13	90	300
M5M467400BXX-6,6S M5M467800BXX-6,6S	60	15	30	15	110	250
M5M465400BXX-5,5S M5M465800BXX-5,5S	50	13	25	13	90	390
M5M465400BXX-6,6S M5M465800BXX-6,6S	60	15	30	15	110	325

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M465160BXX-5,5S	50	13	25	13	90	420
M5M465160BXX-6,6S	60	15	30	15	110	390

XX=J,TP

- Standard 32 pin SOJ, 32 pin TSOP (M5M467400Bxx/M5M465400Bxx/M5M467800Bxx/M5M465800Bxx)
Standard 50 pin SOJ, 50 pin TSOP (M5M465160Bxx)
- Single 3.3 ± 0.3V supply
- Low stand-by power dissipation
1.8mW (Max) ----- LVCMOS input level
- Low operating power dissipation
M5M467400Bxx-5,5S / M5M467800Bxx-5,5S ----- 360.0mW (Max)
M5M467400Bxx-6,6S / M5M467800Bxx-6,6S ----- 324.0mW (Max)
M5M465400Bxx-5,5S / M5M465800Bxx-5,5S ----- 468.0mW (Max)
M5M465400Bxx-6,6S / M5M465800Bxx-6,6S ----- 432.0mW (Max)
M5M465160Bxx-5,5S ----- 504.0mW (Max)
M5M465160Bxx-6,6S ----- 468.0mW (Max)
- Self refresh capability*
Self refresh current ----- 400μA (Max)
- Fast-page mode , Read-modify-write, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance
- All inputs, outputs LVTTTL compatible and low capacitance
* :Applicable to self refresh version(M5M467400/465400/467800/465800/465160BJ,BTP-5S,-6S:option) only

ADDRESS

Part No.	Row Add	Col Add	Refresh	Refresh Cycle	
				Normal	S-version
M5M467400Bxx	A0-A12	A0-A10	RAS Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465400Bxx	A0-A11	A0-A11	RAS Only Ref,Normal R/W	4096/64ms	4096/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M467800Bxx	A0-A12	A0-A9	RAS Only Ref,Normal R/W	8192/64ms	8192/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465800Bxx	A0-A11	A0-A10	RAS Only Ref,Normal R/W	4096/64ms	4096/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms
M5M465160Bxx	A0-A11	A0-A9	RAS Only Ref,Normal R/W	4096/64ms	4096/128ms
			CBR Ref,Hidden Ref	4096/64ms	4096/128ms

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

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PIN DESCRIPTION

M5M467400Bxx / M5M465400Bxx

Pin Name	Function
A0-A12	Address Inputs
DQ1-DQ4	Data Inputs / Outputs
RAS	Row Address Strobe Input
CAS	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

M5M467800Bxx / M5M465800Bxx

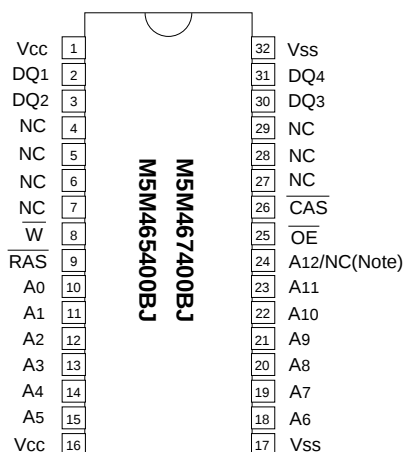
Pin Name	Function
A0-A12	Address Inputs
DQ1-DQ8	Data Inputs / Outputs
RAS	Row Address Strobe Input
CAS	Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

M5M465160Bxx

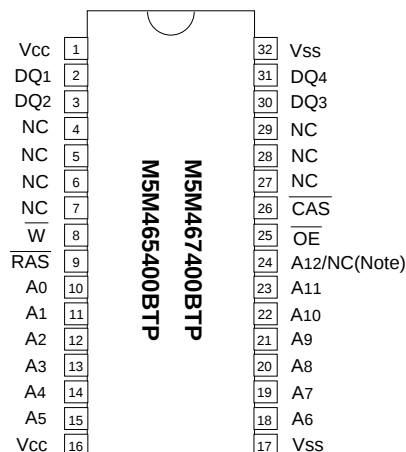
Pin Name	Function
A0-A11	Address Inputs
DQ1-DQ16	Data Inputs / Outputs
RAS	Row Address Strobe Input
$\overline{UCAS}$	Upper byte control Column Address Strobe Input
$\overline{LCAS}$	Lower byte control Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)
NC	No Connection

XX=BJ,BTP

M5M467400/465400BJ,BTP PIN CONFIGURATION (TOP VIEW)



Outline 32P0N (400mil SOJ)



Outline 32P3N (400mil TSOP Normal Bend)

Note : A12...M5M467400Bxx, NC...M5M465400Bxx

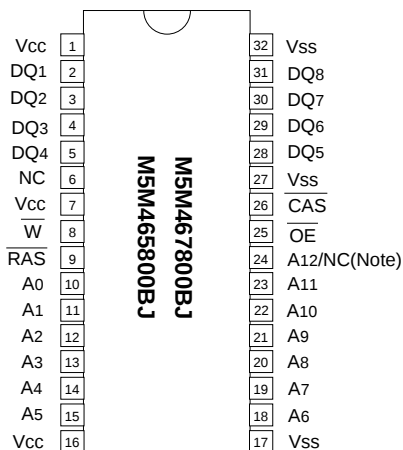
NC : NO CONNECTION

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

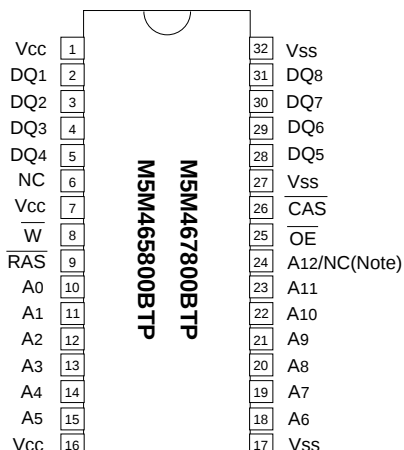
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M5M467800/465800BJ,BTP

PIN CONFIGURATION (TOP VIEW)



Outline 32P0N (400mil SOJ)



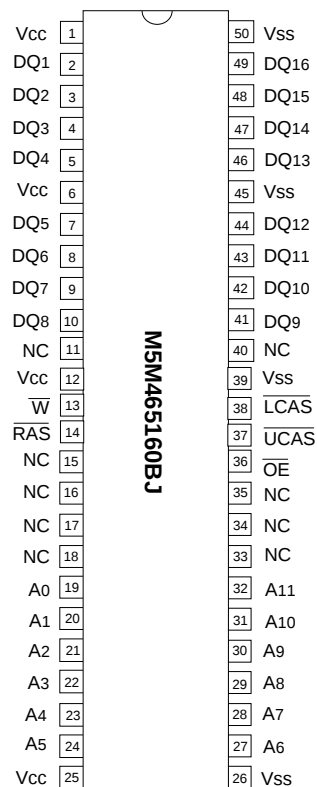
Outline 32P3N (400mil TSOP Normal Bend)

Note : A12...M5M467800Bxx, NC...M5M465800Bxx

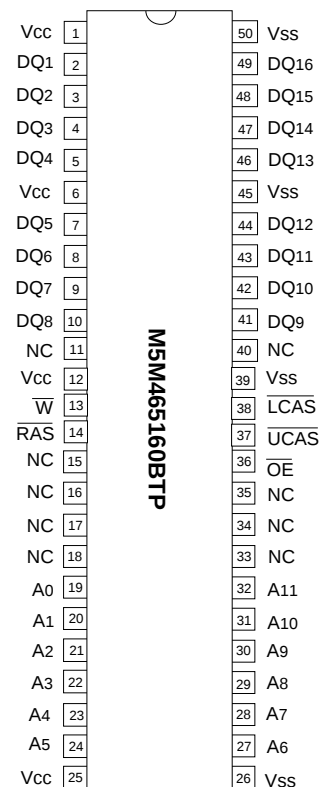
NC : NO CONNECTION

M5M465160BJ,BTP

PIN CONFIGURATION (TOP VIEW)



Outline 50P0G (400mil SOJ)



Outline 50P3G (400mil TSOP Normal Bend)

NC : NO CONNECTION

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

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FUNCTION

The M5M467400(800)/465400(800,160)BJ, BTP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., Fast page mode, CAS before RAS refresh, and delayed-write.
The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

M5M467400Bxx / M5M465400Bxx / M5M467800Bxx / M5M465800Bxx

Operation	Inputs						Input/Output		Refresh	Remark
	RAS	CAS	W	OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	FAST PAGE mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	NO	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	NO	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	NO	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
CAS before RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

M5M465160Bxx

Operation	Inputs							Input/Output		Refresh	Remark
	RAS	LCAS	UCAS	W	OE	Row address	Column address	DQ1-DQ8	DQ9-DQ16		
Lower byte read	ACT	ACT	NAC	NAC	ACT	APD	APD	VLD	OPN	NO	FAST PAGE mode identical
Upper byte read	ACT	NAC	ACT	NAC	ACT	APD	APD	OPN	VLD	NO	
Word read	ACT	ACT	ACT	NAC	ACT	APD	APD	VLD	VLD	NO	
Lower byte write	ACT	ACT	NAC	ACT	NAC	APD	APD	DIN	DNC	NO	
Upper byte write	ACT	NAC	ACT	ACT	NAC	APD	APD	DNC	DIN	NO	
Word write	ACT	ACT	ACT	ACT	NAC	APD	APD	DIN	DIN	NO	
RAS-only refresh	ACT	NAC	NAC	DNC	DNC	APD	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DNC	DNC	VLD	VLD	YES	
CAS before RAS refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	OPN	NO	

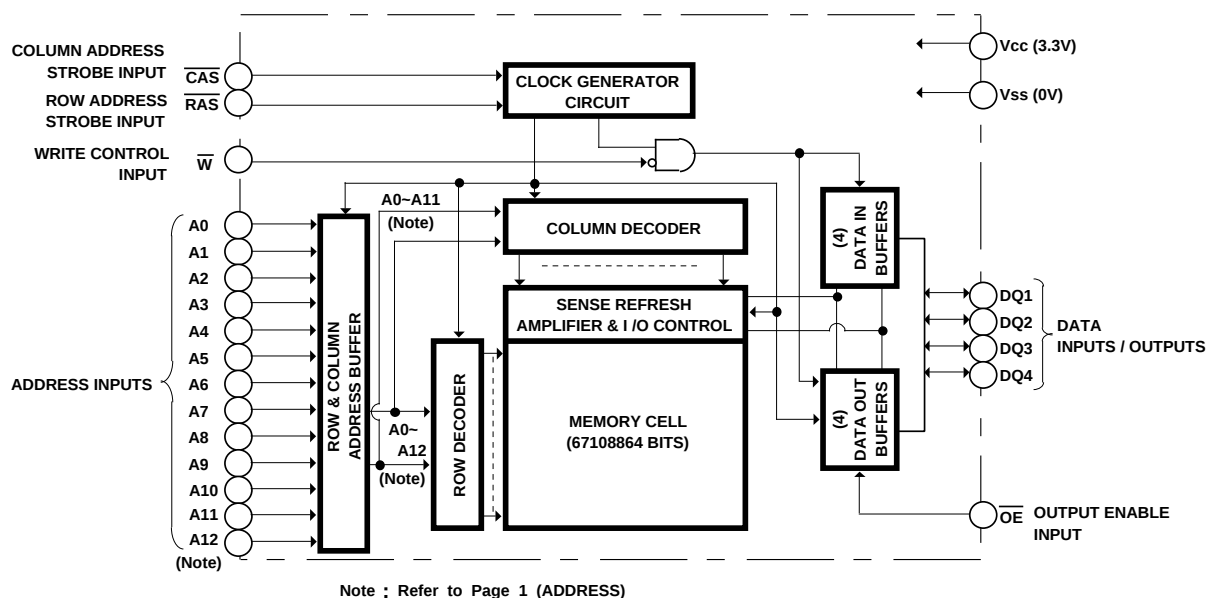
Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

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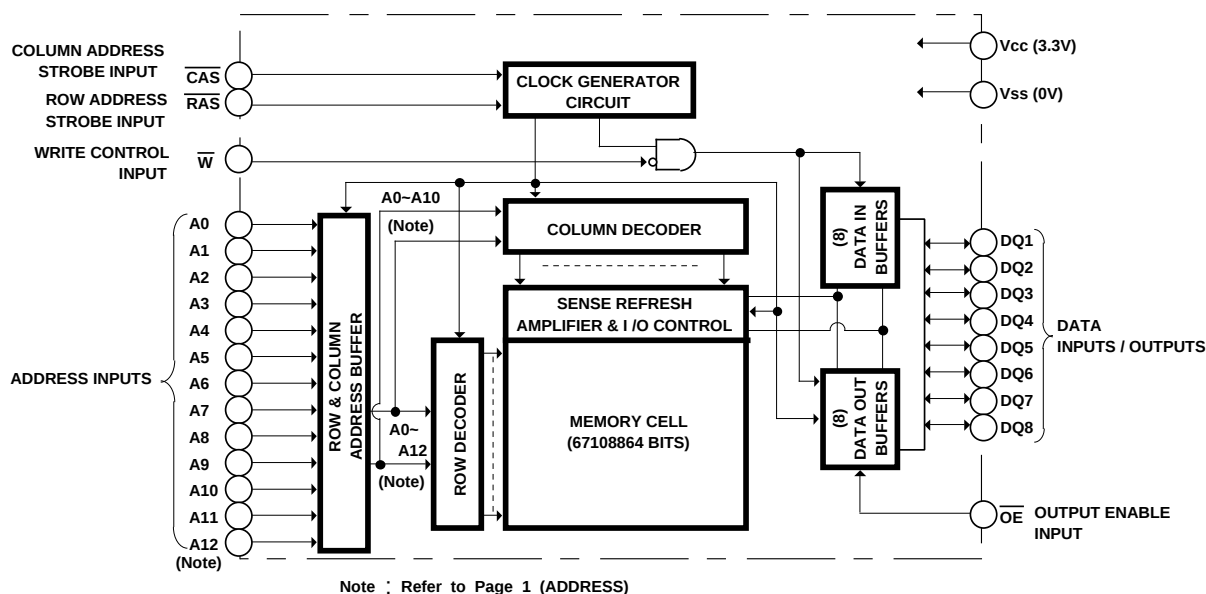
M5M467400Bxx / M5M465400Bxx

BLOCK DIAGRAM



M5M467800Bxx / M5M465800Bxx

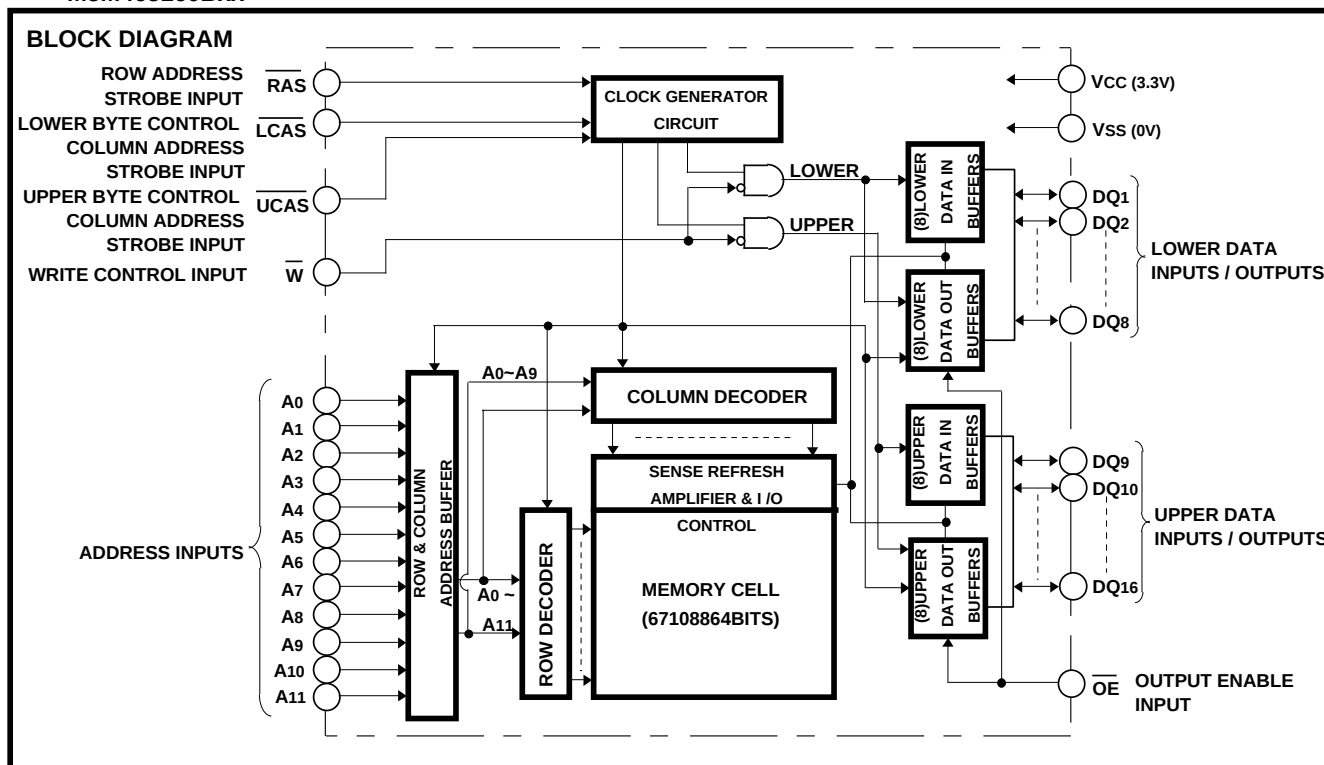
BLOCK DIAGRAM



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

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M5M465160Bxx



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-0.5 ~ 4.6	V
V _I	Input voltage		-0.5 ~ 4.6	V
V _O	Output voltage		-0.5 ~ 4.6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	3.0	3.3	3.6	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.0		V _{CC} +0.3	V
V _{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{CC}=3.3 ± 0.3V, V_{SS}=0V, unless otherwise noted) (Note 2)

[M5M467400B / M5M467800B]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} =-2mA	2.4		V _{CC}	v
V _{OL}	Low-level output voltage		I _{OL} =2mA	0		0.4	v
I _{OZ}	Off-state output current		Q floating 0V ≤ V _{OUT} ≤ V _{CC}	-10		10	μA
I _I	Input current		0V ≤ V _{IN} ≤ V _{CC} +0.3V, Other input pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	M5M467400B-5,5S M5M467800B-5,5S	RAS, CAS cycling trc=twc=min. output open			100	mA
		M5M467400B-6,6S M5M467800B-6,6S				90	
I _{CC2} (AV)	Average supply current from V _{CC} stand-by (Note 6)	M5M467400B-5,5S -6,6S M5M467800B-5,5S -6,6S	RAS= CAS =V _{IH} , output open			1	mA
		M5M467400B-5,6 M5M467800B-5,6	RAS= CAS ≥V _{CC} -0.2V,output open			0.5	
		M5M467400B-5S,6S M5M467800B-5S,6S				0.3	
I _{CC4} (AV)	Average supply current from V _{CC} Fast-Page-Mode (Note 3,4,5)	M5M467400B-5,5S M5M467800B-5,5S	RAS=V _{IL} , CAS cycling tpc=min. output open			100	mA
		M5M467400B-6,6S M5M467800B-6,6S				90	
I _{CC6} (AV)	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3,5)	M5M467400B-5,5S M5M467800B-5,5S	CAS before RAS refresh cycling trc=min. output open			130	mA
		M5M467400B-6,6S M5M467800B-6,6S				120	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC4} (AV) and I_{CC6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and CAS=V_{IH}.

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ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

[M5M465400B / M5M465800B]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} =-2mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage		I _{OL} =2mA	0		0.4	V
I _{OZ}	Off-state output current		Q floating 0V ≤ V _{OUT} ≤ V _{CC}	-10		10	μA
I _I	Input current		0V ≤ V _{IN} ≤ V _{CC} +0.3V, Other input pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	M5M465400B-5,5S M5M465800B-5,5S	RAS, CAS cycling trc=twc=min. output open			130	mA
		M5M465400B-6,6S M5M465800B-6,6S				120	
I _{CC2} (AV)	Average supply current from V _{CC} stand-by (Note 6)	M5M465400B-5,5S -6,6S M5M465800B-5,5S -6,6S	RAS= CAS =V _{IH} , output open			1	mA
		M5M465400B-5,6 M5M465800B-5,6	RAS= CAS ≥V _{CC} -0.2V, output open			0.5	
		M5M465400B-5S,6S M5M465800B-5S,6S				0.3	
I _{CC4} (AV)	Average supply current from V _{CC} Fast-Page-Mode (Note 3,4,5)	M5M465400B-5,5S M5M465800B-5,5S	RAS=V _{IL} , CAS cycling tpc=min. output open			100	mA
		M5M465400B-6,6S M5M465800B-6,6S				90	
I _{CC6} (AV)	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3,5)	M5M465400B-5,5S M5M465800B-5,5S	CAS before RAS refresh cycling trc=min. output open			130	mA
		M5M465400B-6,6S M5M465800B-6,6S				120	

[M5M465160B]

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} =-2mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage		I _{OL} =2mA	0		0.4	V
I _{OZ}	Off-state output current		Q floating 0V ≤ V _{OUT} ≤ V _{CC}	-10		10	μA
I _I	Input current		0V ≤ V _{IN} ≤ V _{CC} +0.3V, Other input pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	M5M465160B-5,5S M5M465160B-6,6S	RAS, CAS cycling trc=twc=min. output open			140	mA
						130	
I _{CC2} (AV)	Average supply current from V _{CC} stand-by (Note 6)	M5M465160B-5,5S -6,6S	RAS= CAS =V _{IH} , output open			1	mA
		M5M465160B-5,6 M5M465160B-5S,6S	RAS= CAS ≥V _{CC} -0.2V, output open			0.5	
						0.3	
I _{CC4} (AV)	Average supply current from V _{CC} Fast-Page-Mode (Note 3,4,5)	M5M465160B-5,5S M5M465160B-6,6S	RAS=V _{IL} , CAS cycling tpc=min. output open			105	mA
						95	
I _{CC6} (AV)	Average supply current from V _{CC} CAS before RAS refresh mode (Note 3,5)	M5M465160B-5,5S M5M465160B-6,6S	CAS before RAS refresh cycling trc=min. output open			140	mA
						130	

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CAPACITANCE (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{I(A)}	Input capacitance, address inputs	Vi=Vss f=1MHz Vi=25mVrms			5	pF
C _{I(OE)}	Input capacitance, OE input				7	pF
C _{I(W)}	Input capacitance, write control input				7	pF
C _{I(RAS)}	Input capacitance, RAS input				7	pF
C _{I(CAS)}	Input capacitance, CAS input				7	pF
C _{I/O}	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3 ± 0.3V, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M46S160B-5,5S		M5M46S160B-6,6S		
		Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7,8)		13		15	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 7,9)		50		60	ns
tAA	Column address access time (Note 7,10)		25		30	ns
tCPA	Access time from CAS precharge (Note 7,11)		30		35	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		13		15	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	13	0	15	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	13	0	15	ns

Note 6: An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS before RAS refresh).

Note the RAS may be cycled during the initial pause. And any eight initialization cycles are required after prolonged periods (greater than 64 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-2mA) / VOL=0.4V(IOL=2mA) loads and 100pF. The reference levels for measuring of output signals are VOH=2.0V and VOL=0.8V.

8: Assumes that trCD ≥ trCD(max) and tASC ≥ tASC(max) and tCP ≥ tCP(max).

9: Assumes that trCD ≤ trCD(max) and tRAD ≤ tRAD(max). If trCD or tRAD is greater than the maximum recommended value shown in this table, trAC will increase by amount that trCD exceeds the value shown.

10: Assumes that tRAD ≥ tRAD(max) and tASC ≤ tASC(max).

11: Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).

12: tOFF(max) and tOEZ(max) defines the time at which the output achieves the high impedance state (IOUT ≤ ±10 μA) and is not reference to VOH(min) or VOL(max).

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles) (Ta=0 ~ 70°C, Vcc=3.3 ±0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M465160B-5,5S		M5M465160B-6,6S		
		Min	Max	Min	Max	
tREF	Refresh cycle time		64		64	ms
tREF	Refresh cycle time (S-version only)		128		128	ms
trP	RAS high pulse width	30		40		ns
trCD	Delay time, RAS low to CAS low (Note15)	18	37	20	45	ns
tCRP	Delay time, CAS high to RAS low	5		10		ns
trPC	Delay time, RAS high to CAS low	0		0		ns
tCPN	CAS high pulse width	8		10		ns
tRAD	Column address delay time from RAS low (Note16)	13	25	15	30	ns
tASR	Row address setup time before RAS low	0		0		ns
tASC	Column address setup time before CAS low (Note17)	0	7	0	10	ns
tRAH	Row address hold time after RAS low	8		10		ns
tCAH	Column address hold time after CAS low	13		15		ns
tdZC	Delay time, data to CAS low (Note18)	0		0		ns
tdZO	Delay time, data to OE low (Note18)	0		0		ns
tcDD	Delay time, CAS high to data (Note19)	13		15		ns
todd	Delay time, OE high to data (Note19)	13		15		ns
tr	Transition time (Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed $t_T = 5\text{ns}$.

14: $V_{IH(\min)}$ and $V_{IL(\max)}$ are reference levels for measuring timing of input signals. $V_{IH(\min)}$ and $V_{IL(\max)}$ of the switching characteristics are 2.0V and 0.8V respectively.

15: $t_{\text{RCD}(\max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{\text{RCD}(\max)}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{\text{RCD}(\max)}$, access time is controlled exclusively by t_{CAC} or t_{AA} . $t_{\text{RCD}(\min)}$ is specified as $t_{\text{RCD}(\min)} = t_{\text{RAH}(\min)} + 2t_T + t_{\text{ASC}(\min)}$.

16: $t_{\text{RAD}(\max)}$ is specified as a reference point only. If $t_{\text{RAD}} \geq t_{\text{RAD}(\max)}$ and $t_{\text{ASC}} \geq t_{\text{ASC}(\max)}$, access time is controlled exclusively by t_{AA} .

17: $t_{\text{ASC}(\max)}$ is specified as a reference point only. If $t_{\text{RCD}} \geq t_{\text{RCD}(\max)}$ and $t_{\text{ASC}} \geq t_{\text{ASC}(\max)}$, access time is controlled exclusively by t_{CAC} .

18: Either t_{DZC} or t_{DZO} must be satisfied.

19: Either t_{CDD} or t_{ODD} must be satisfied.

20: t_T is measured between $V_{IH(\min)}$ and $V_{IL(\max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M465160B-5,5S		M5M465160B-6,6S		
		Min	Max	Min	Max	
tRC	Read cycle time	90		110		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	50	10000	60	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	13	10000	15	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after RAS low	50		60		ns
tRSH	RAS hold time after CAS low	13		15		ns
tRCS	Read Setup time before CAS low	0		0		ns
tRCH	Read hold time after CAS high (Note 21)	0		0		ns
tRRH	Read hold time after RAS high (Note 21)	10		10		ns
tRAL	Column address to RAS hold time	25		30		ns
toCH	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		ns
toRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	13		15		ns

Note 21: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M465160B-5,5S		M5M465160B-6,6S		
		Min	Max	Min	Max	
tWC	Write cycle time	90		110		ns
tRAS	RAS low pulse width	50	10000	60	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	ns
tCSH	CAS hold time after RAS low	50		60		ns
tRSH	RAS hold time after CAS low	13		15		ns
tWCS	Write setup time before CAS low (Note 23)	0		0		ns
tWCH	Write hold time after CAS low	8		10		ns
tCWL	CAS hold time after W low	13		15		ns
trWL	RAS hold time after W low	13		15		ns
tWP	Write pulse width	8		10		ns
tDS	Data setup time before CAS low or W low	0		0		ns
tDH	Data hold time after CAS low or W low	8		10		ns
toEH	OE hold time after W low	13		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M465160B-5,5S		M5M465160B-6,6S		
		Min	Max	Min	Max	
t _{RWC}	Read write/read modify write cycle time (Note22)	126		150		ns
t _{RAS}	RAS low pulse width	85	10000	95	10000	ns
t _{CAS}	CAS low pulse width	50	10000	50	10000	ns
t _{CSH}	CAS hold time after $\overline{\text{RAS}}$ low	85		95		ns
t _{RS}	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	50		50		ns
t _{RCS}	Read setup time before $\overline{\text{CAS}}$ low	0		0		ns
t _{CWD}	Delay time, CAS low to W low (Note23)	30		30		ns
t _{RWD}	Delay time, RAS low to W low (Note23)	65		75		ns
t _{AWD}	Delay time, address to W low (Note23)	40		45		ns
t _{CWL}	CAS hold time after $\overline{\text{W}}$ low	13		15		ns
t _{RWL}	RAS hold time after $\overline{\text{W}}$ low	13		15		ns
t _{WP}	Write pulse width	8		10		ns
t _{DS}	Data setup time before $\overline{\text{CAS}}$ low or $\overline{\text{W}}$ low	0		0		ns
t _{DH}	Data hold time after CAS low or W low	8		10		ns
t _{OE}	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	13		15		ns

Note 22: t_{RWC} is specified as t_{RWC}(min)=t_{RAS}(max)+t_{ODD}(min)+t_{RWL}(min)+t_{RP}(min)+4t_t.

23: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If t_{WCS} ≥ t_{WCS}(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t_{CWD} ≥ t_{CWD}(min), t_{RWD} ≥ t_{RWD}(min), t_{AWD} ≥ t_{AWD}(min) and t_{CPWD} ≥ t_{CPWD}(min) (for Fast Page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the DQ (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to V_{ih}) is indeterminate.

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M465160B-5,5S		M5M465160B-6,6S		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		ns
tPRWC	Fast page mode read write/read modify write cycle time	70		75		ns
tRAS	RAS low pulse width for read write cycle (Note25)	85	125000	100	125000	ns
tCP	CAS high pulse width (Note26)	8	12	10	15	ns
tCPRH	RAS hold time after CAS precharge	30		35		ns
tCPWD	Delay time, CAS precharge to W low (Note23)	30		35		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Fast page mode cycle.

25: t_{RAS(min)} is specified as two cycles of $\overline{\text{CAS}}$ input are performed.

26: t_{CP(max)} is specified as a reference point only. If t_{CP} ≥ t_{CP(max)}, access time is controlled exclusively by t_{CAC}.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		M5M46X400B-5,5S		M5M46X400B-6,6S		
		M5M46X800B-5,5S		M5M46X800B-6,6S		
		M5M465160B-5,5S		M5M465160B-6,6S		
		Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	5		5		ns
tCHR	CAS hold time after RAS low	10		10		ns
tRSR	Read setup time before RAS low	10		10		ns
tRHR	Read hold time after RAS low	10		10		ns

Note 27: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles instead of eight $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S / -6S . The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I _{CC8} (AV)	Average supply current from V _{CC} Extended - Refresh cycle (note 5,6)	M5M46X400B-5S,6S M5M46X800B-5S,6S M5M465160B-5S,6S CAS before RAS refresh cycling input high level $\geq$ V _{CC} -0.2V input low level $\leq$ 0.2V output = OPEN, t _{RC} = 31.25μs t _{RAS} = t _{RAS} (min) ~ 300ns			500	μA
I _{CC9} (AV)	Average supply current from V _{CC} Self - Refresh cycle (note 6)	M5M46X400B-5S,6S M5M46X800B-5S,6S M5M465160B-5S,6S RAS = CAS $\leq$ 0.2V output = OPEN			400	μA

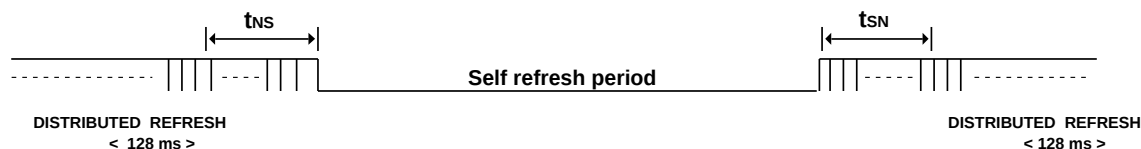
TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		M5M46X400B-5S		M5M46X400B-6S		
		M5M46X800B-5S		M5M46X800B-6S		
		M5M465160B-5S		M5M465160B-6S		
		Min	Max	Min	Max	
t _{RASS}	Self Refresh RAS low pulse width	100		100		μS
t _{RPS}	Self Refresh RAS high precharge time	90		110		ns
t _{CHS}	Self Refresh CAS hold time	- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

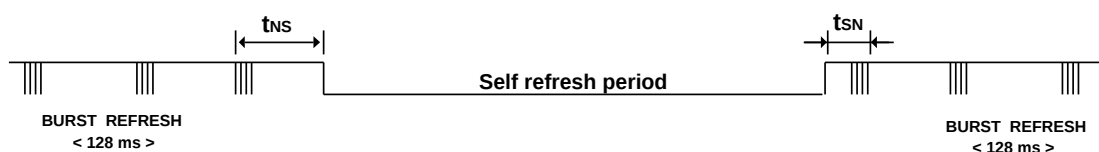
(1) In case of CBR distributed refresh

The last / first full refresh cycles must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} $\leq$ 128 ms and t_{SN} $\leq$ 128 ms.



(2) In case of burst refresh

The last / first full refresh cycles must be made within t_{NS} / t_{SN} before / after self refresh , on the condition of t_{NS} $\leq$ 16 ms and t_{SN} $\leq$ 16 ms.

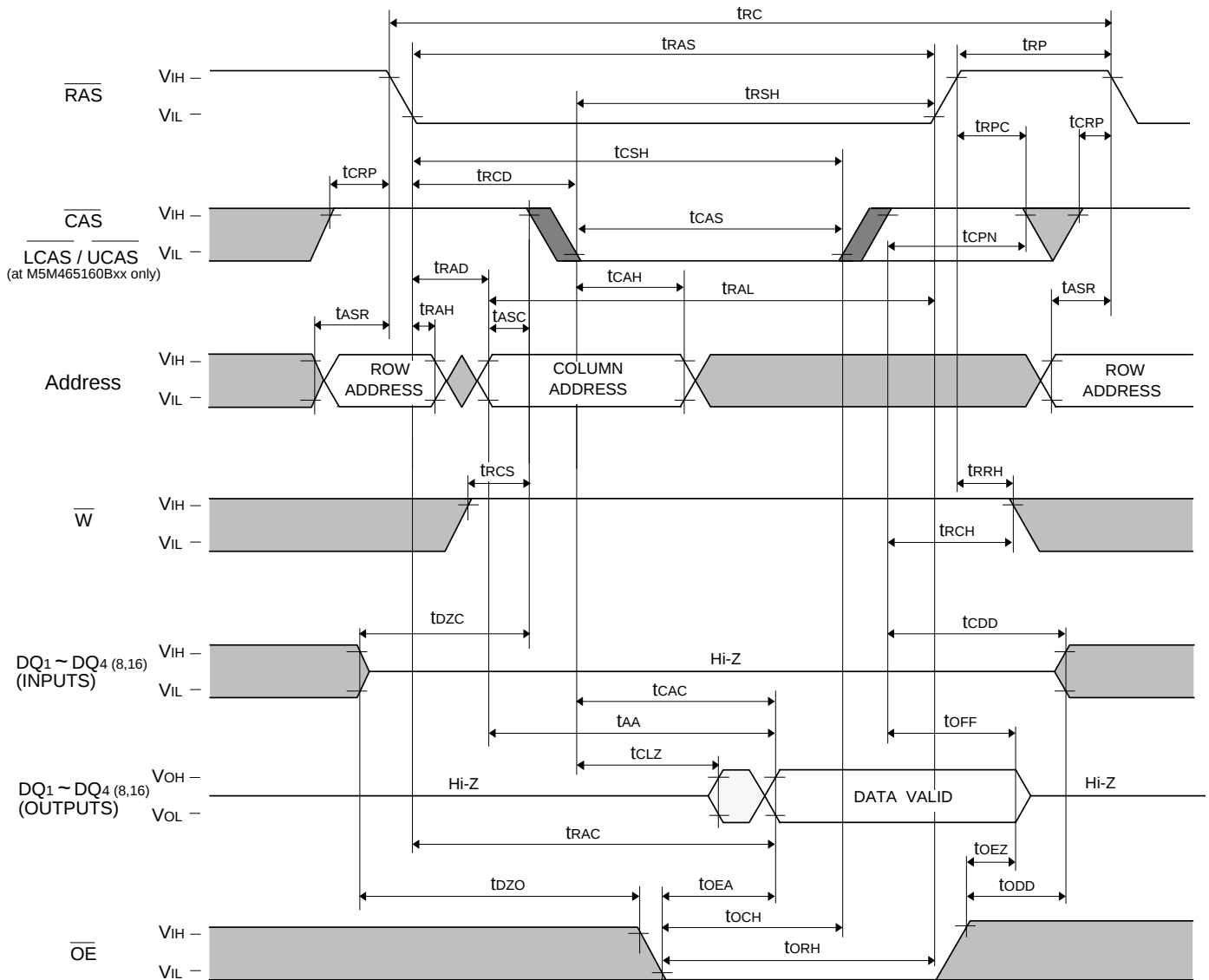


M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Timing Diagrams (Note 28)

Read Cycle



Note 28:



Indicates the don't care input.
 $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ or $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$



Indicates the invalid output.

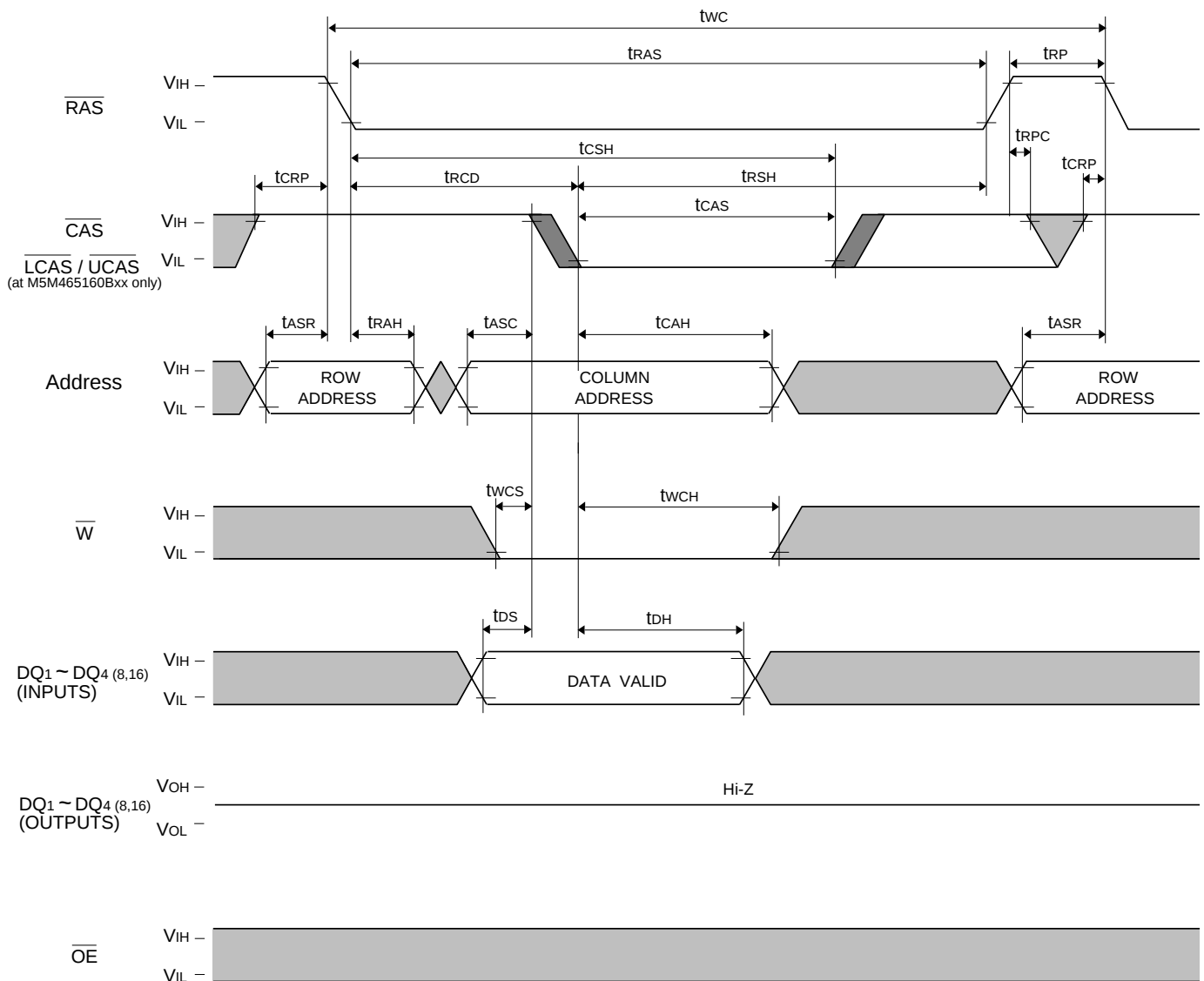


Indicates the skew of the two inputs. (at M5M465160xx only)

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

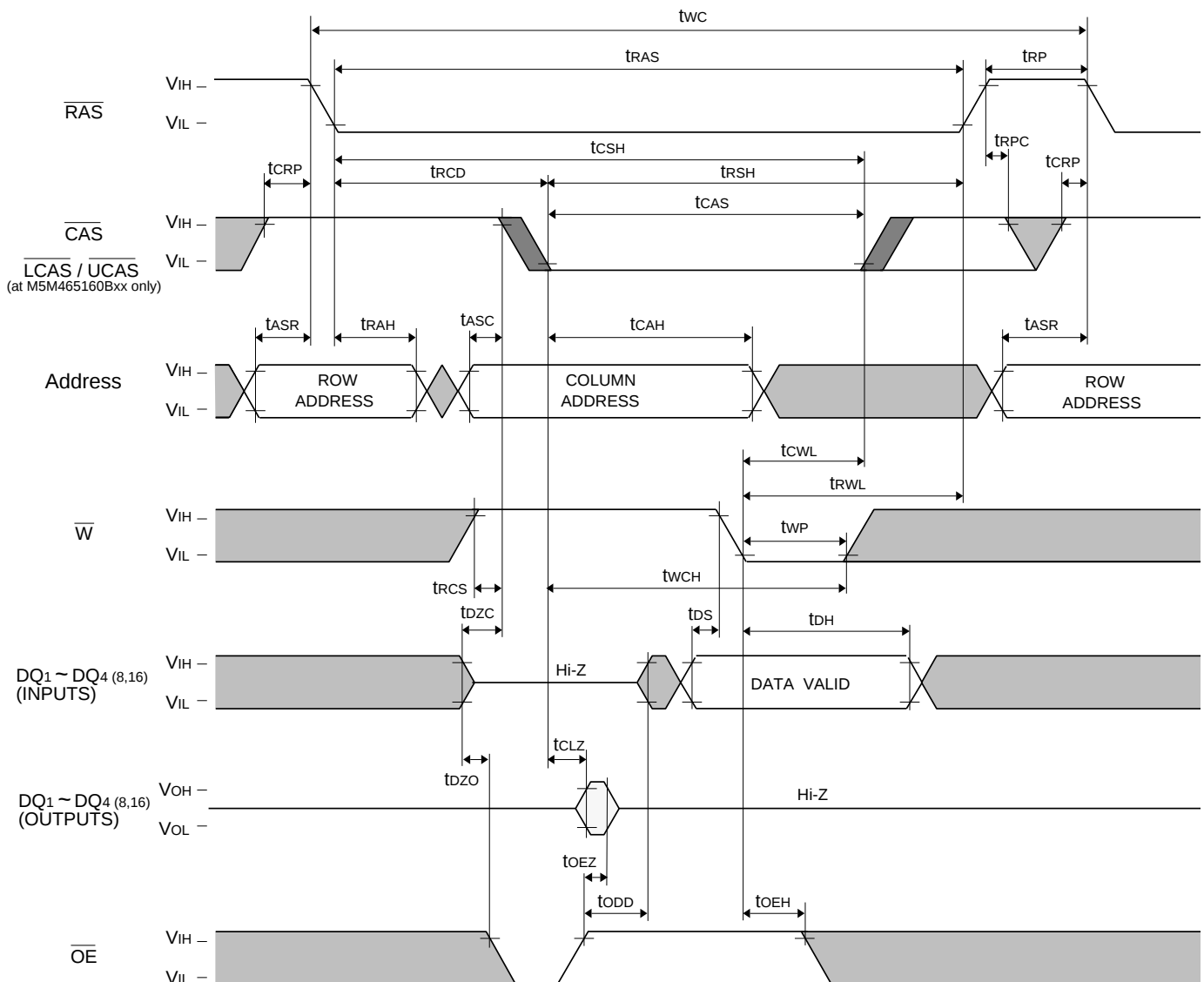
Write Cycle (Early Write)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

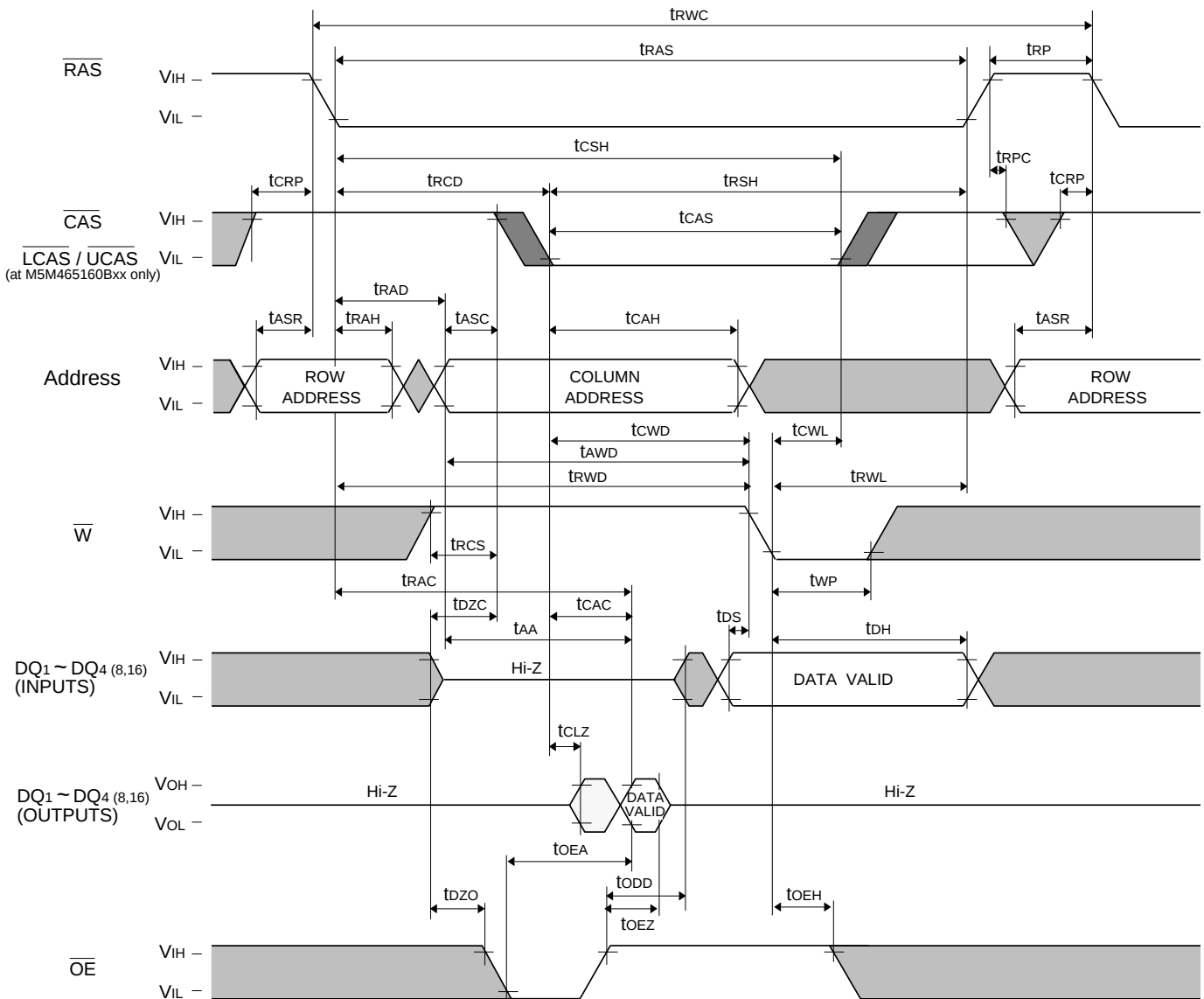
Write Cycle (Delayed Write)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Read-Write, Read-Modify-Write Cycle



FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

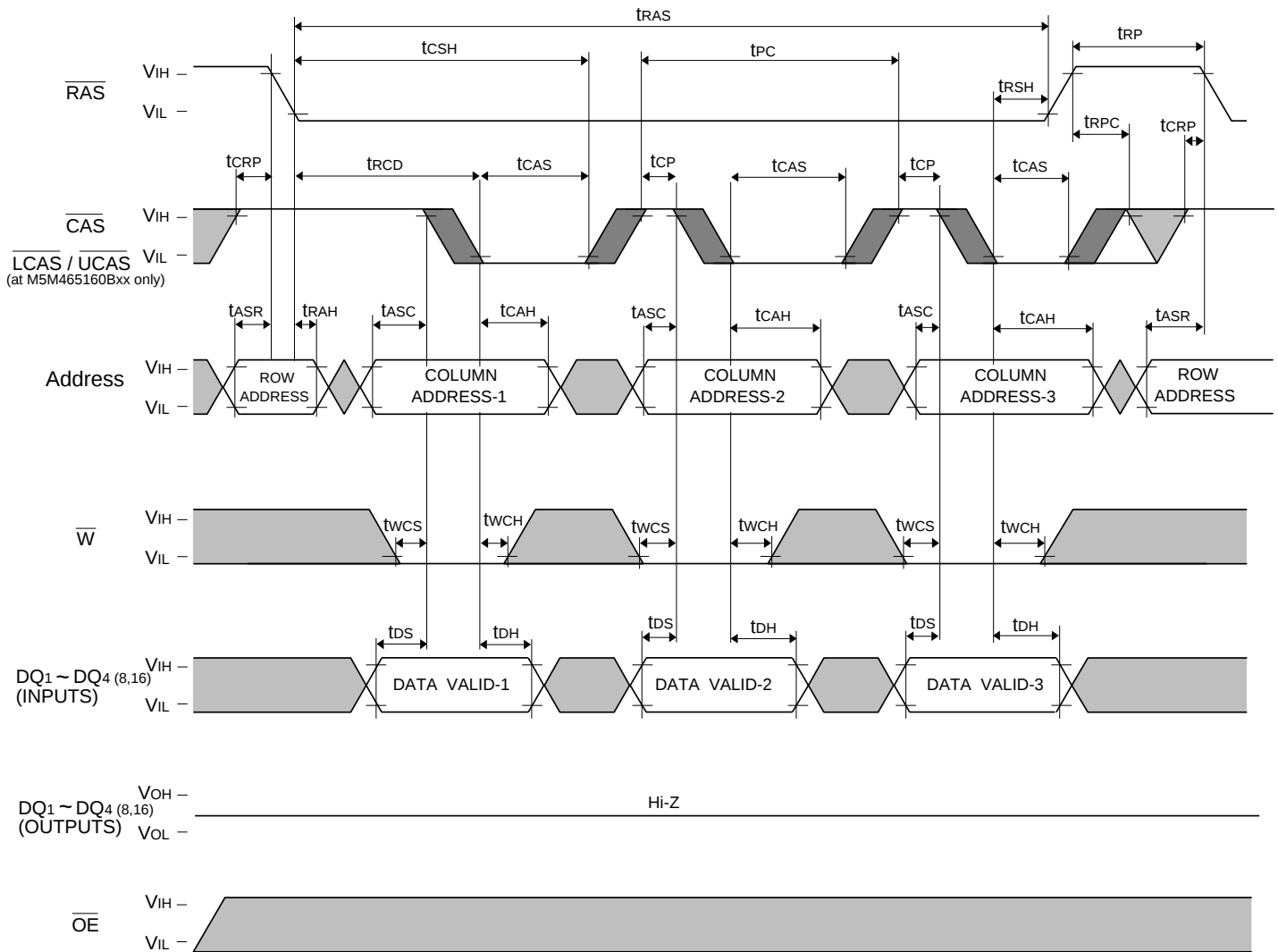
The diagram illustrates the timing relationships for the M5M465160Bxx memory device. It shows the signals $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address, $\overline{\text{W}}$, $\text{DQ}_1 \sim \text{DQ}_4$ (INPUTS), $\text{DQ}_1 \sim \text{DQ}_4$ (OUTPUTS), and $\overline{\text{OE}}$. The timing parameters are defined as follows:

- t_{CSH} : RAS setup time before CAS.
- t_{PC} : RAS pulse width.
- t_{CRPH} : RAS hold time after CAS.
- t_{RP} : RAS period.
- t_{CRP} : RAS to CAS setup time.
- t_{RCD} : RAS to CAS delay.
- t_{CAS} : CAS pulse width.
- t_{CP} : CAS to RAS delay.
- t_{CAH} : CAS hold time after RAS.
- t_{ASR} : Address setup time before RAS.
- t_{RAH} : Address hold time after RAS.
- t_{ASC} : Address setup time before CAS.
- t_{RAD} : Address hold time after CAS.
- t_{AA} : Address to RAS delay.
- t_{RRH} : RAS hold time after RAS.
- t_{RCH} : RAS hold time after RAS.
- t_{DZC} : Data to RAS delay.
- t_{CDD} : Data to RAS delay.
- t_{CAC} : Data to RAS delay.
- t_{CLZ} : Data to RAS delay.
- t_{OFF} : Data to RAS delay.
- t_{AA} : Address to RAS delay.
- t_{CPA} : Address to RAS delay.
- t_{RAC} : Address to RAS delay.
- t_{DZO} : Data to RAS delay.
- t_{OEA} : Data to RAS delay.
- t_{TOCH} : Data to RAS delay.
- t_{TODD} : Data to RAS delay.
- t_{TORH} : Data to RAS delay.
- t_{TOEZ} : Data to RAS delay.
- t_{TODD} : Data to RAS delay.
- t_{TOCH} : Data to RAS delay.

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

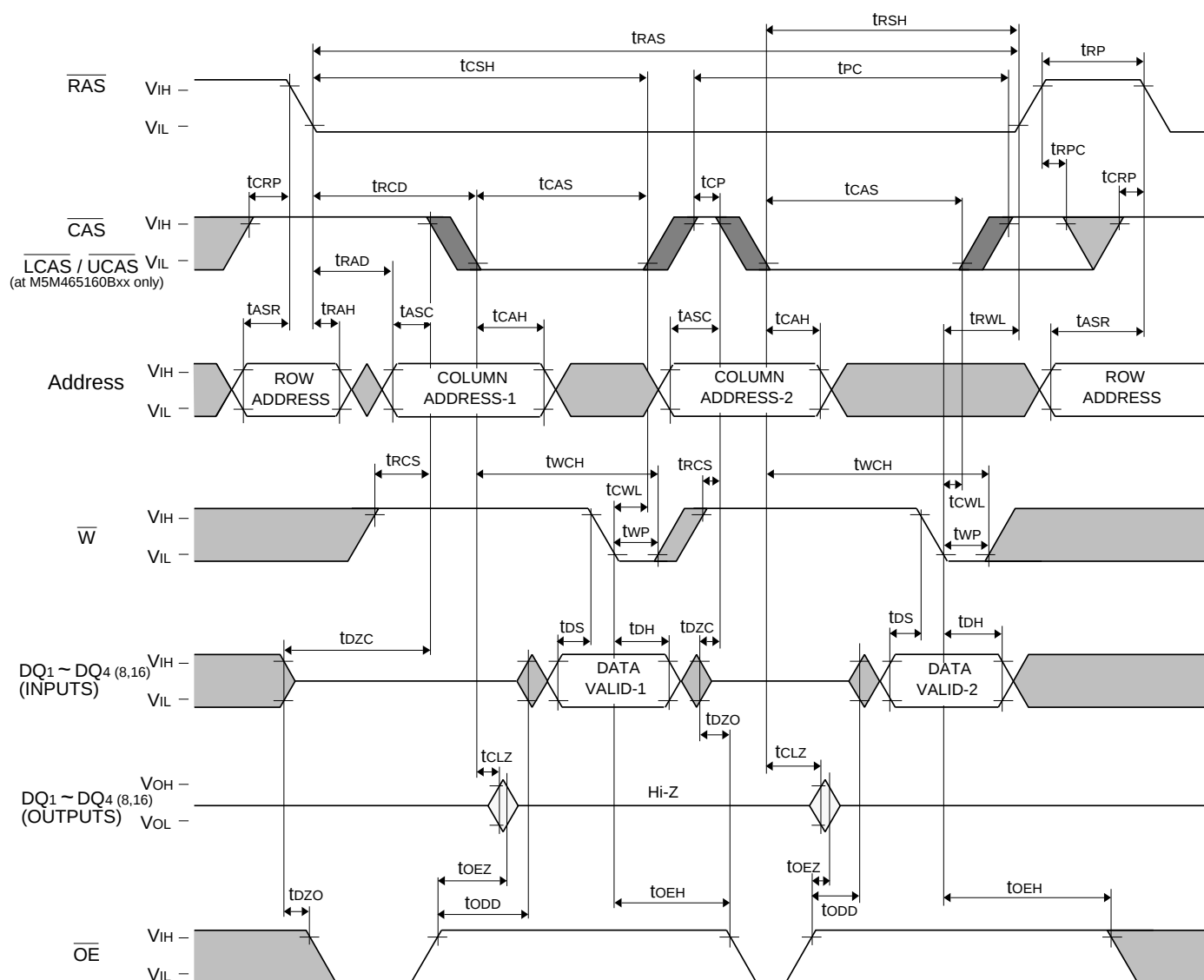
Fast Page Mode Write Cycle (Early Write)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S
M5M467800/465800BJ,BTP -5,-6,-5S,-6S
M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Write Cycle (Delayed Write)



FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

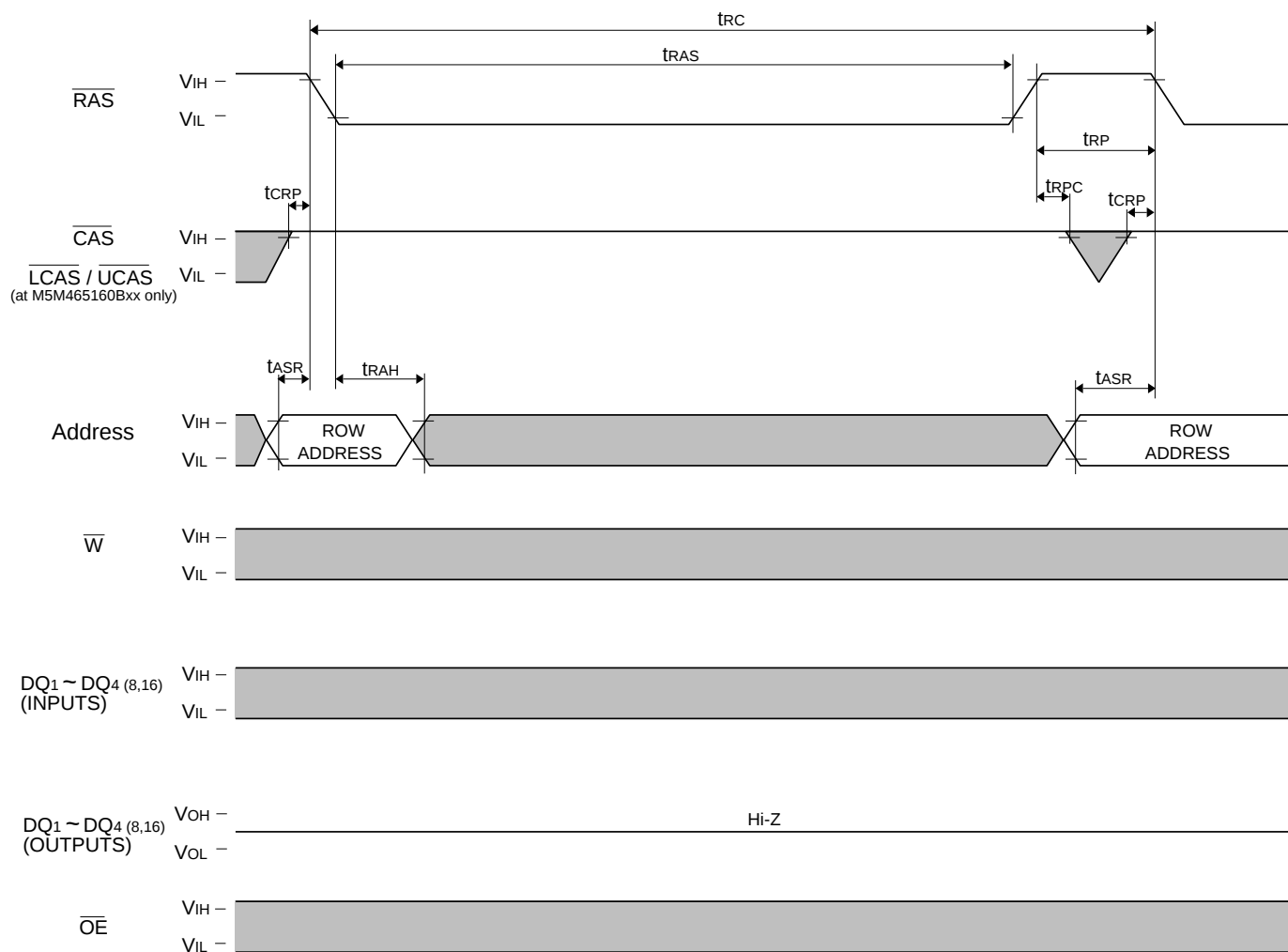
[illegible]

M5M467400/465400BJ,BTP -5,-6,-5S,-6S
M5M467800/465800BJ,BTP -5,-6,-5S,-6S
M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM

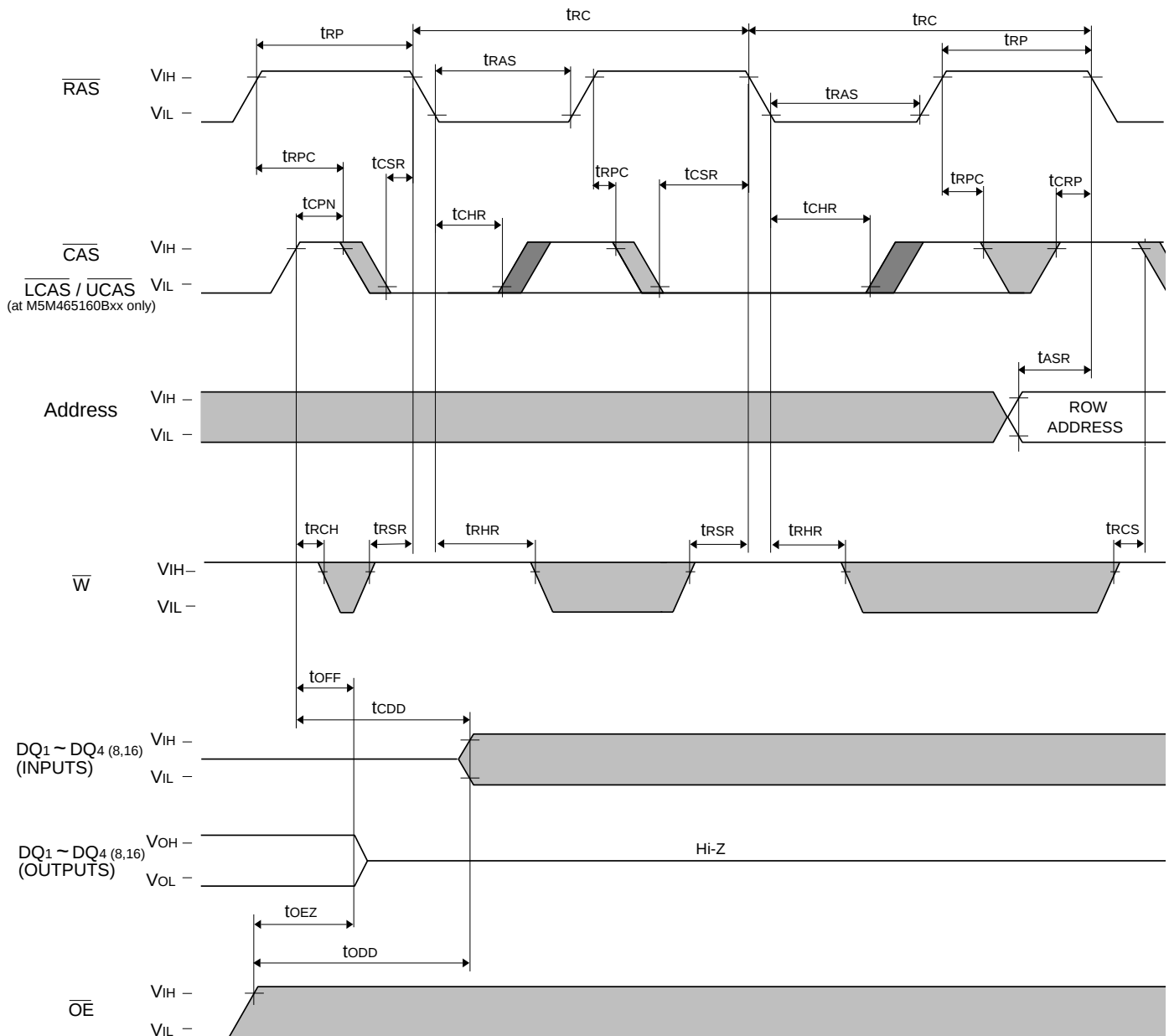
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

RAS-only Refresh Cycle

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
 FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
 FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

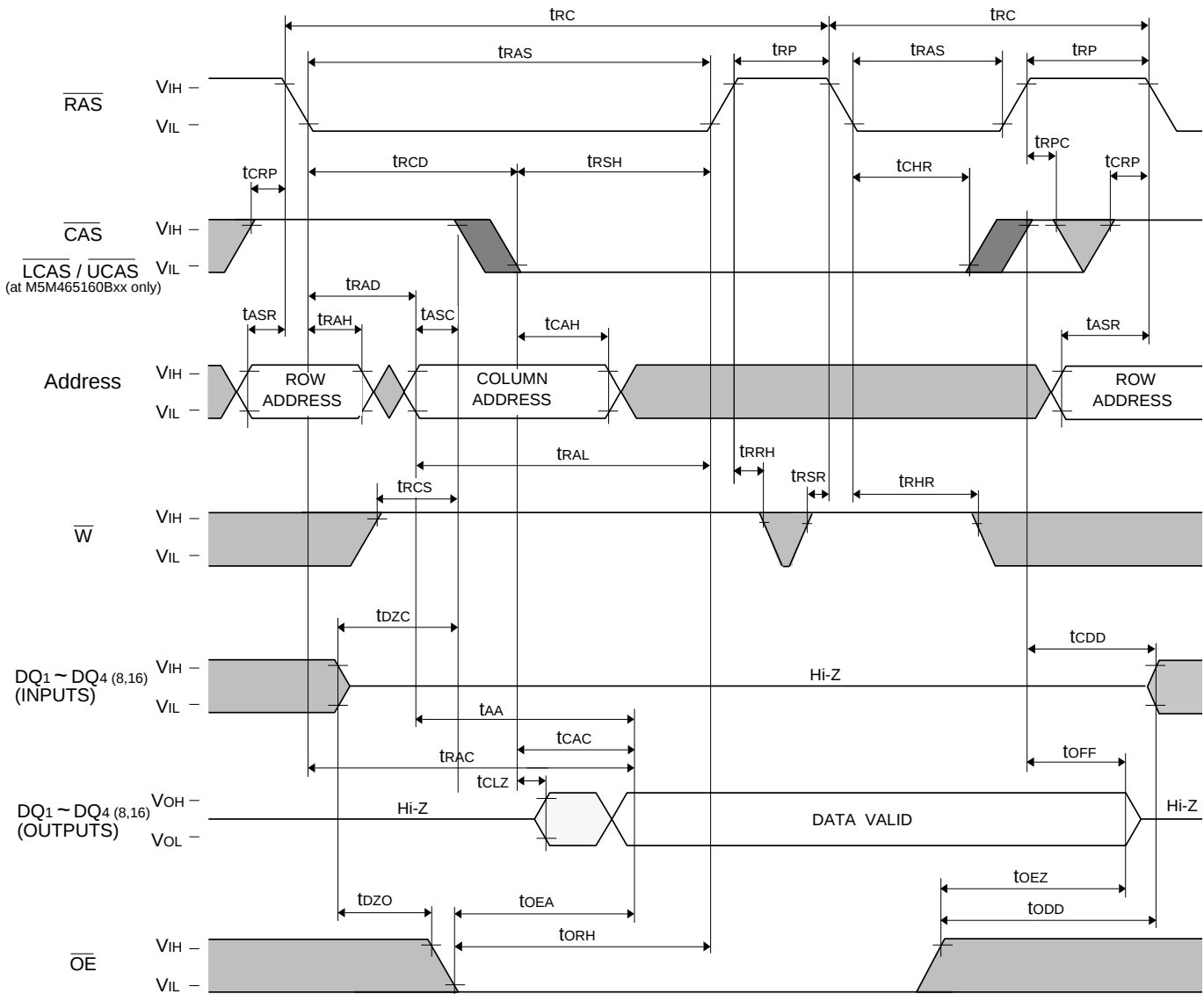
CAS before RAS Refresh Cycle



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 29)

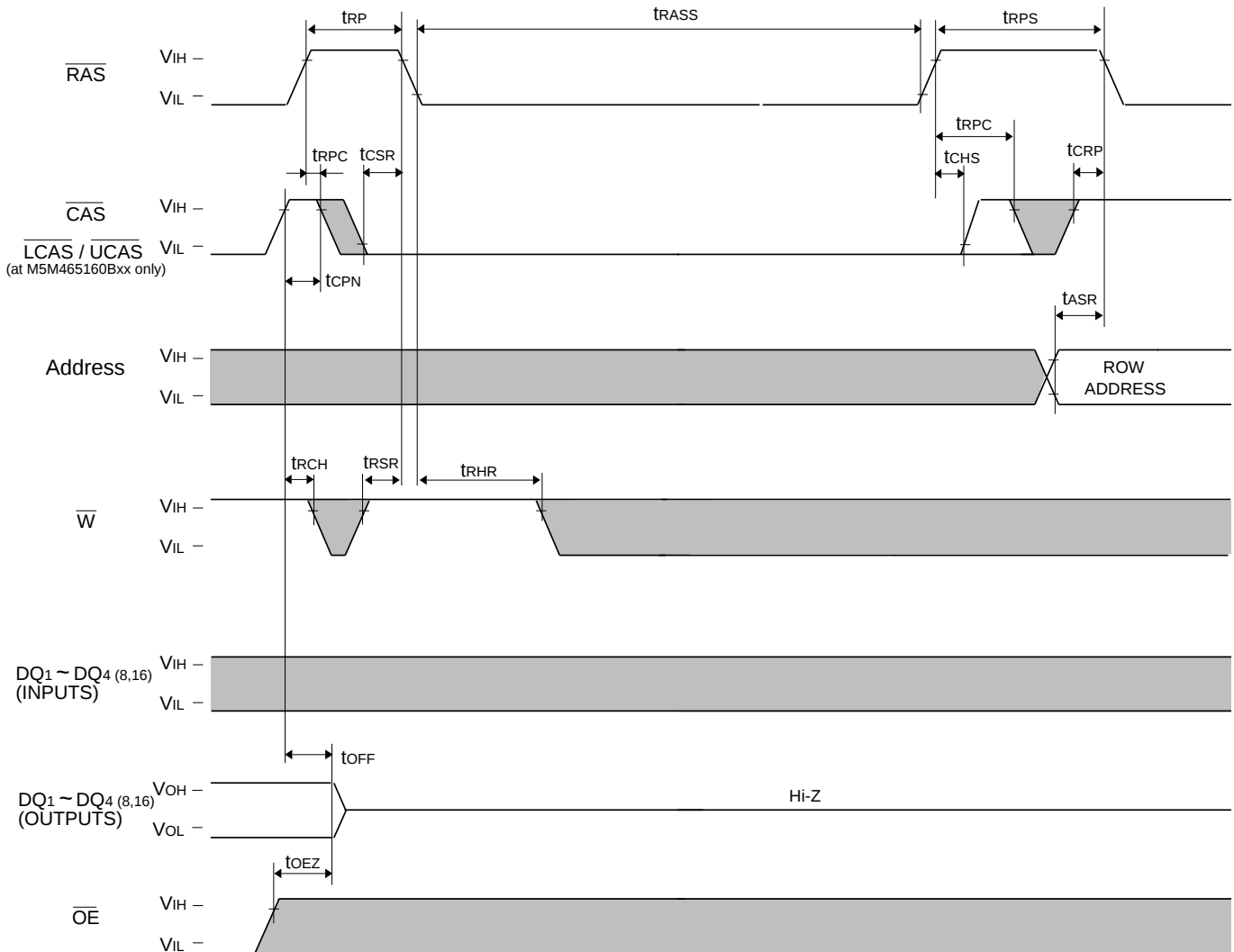


Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

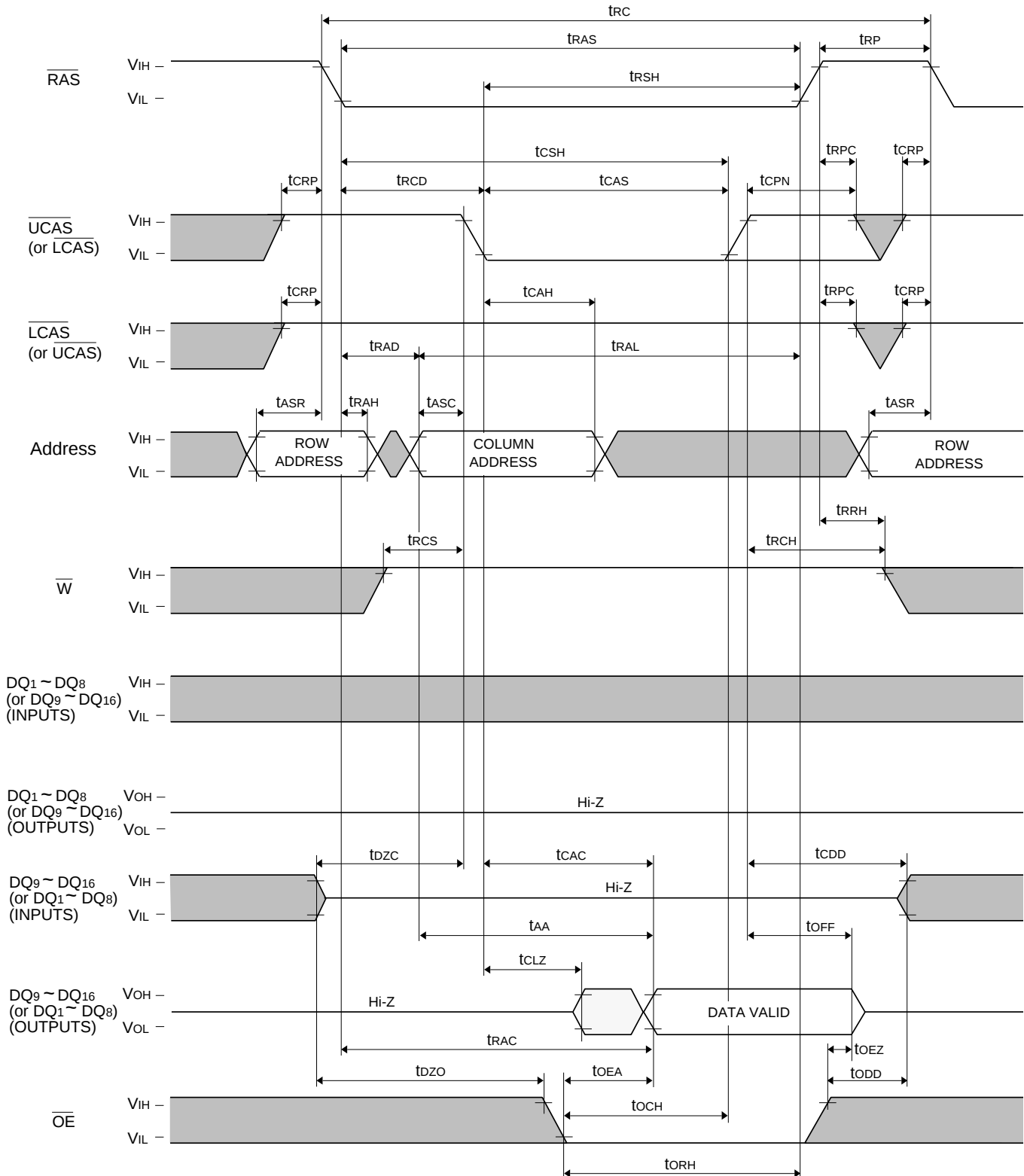
Self Refresh Cycle



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

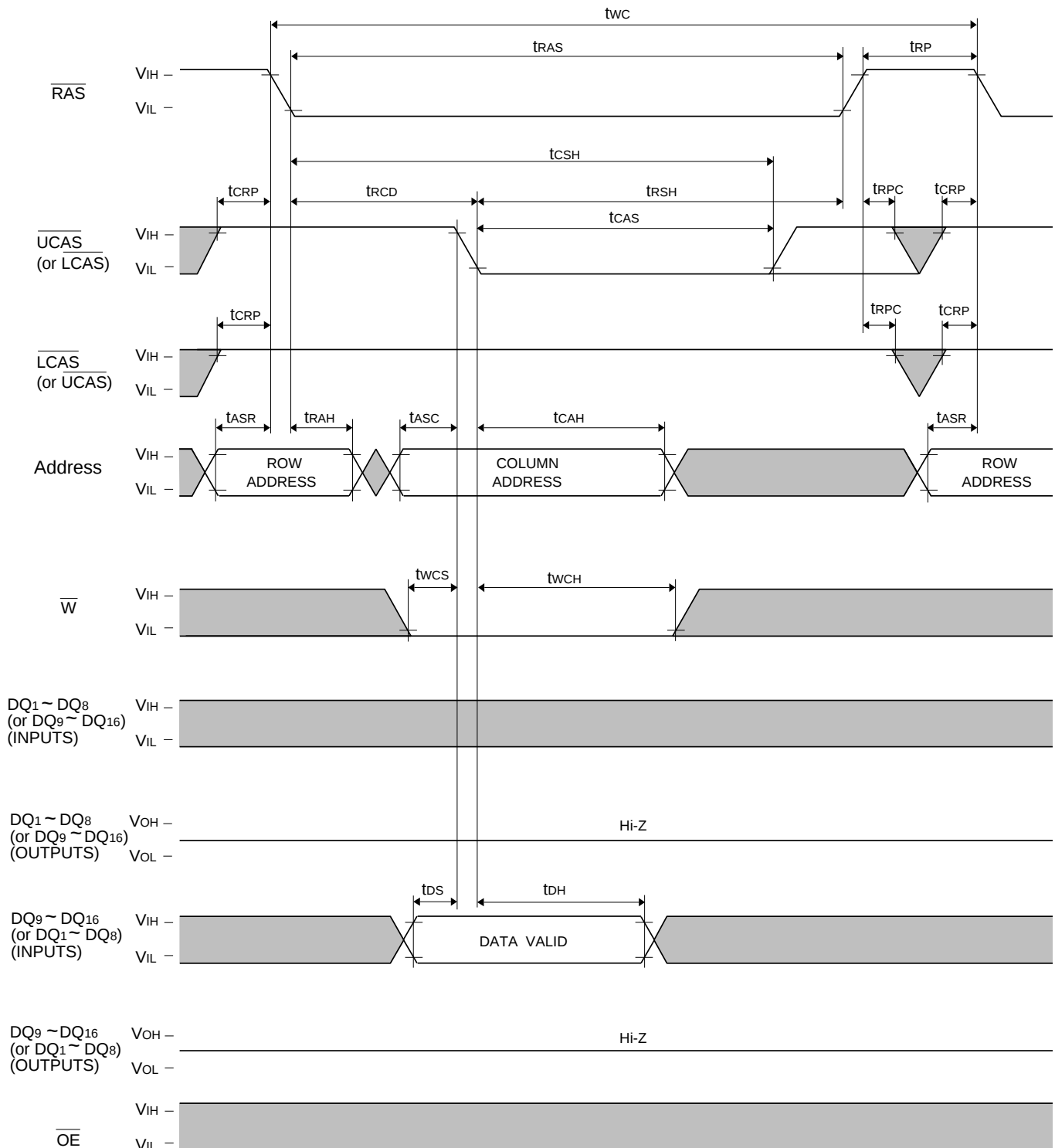
Upper / (Lower) Byte Read Cycle (at M5M465160Bxx only)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

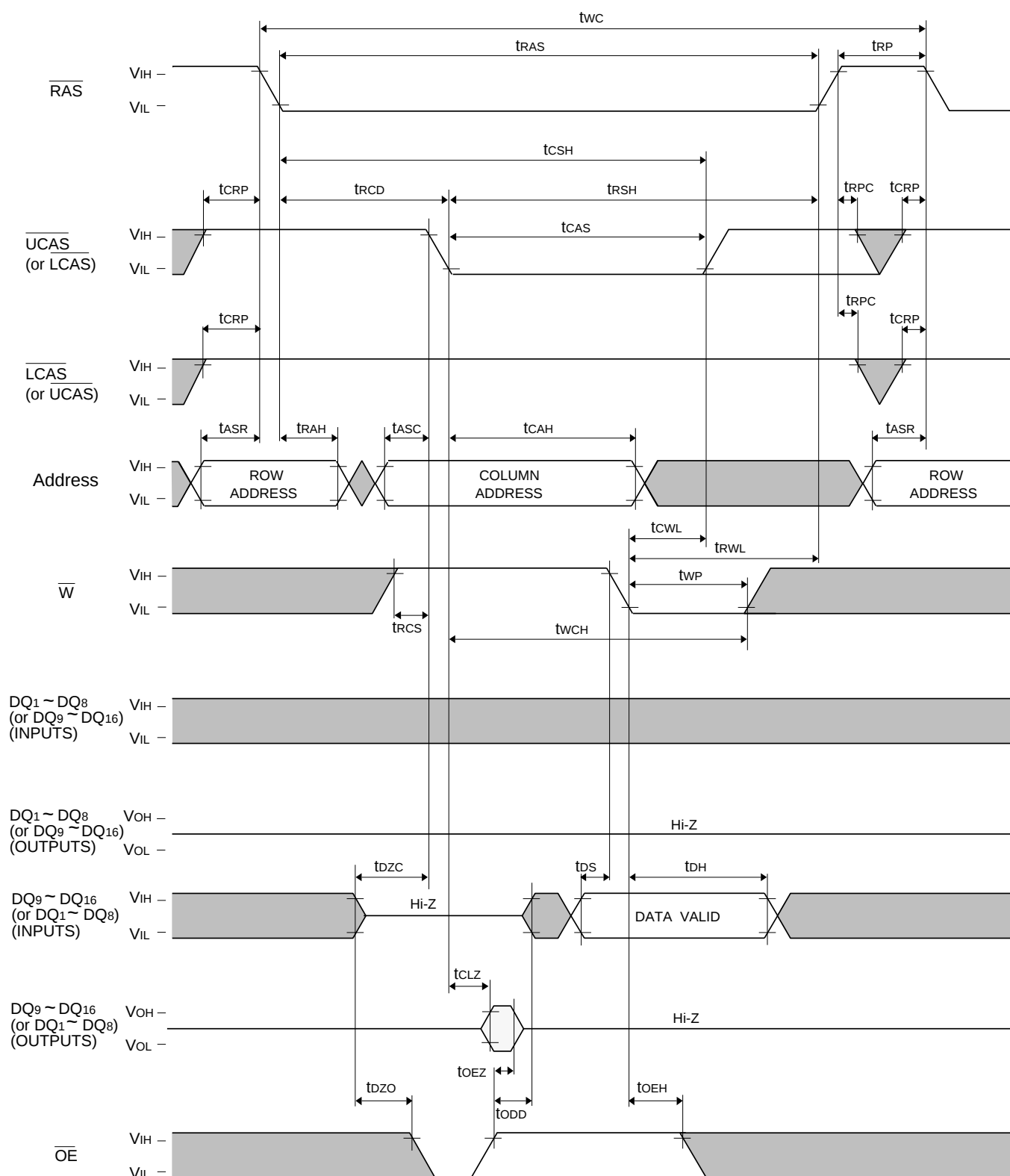
FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) Byte Write Cycle (Early Write) (at M5M465160Bxx only)



FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

(at M5M465160Bxx only)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

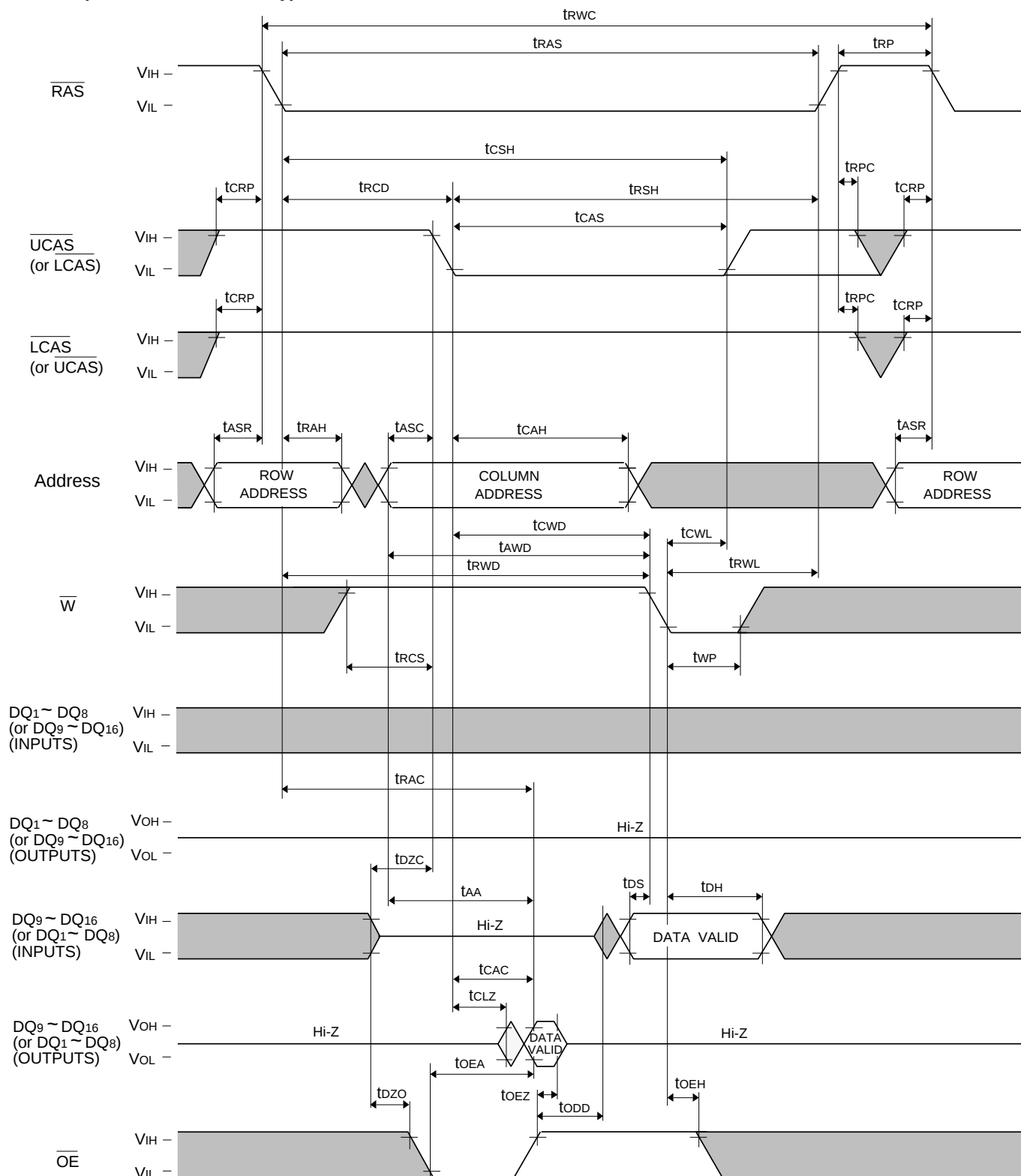
FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Byte Read-Write, Upper/(Lower) Byte Read-Modify-Write Cycle

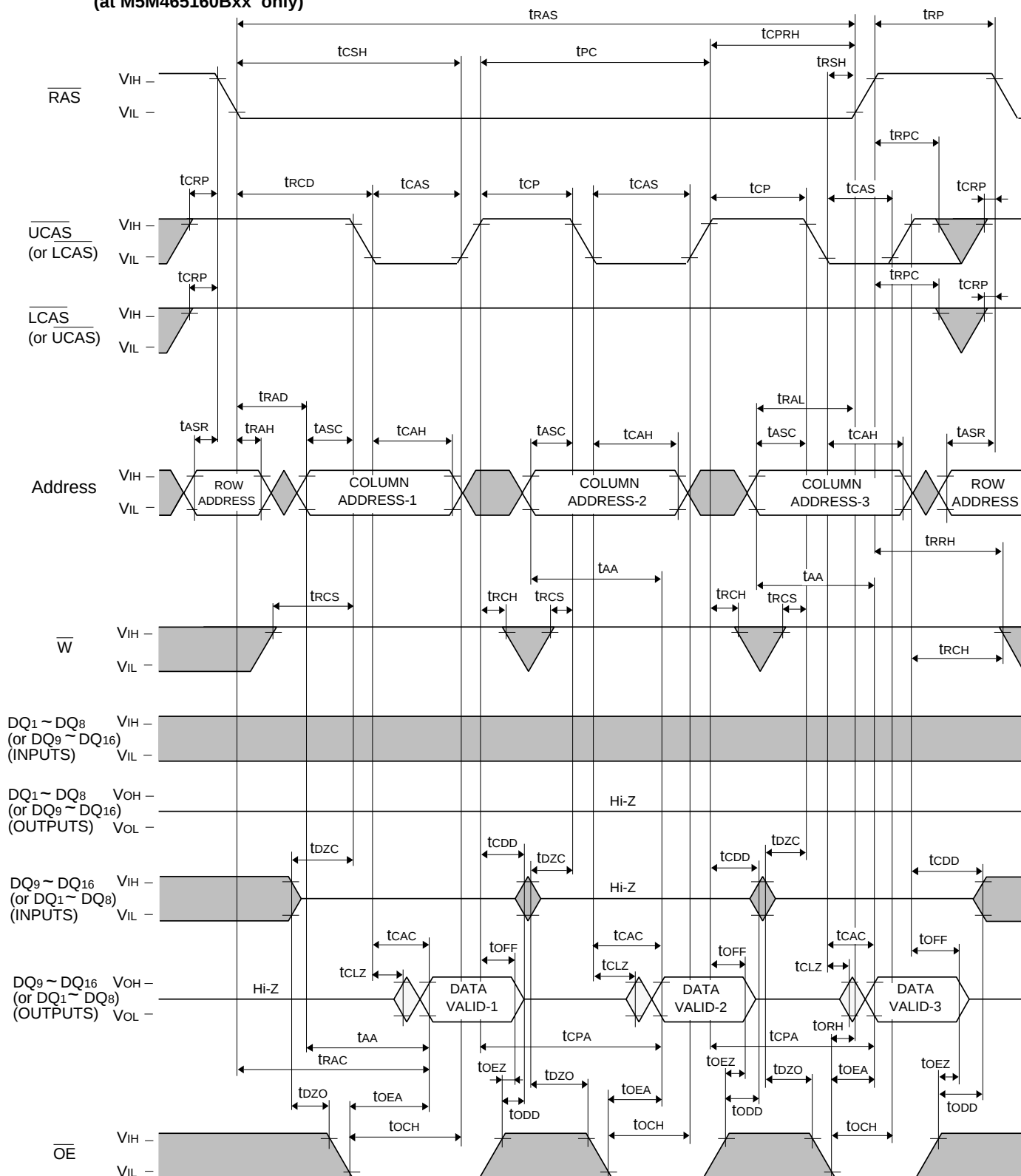
(at M5M465160Bxx only)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper / (Lower) Byte Read Cycle (at M5M465160Bxx only)

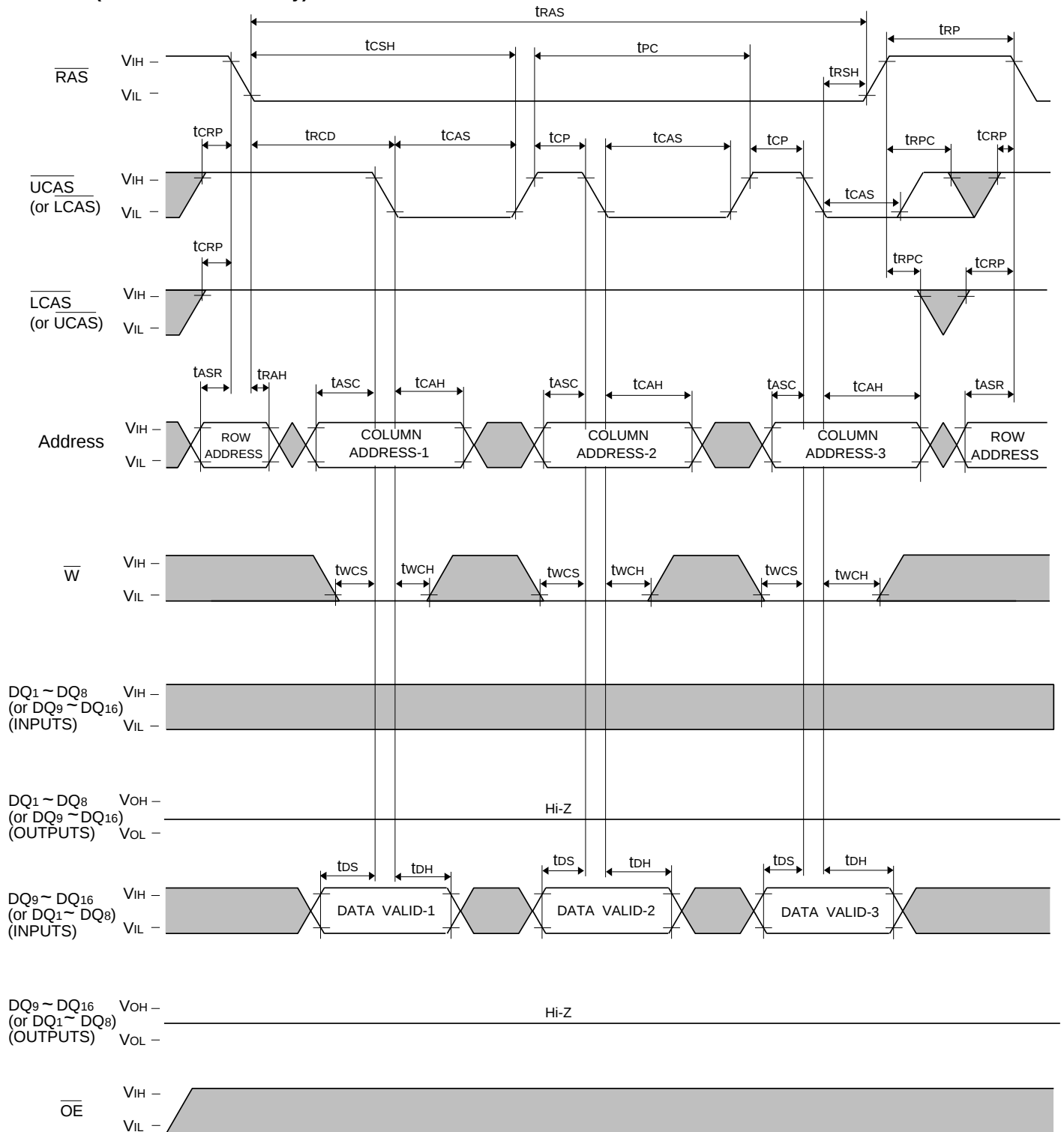


M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper / (Lower) Byte Write Cycle (Early Write)

(at M5M465160Bxx only)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

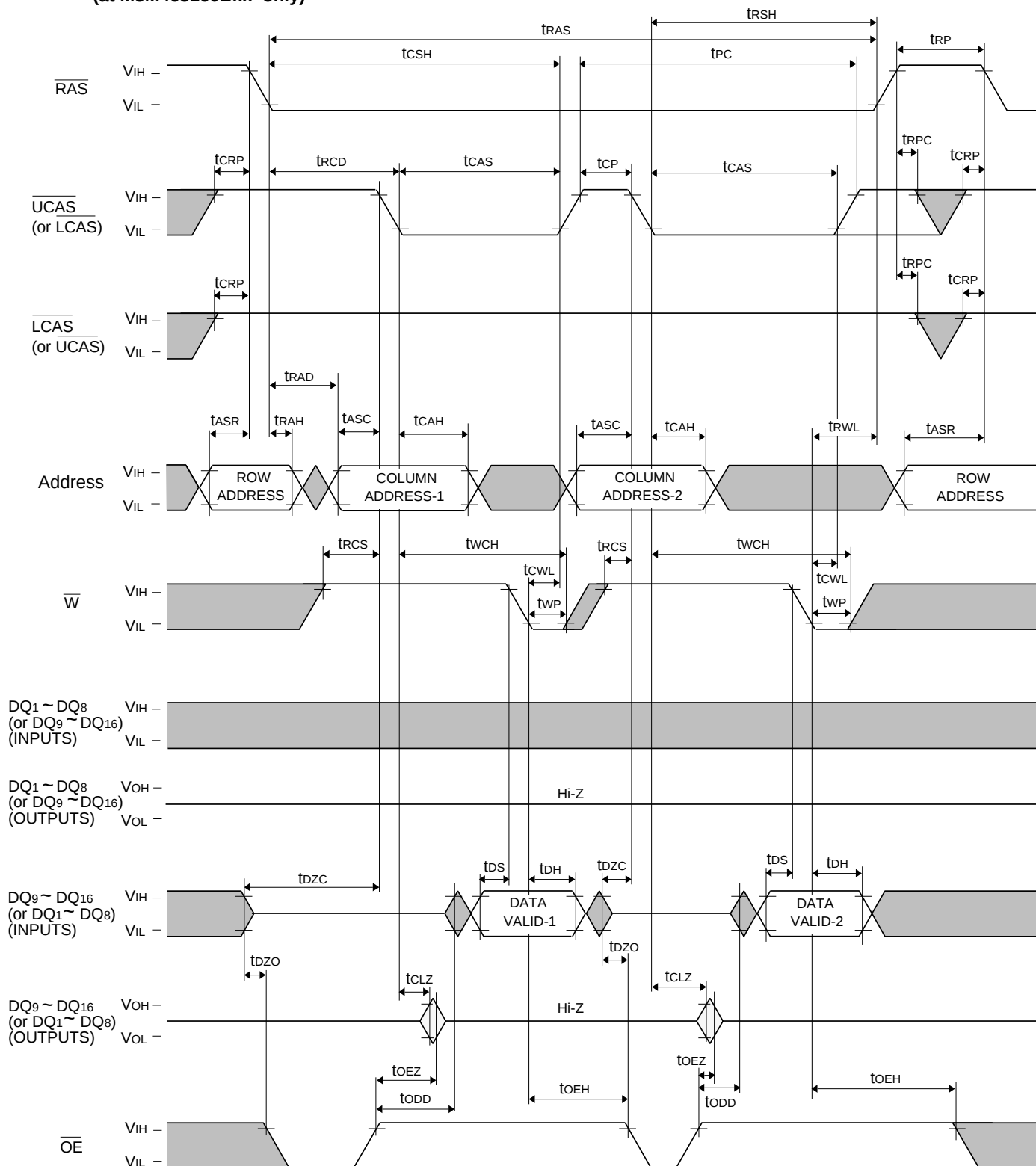
FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper / (Lower) Byte Write Cycle (Delayed Write)

(at M5M465160Bxx only)



FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

The timing diagram illustrates the relationship between various signals and their timing parameters. The signals shown are:

- VIH, VIL:** Input voltage levels.
- V_{SS}:** Ground reference.
- DATA VALID-1, DATA VALID-2:** Data bus signals.
- Hi-Z:** High-impedance state.
- VOH, VOL:** Output voltage levels.

The timing parameters are defined as follows:

- t_{AS}:** Address setup time.
- t_{CSH}:** Column address setup time.
- t_{CRP}:** Column address rise/fall time.
- t_{CD}:** Column address delay time.
- t_{CAS}:** Column address access time.
- t_{CP}:** Column address pulse width.
- t_{PRWC}:** Precharge to write clock time.
- t_{RPC}:** Row address pulse width.
- t_{TRP}:** Row address setup time.
- t_{TRSH}:** Row address setup time.
- t_{TRPC}:** Row address rise/fall time.
- t_{ASR}:** Address setup time.
- t_{RAH}:** Row address hold time.
- t_{ASC}:** Row address setup time.
- t_{CAH}:** Column address hold time.
- t_{AD}:** Address delay time.
- t_{AWD}:** Address width delay time.
- t_{AWL}:** Address width limit time.
- t_{AWD}:** Address width delay time.
- t_{AWL}:** Address width limit time.
- t_{CPA}:** Column address pulse width.
- t_{AA}:** Address access time.
- t_{DS}:** Data setup time.
- t_{DH}:** Data hold time.
- t_{DZC}:** Data zero current time.
- t_{CAC}:** Column address access time.
- t_{AC}:** Address access time.
- t_{DO}:** Data output delay time.
- t_{CLZ}:** Data output delay time.
- t_{OEZ}:** Output enable delay time.
- t_{ODD}:** Output delay time.
- t_{OEH}:** Output enable hold time.

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

The timing diagram illustrates the operational sequence of the 64K1602S memory device. It shows the relationship between the Row Address Strobe (RAS), Column Address Strobe (UCAS/LCAS), Write Enable (W), and data outputs (Q1~Q8 and Q9~Q16) over time. Key timing parameters are defined as follows:

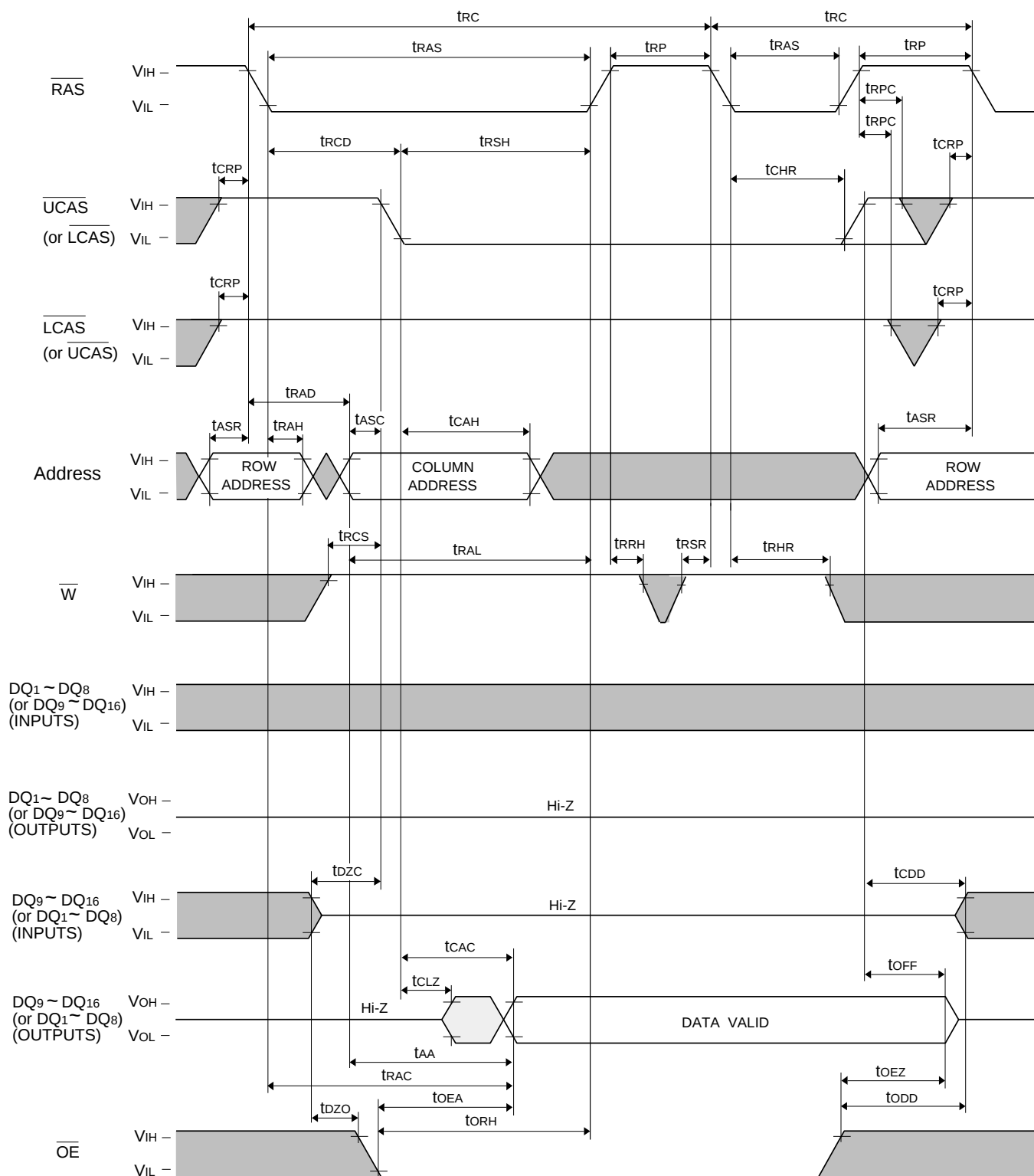
- tRP**: RAS pulse width.
- tRC**: RAS to column address delay.
- tRAS**: RAS to data output delay.
- tRPC**: RAS to column address delay (for UCAS/LCAS).
- tCSR**: RAS to column address delay (for UCAS/LCAS).
- tCHR**: RAS to column address delay (for UCAS/LCAS).
- tCPN**: RAS to column address delay (for UCAS/LCAS).
- tCRP**: RAS to column address delay (for UCAS/LCAS).
- tASR**: RAS to column address delay (for UCAS/LCAS).
- tRCH**: RAS to column address delay (for UCAS/LCAS).
- tRSR**: RAS to column address delay (for UCAS/LCAS).
- tRHR**: RAS to column address delay (for UCAS/LCAS).
- tRCS**: RAS to column address delay (for UCAS/LCAS).
- tOEZ**: Output enable delay.
- tCDD**: Output data delay.
- tOFF**: Output data delay.
- tODD**: Output data delay.
- tOE**: Output enable delay.

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM

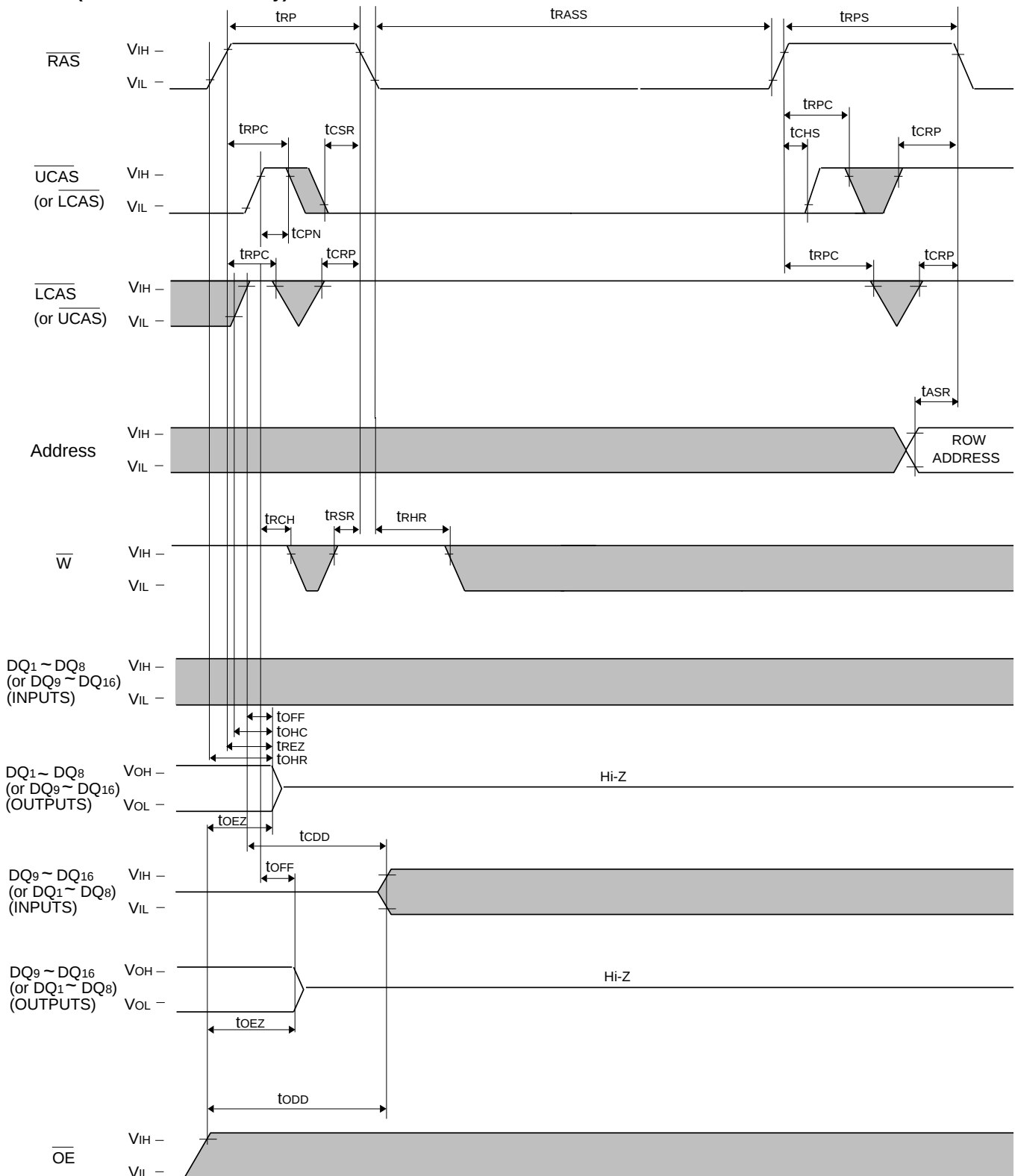
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Upper / (Lower) Hidden Refresh Cycle (Byte Read) (Note 29)**(at M5M465160Bxx only)**

M5M467400/465400BJ,BTP -5,-6,-5S,-6S M5M467800/465800BJ,BTP -5,-6,-5S,-6S M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM
FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

Byte Self Refresh Cycle (at M5M465160Bxx only)



M5M467400/465400BJ,BTP -5,-6,-5S,-6S
M5M467800/465800BJ,BTP -5,-6,-5S,-6S
M5M465160BJ,BTP -5,-6,-5S,-6S

FAST PAGE MODE 67108864-BIT (16777216-WORD BY 4-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (8388608-WORD BY 8-BIT) DYNAMIC RAM

FAST PAGE MODE 67108864-BIT (4194304-WORD BY 16-BIT) DYNAMIC RAM

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