SMALL-OUTLINE SDRAM MODULE

MT4LSDT464(L)H, MT8LSDT864(L)H, MT8LSDT1664(L)H

For the latest full-length data sheet, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard 144-pin, small-outline, dual in-line memory module (SODIMM)
- Utilizes 100 MHz and 125 MHz SDRAM components
- Nonbuffered
- 32MB (4 Meg x 64), 64MB (8 Meg x 64) and 128MB (16 Meg x 64)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode: Standard and Low Power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial presence-detect (SPD)

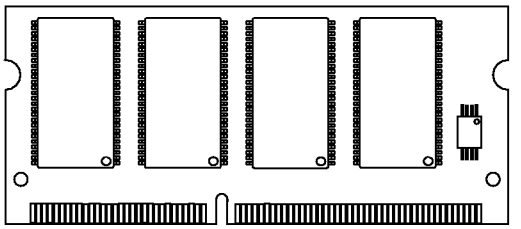
OPTIONS — MARKING

- Self Refresh Current
  - Standard — None
  - Low power — L
- Package
  - 144-pin SODIMM (gold) — G
- Frequency/CAS Latency
  - 100 MHz/CL = 2 (8ns, 125 MHz SDRAMs) — -10E
  - 100 MHz/CL = 3 (8ns, 125 MHz SDRAMs) — -10C
  - 66 MHz/CL = 2 (10ns, 100 MHz SDRAMs) — -662
- Module Height
  - 1.15" (32MB, 66 MHz, SS*) — -662_1
  - 1.00" (32MB, 66 MHz, DS*) — -662_2
  - 1.05" (64MB/128MB, 66 MHz, DS*) — -662_3
  - 1.25" (32MB/64MB/128MB, 100 MHz, DS*) — -10__5**
  - 1.00" (32MB/64MB, 100 MHz, DS*) — -10__3**

* SS = Single Sided, DS = Double Sided.
** Adheres to PC100 SODIMM rev. 1.0 specification.

PIN ASSIGNMENT (Front View)

144-Pin Small-Outline DIMM (32MB)



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	VSS	2	VSS	73	DNU	74	CK1
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	VDD	46	VDD	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	VSS	140	VSS
69	S0#	70	RFU (A12)	141	SDA	142	SCL
71	S1#	72	RFU (A13)	143	VDD	144	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-10E	-8E	2	6ns	2ns	1ns
-10C	-8C	3	6ns	2ns	1ns
-662	-10	2	9ns	2ns	1ns

PART NUMBERS

PART NUMBER	CONFIGURATION	VERSION
MT4LSDT464HG-10E__	4 Meg x 64	100 MHz, CL = 2
MT4LSDT464HG-10C__	4 Meg x 64	100 MHz, CL = 3
MT4LSDT464HG-662__	4 Meg x 64	66 MHz, CL = 2
MT4LSDT464LHG-10E__	4 Meg x 64*	100 MHz, CL = 2
MT4LSDT464LHG-10C__	4 Meg x 64*	100 MHz, CL = 3
MT4LSDT464LHG-662__	4 Meg x 64*	66 MHz, CL = 2
MT8LSDT864HG-10E__	8 Meg x 64	100 MHz, CL = 2
MT8LSDT864HG-10C__	8 Meg x 64	100 MHz, CL = 3
MT8LSDT864HG-662__	8 Meg x 64	66 MHz, CL = 2
MT8LSDT864LHG-10E__	8 Meg x 64*	100 MHz, CL = 2
MT8LSDT864LHG-10C__	8 Meg x 64*	100 MHz, CL = 3
MT8LSDT864LHG-662__	8 Meg x 64*	66 MHz, CL = 2
MT8LSDT1664HG-10E__	16 Meg x 64	100 MHz, CL = 2
MT8LSDT1664HG-10C__	16 Meg x 64	100 MHz, CL = 3
MT8LSDT1664HG-662__	16 Meg x 64	66 MHz, CL = 2
MT8LSDT1664LHG-10E__	16 Meg x 64*	100 MHz, CL = 2
MT8LSDT1664LHG-10C__	16 Meg x 64*	100 MHz, CL = 3
MT8LSDT1664LHG-662__	16 Meg x 64*	66 MHz, CL = 2

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT8LSDT864HG-10EB5.

*Low power option.

GENERAL DESCRIPTION

The Micron® MT4LSDT464(L)H, MT8LSDT864(L)H and MT8LSDT1664(L)H are high-speed CMOS, dynamic random-access, 32MB, 64MB and 128MB memories organized in a x64 configuration. These modules use SDRAMs that are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK1). Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

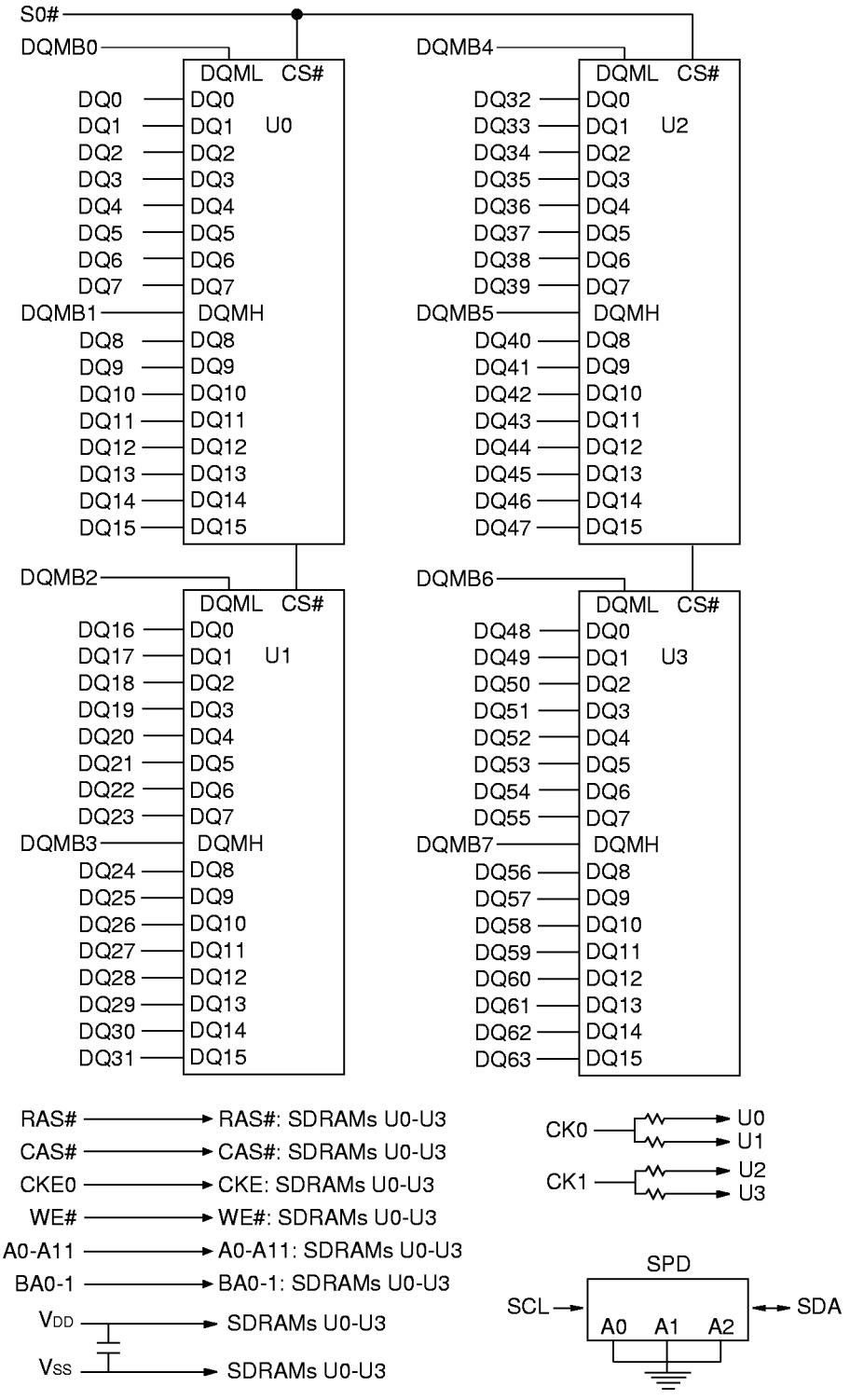
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals.

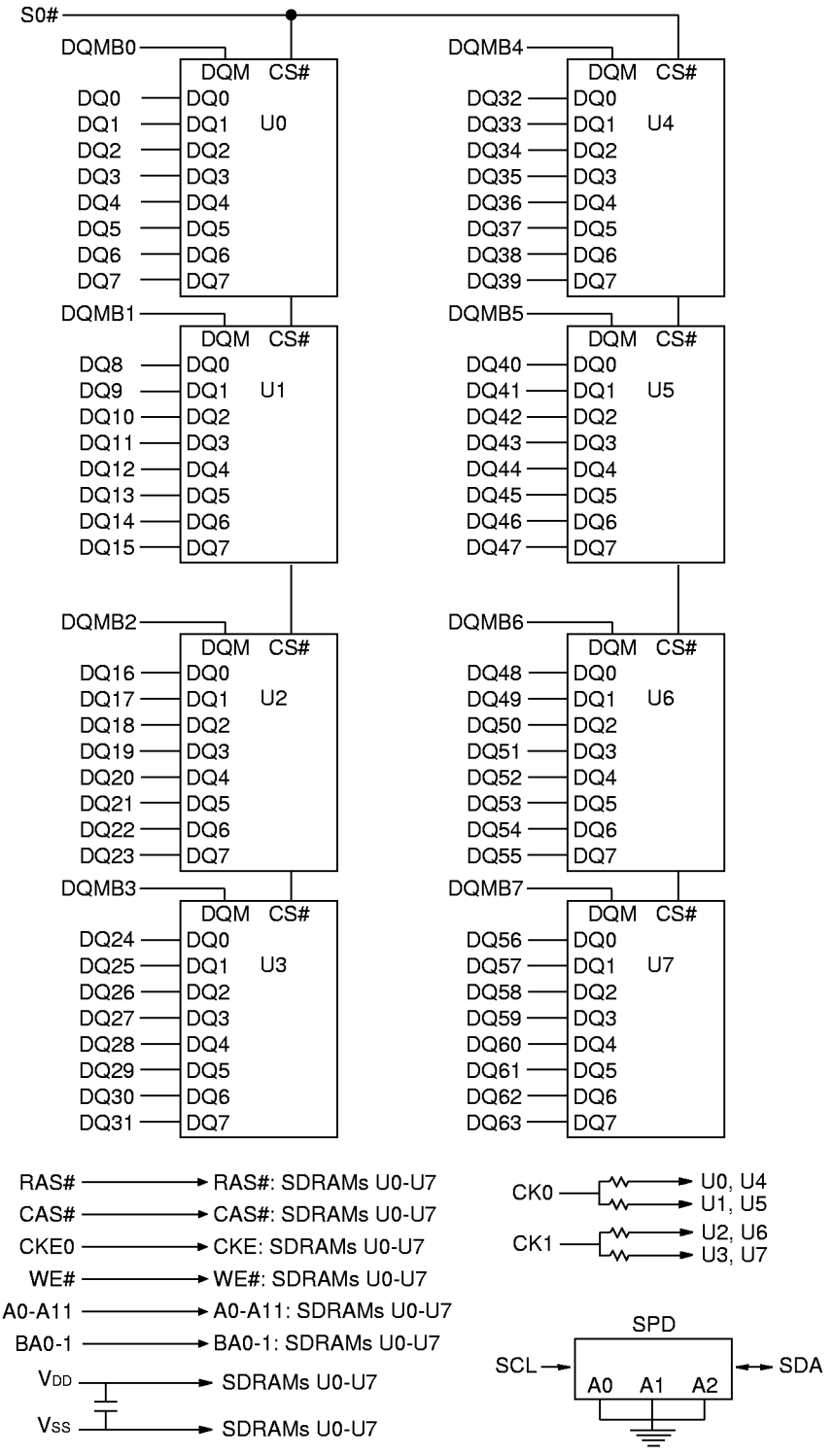
FUNCTIONAL BLOCK DIAGRAM
MT4LSDT464(L)H (32MB, 66 MHz)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC4M16A2TG SDRAMs

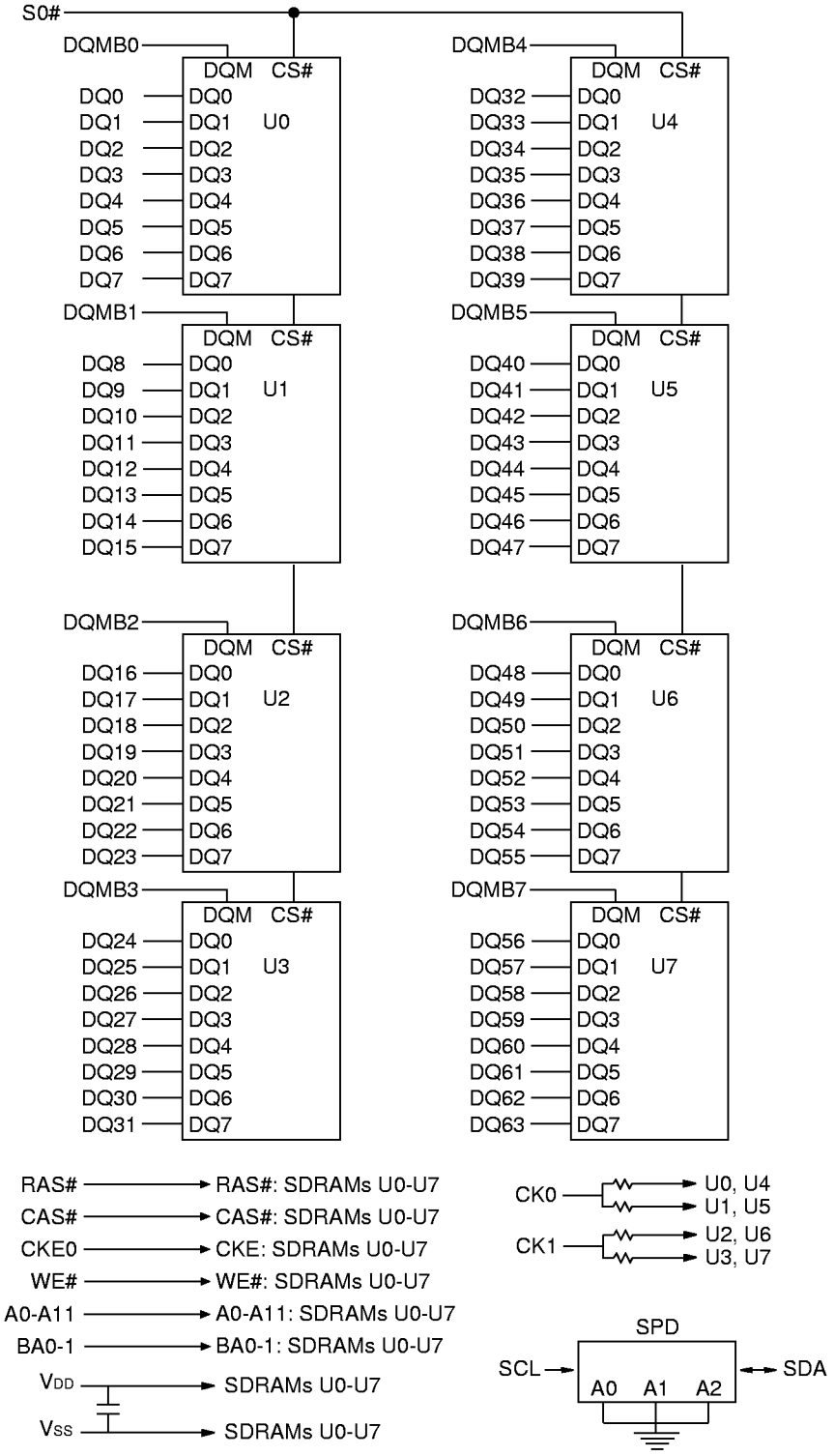
FUNCTIONAL BLOCK DIAGRAM
MT8LSDT864(L)H (64MB, 66 MHz)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC8M8A2TG SDRAMs

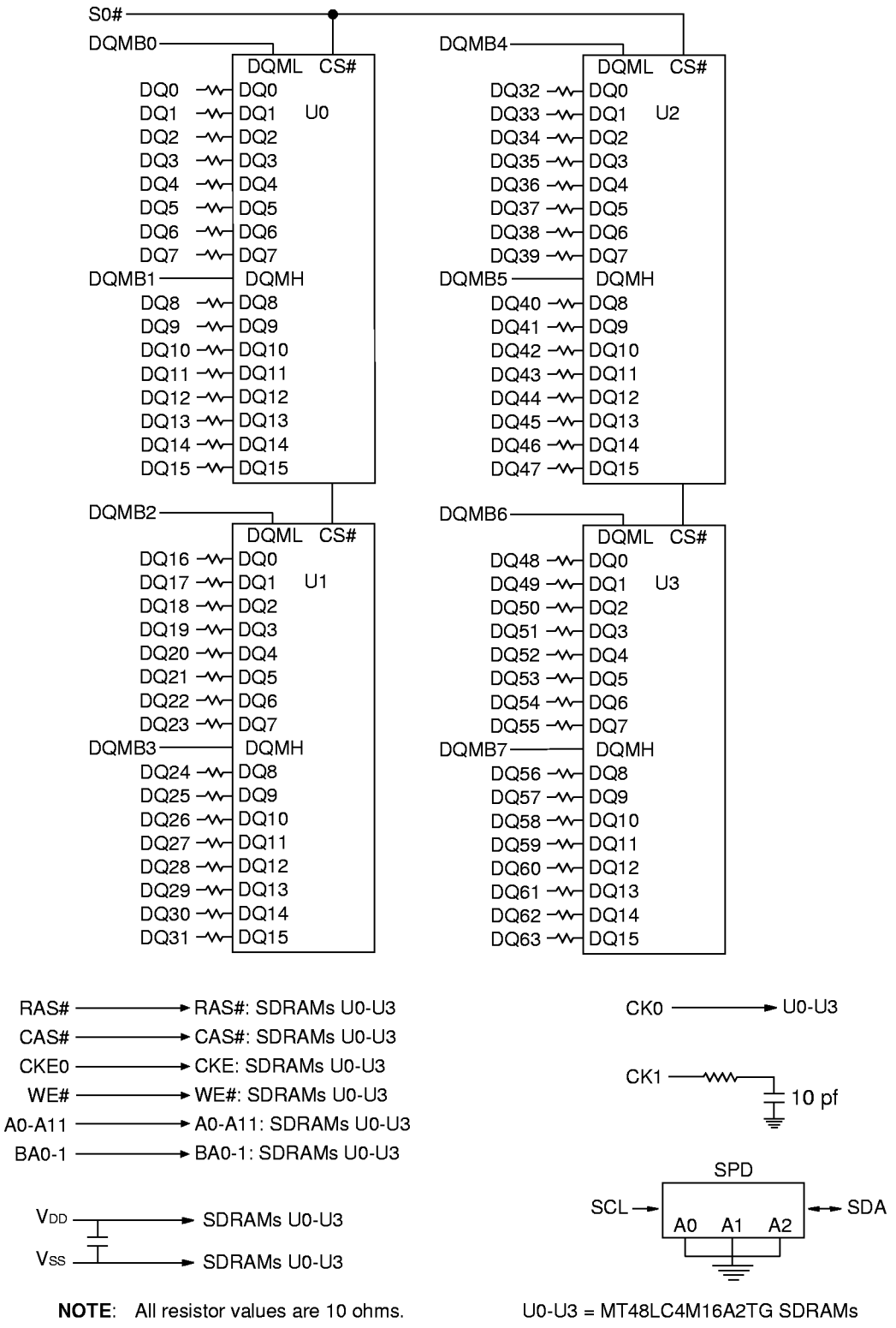
FUNCTIONAL BLOCK DIAGRAM
MT8LSDT1664(L)H (128MB, 66 MHz)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC16M8A2TG SDRAMs

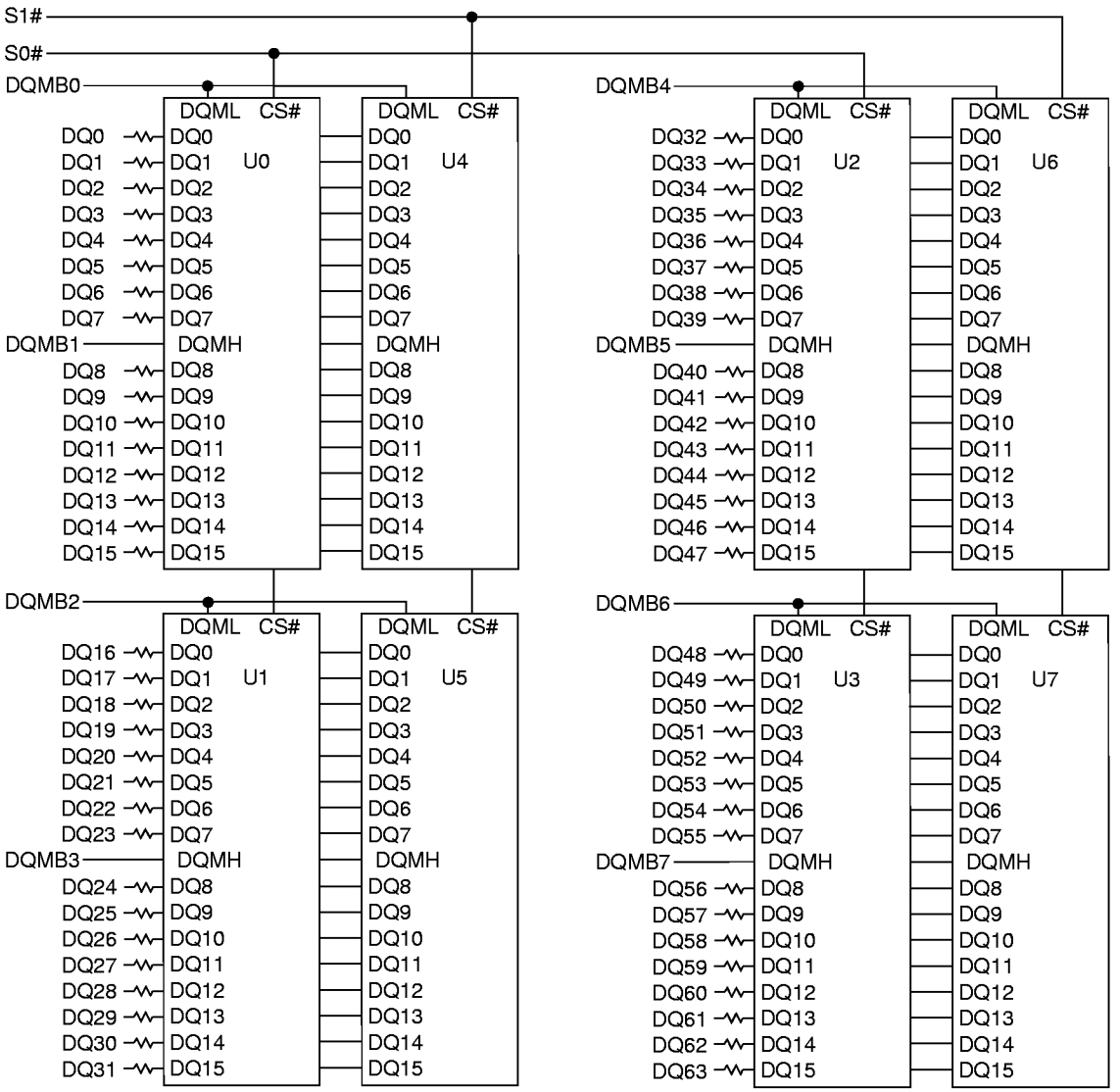
FUNCTIONAL BLOCK DIAGRAM
MT4LSDT464(L)H (32MB, 100 MHz)



NOTE: All resistor values are 10 ohms.

U0-U3 = MT48LC4M16A2TG SDRAMs

FUNCTIONAL BLOCK DIAGRAM
MT8LSDT864(L)H / MT8LSDT1664(L)H (64MB / 128MB, 100 MHz)



NOTE: All resistor values are 10 ohms.

U0-U7 = MT48LC4M16A2TG SDRAMs (64MB)
U0-U7 = MT48LC8M16A2TG SDRAMs (128MB)

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
65-67	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S0#) define the command being entered.
61, 74	CK0, CK1	Input	Clock: CK0 and CK1 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
62, 68	CKE0, CKE1	Input	Clock Enable: CKE0 and CKE1 activates (HIGH) and deactivates (LOW) the CK0-CK1 signals. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 and CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0 and CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-CK1, are disabled during power-down and self refresh modes, providing low standby power.
69, 71	S0#, S1#	Input	Chip Select: S0# and S1# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# and S1# are registered HIGH. S0# and S1# are considered part of the command code.
23-26, 115-118	DQMB0-DQMB7	Input	Input Mask: DQMB is an input mask signal for write accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
106, 110	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 is also used to program the twelfth bit of the Mode Register.
29-34, 103-105, 109, 111, 112	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A7/A8/A9, with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
3-10, 13-20, 37-44, 47-54, 83-90, 93-100, 121-128, 131-138	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
11, 12, 27, 28, 45, 46, 63, 64, 81, 82, 101, 102, 113, 114, 129, 130, 143, 144	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 2, 21, 22, 35, 36, 55, 56, 75, 76, 91, 92, 107, 108, 119, 120, 139, 140	Vss	Supply	Ground.
141	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
142	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
70, 72	RFU	–	Reserved for Future Use: These pins should be left unconnected.
73	DNU	–	Do Not Use: This pin is not connected on these modules but is an assigned pin on the compatible DRAM version.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

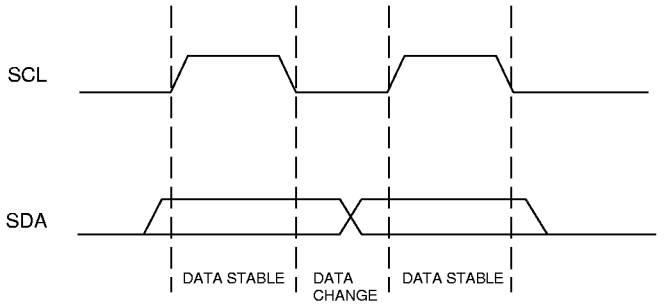


Figure 1
DATA VALIDITY

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

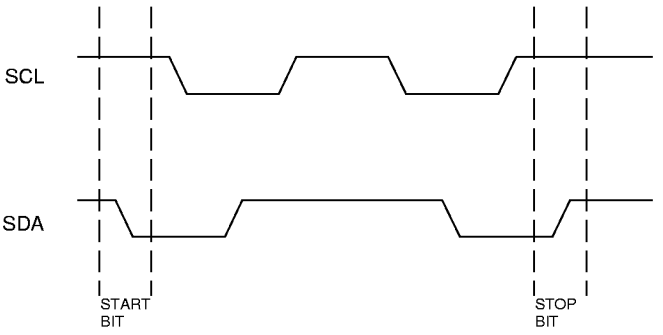


Figure 2
DEFINITION OF START AND STOP

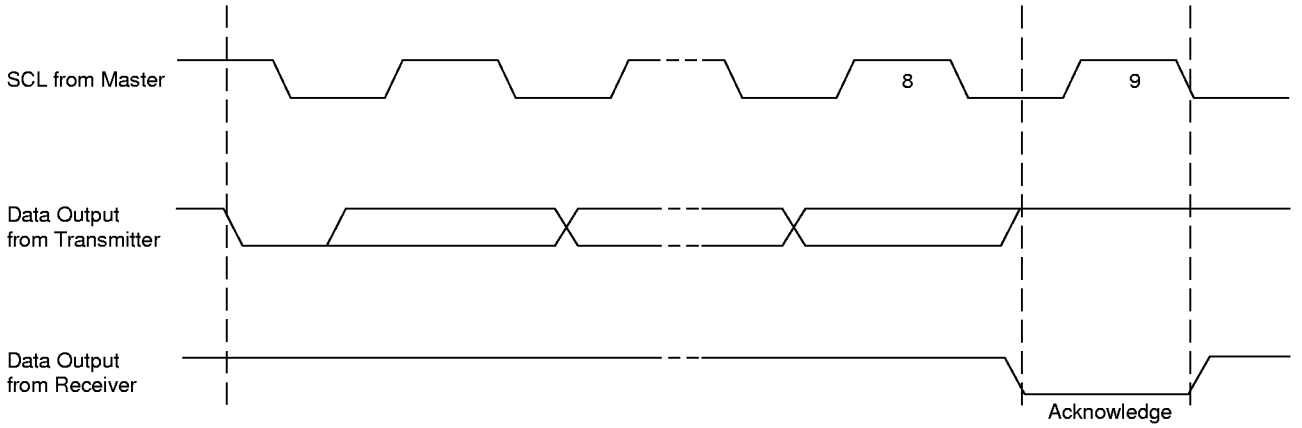


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY	MT4LSDT464(L)H	MT8LSDT864(L)H	MT8LSDT1664(L)H
0	NUMBER OF BYTES USED BY MICRON	128	80h	80h	80h
1	TOTAL NUMBER OF SPD BYTES	256	08h	08h	08h
2	MEMORY TYPE	SDRAM	04h	04h	04h
3	NUMBER OF ROW ADDRESSES	12	0Ch	0Ch	0Ch
4	NUMBER OF COLUMN ADDRESSES				
	-10E/C	8 or 9	8 (08h)	8 (08h)	9 (09h)
	-662	8 or 9 or 10	8 (08h)	9 (09h)	10 (0Ah)
5	NUMBER OF BANKS PER MODULE				
	-10E/C	1 or 2	1 (01h)	2 (02h)	2 (02h)
	-662	1	01h	01h	01h
6	MODULE DATA WIDTH	x64	40h	40h	40h
7	MODULE DATA WIDTH (continued)	0	00h	00h	00h
8	MODULE VOLTAGE INTERFACE LEVEL	LVTTL	01h	01h	00h
9	SDRAM CYCLE TIME (CL = 3), ^{t}CK				
	-10E/C	8ns	80h	80h	80h
	-662	10ns	A0h	A0h	A0h
10	SDRAM ACCESS (CL = 3), ^{t}AC				
	-10E/C	6ns	60h	60h	60h
	-662	7.5ns	75h	75h	75h
11	MODULE CONFIGURATION TYPE	NONPARITY	00h	00h	00h
12	REFRESH RATE/TYPE	15.6µs/SELF	80h	80h	80h
13	SDRAM WIDTH (PRIMARY SDRAM)				
	-10E/C	x16	10h	10h	10h
	-662	x8 or x16	16 (10h)	8 (08h)	8 (08h)
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE	00h	00h	00h
15	MINIMUM CLOCK DELAY, ^{t}CCD	1	01h	01h	01h
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE	8Fh	8Fh	8Fh
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04h	04h	04h
18	CAS LATENCIES SUPPORTED	2, 3	06h	06h	06h
19	CS LATENCY	0	01h	01h	01h
20	WE LATENCY	0	01h	01h	01h
21	SDRAM MODULE ATTRIBUTES	NONBUFFERED	00h	00h	00h
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0Eh	0Eh	0Eh
23	SDRAM CYCLE TIME (CL = 2), ^{t}CK				
	-10E	10ns	A0h	A0h	A0h
	-10C	12ns	C0h	C0h	C0h
	-662	15ns	F0h	F0h	F0h
24	SDRAM ACCESS TIME (CL = 2), ^{t}AC				
	-10E	6ns	60h	60h	60h
	-10C/-662	9ns	90h	90h	90h
25	SDRAM CYCLE TIME (CL = 1), ^{t}CK	–	00h	00h	00h
26	SDRAM ACCESS TIME (CL = 1), ^{t}AC	–	00h	00h	00h
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP				
	-10E/C	20ns	14h	14h	14h
	-662	30ns	1Eh	1Eh	1Eh
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	20ns	14h	14h	14h

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY	MT4LSDT464(L)H	MT8LSDT864(L)H	MT8LSDT1664(L)H
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD				
	-10E/C	20ns	14h	14h	14h
	-662	30ns	1Eh	1Eh	1Eh
30	MINIMUM RAS# PULSE WIDTH, ^{t}RAS				
	-10E/C	50ns	32h	32h	32h
	-662	60ns	3Ch	3Ch	3Ch
31	MODULE BANK DENSITY				
	-10E/C	32 or 64	32MB (08h)	32MB (08h)	64MB (10h)
	-662	32 or 64 or 128	32MB (08h)	64MB (10h)	128MB (20h)
32	COMMAND/ADDRESS INPUT SETUP, ^{t}AS, ^{t}CMS				
	-10E/C	2ns	20h	20h	20h
	-662	0	00h	00h	00h
33	COMMAND/ADDRESS INPUT HOLD, ^{t}AH, ^{t}CMH				
	-10E/C	1ns	10h	10h	10h
	-662	0	00h	00h	00h
34	DATA SIGNAL INPUT SETUP, ^{t}DS				
	-10E/C	2ns	20h	20h	20h
	-662	0	00h	00h	00h
35	DATA SIGNAL INPUT HOLD, ^{t}DH				
	-10E/C	1ns	10h	10h	10h
	-662	0	00h	00h	00h
36-61	RESERVED BYTES	0	00h	00h	00h
62	SPD REVISION				
	-10E/C	1.2	12h	12h	12h
	-662	1.0	01h	01h	01h
63	CHECKSUM FOR BYTES 0-62				
	-10E		E4h	E5h	EEh
	-10C		34h	35h	3Eh
	-662		46h	47h	58h
64	MANUFACTURER'S JEDEC ID CODE	Micron	2Ch	2Ch	2Ch
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)		FFh	FFh	FFh
72	MANUFACTURING LOCATION				
		1	01h	01h	01h
		2	02h	02h	02h
		3	03h	03h	03h
		4	04h	04h	04h
		5	05h	05h	05h
		6	06h	06h	06h
73-90	MICRON PART NUMBER WITHOUT "MT" (LEFT JUSTIFIED ASCII) PAD WITH 20h		xx	xx	xx
91	PCB IDENTIFICATION CODE				
	-10E/C		03h	05h	05h
	-662		02h	03h	03h
92	IDENTIFICATION CODE (CONTINUED)	1, 2, 4, 8, PAGE	8Fh	8Fh	8Fh
93	YEAR OF MANUFACTURE IN BCD		xx	xx	xx
94	WEEK OF MANUFACTURE IN BCD		xx	xx	xx

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY	MT4LSDT464(L)H	MT8LSDT864(L)H	MT8LSDT1664(L)H
95-98	MODULE SERIAL NUMBER		xx	xx	xx
99-125	RESERVED (MANUFACTURER-SPECIFIC DATA)		–	–	–
126	SYSTEM FREQUENCY				
	-10E/C	100 MHz	64h	64h	64h
	-662	66 MHz	66h	66h	66h
127	SDRAM COMPONENT AND CLOCK DETAIL				
	-10E		8Fh	CFh	CFh
	-10C		8Dh	CDh	CDh
	-662		06h	06h	06h

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

COMMANDS

Truth Table 1 provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 64Mb: x4, x8, x16 SDRAM data sheet.

TRUTH TABLE 1 – Commands and DQMB Operation

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter Self Refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A11 define the op-code written to the Mode Register.
3. A0-A11 provide row address and BA0, BA1 determine which bank is made active.
4. A0-A7 (32MB, 66/100 MHz; 64MB, 100 MHz), A0-A8 (64MB, 66 MHz; 128MB, 100 MHz), A0-A9 (128MB, 66 MHz) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: all banks are precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

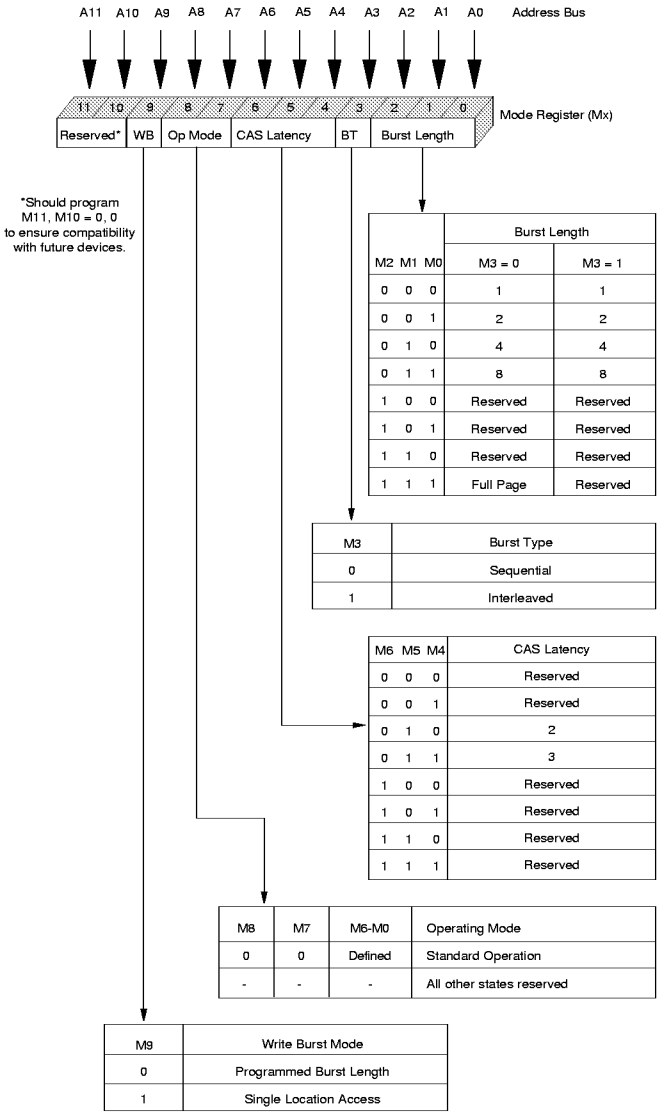


Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A7/8/9 (location 0-y)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... …Cn-1, Cn…	Not supported

NOTE:
1. For full-page accesses: y = 256 (32MB, 66/100 MHz; 64MB, 100 MHz); y = 512 (64MB, 66MHz; 128MB, 100 MHz); y = 1,024 (128MB, 66 MHz).
2. For a burst length of two, A1-A7/8/9 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A7/8/9 select the block-of-four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A7/8/9 select the block-of-eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected, and A0-A7/8/9 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A7/8/9 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +125°C
Power Dissipation 8W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	CK0-CK1	I_{I1}	-20	20	µA	22
	S0#, S1#, CKE0, CKE1, RAS#, CAS#, A0-A11, BA0-BA1, WE#	I_{I2}	-40	40	µA	22
	DQMB0-DQMB7	I_{I3}	-5	5	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	DQ0-DQ63	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)		V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)		V_{OL}	–	0.4	V	

IDD SPECIFICATIONS AND CONDITIONS

(Notes: 1, 6, 11, 13) (V_{DD} = +3.3V ±0.3V)

				MAX			
PARAMETER/CONDITION		SYMBOL	SIZE (MB)	-10E/C	-662	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; tRC = tRC (MIN); CAS latency = 3		I_{DD1}	32 64 128	380 520 760	360 720 1,040	mA	3, 18, 19, 30
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		I_{DD2}	32 64 128	8 16 16	12 24 16	mA	30
STANDBY CURRENT: Active Mode; S0# = HIGH; CKE = HIGH; All banks active after tRCD met; No accesses in progress		I_{DD3}	32 64 128	140 280 320	120 240 400	mA	3, 12, 19, 30
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		I_{DD4}	32 64 128	480 620 760	420 840 1,120	mA	3, 18, 19, 30
AUTO REFRESH CURRENT: CKE = HIGH; S0# = HIGH	tRC = tRC (MIN); CL = 3	I_{DD5}	32 64 128	760 900 1,000	680 1,360 1,600	mA	3, 12, 18, 19, 30
	tRC = 15.625µs; CL = 3	I_{DD6}	32 64 128	160 300 380	140 280 360	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	Standard	I_{DD7}	32 64 128	4 8 12	8 16 16	mA	4
	Low power (L)	I_{DD7}	32 64 128	2 4 6.4	2 4 6.4	mA	

CAPACITANCE (66 MHz)

		32MB		64MB		128MB			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#, S0#, CKE0	C_{I1}	12	22	22	42	22	42	pF	2
Input Capacitance: CK0, CK1	C_{I2}	7	10	12	18	12	18	pF	2
Input Capacitance: DQMB0#-DQMB7#	C_{I3}	4	8	4	8	4	8	pF	2
Input Capacitance: SCL	C_{I4}	–	6	–	6	–	6	pF	2
Input/Output Capacitance: DQ0-DQ63, SDA	C_{IO}	6	10	6	10	6	10	pF	2

CAPACITANCE (100 MHz)

		32MB		64MB		128MB			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#	C_{I1}	12	22	22	42	22	42	pF	2
Input Capacitance: CKE0, CKE1, S0#, S1#	C_{I2}	12	22	12	22	12	22	pF	2
Input Capacitance: CK0, CK1	C_{I3}	12	18	12	18	12	18	pF	2
Input Capacitance: DQMB0#-DQMB7#	C_{I4}	4	8	7	12	7	12	pF	2
Input Capacitance: SCL	C_{I5}	–	6	–	6	–	6	pF	2
Input/Output Capacitance: DQ0-DQ63, SDA	C_{IO}	6	10	10	16	10	16	pF	2

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

AC CHARACTERISTICS			-10E		-10C		-662			
PARAMETER		SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	^{t}AC		6		6		7.5	ns	
	CL = 2	^{t}AC		6		9		9	ns	29
Address hold time		^{t}AH	1		1		1		ns	
Address setup time		^{t}AS	2		2		2		ns	
CLK high-level width		^{t}CH	3		3		3		ns	
CLK low-level width		^{t}CL	3		3		3		ns	
Clock cycle time	CL = 3	^{t}CK	8		8		10		ns	25
	CL = 2	^{t}CK	10		12		15		ns	25, 29
CKE hold time		^{t}CKH	1		1		1		ns	
CKE setup time		^{t}CKS	2		2		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	2		2		2		ns	
Data-in hold time		^{t}DH	1		1		1		ns	
Data-in setup time		^{t}DS	2		2		2		ns	
Data-out high-impedance time	CL = 3	^{t}HZ		6		6		8	ns	10
	CL = 2	^{t}HZ		7		7		10	ns	10
Data-out low-impedance time		^{t}LZ	1		1		2		ns	
Data-out hold time (load)		^{t}OH	3		3		3		ns	
Data-out hold time (no load)		$^{t}OH_{N}$	1.8		1.8		n/a		ns	32
ACTIVE to PRECHARGE command		^{t}RAS	50	120,000	50	120,000	60	120,000	ns	
ACTIVE to ACTIVE command period		^{t}RC	70		70		90		ns	29
Auto refresh period		^{t}RCAR	70		70		90		ns	
ACTIVE to READ or WRITE delay		^{t}RCD	20		20		30		ns	29
Refresh period (4,096 rows)		^{t}REF		64		64		64	ms	
PRECHARGE command period		^{t}RP	20		20		30		ns	21, 29
ACTIVE bank A to ACTIVE bank B command		^{t}RRD	20		20		20		ns	
Transition time		^{t}T	0.3	1.2	0.3	1.2	1	1.2	ns	7
WRITE recovery time		^{t}WR	1 CLK + 7ns		1 CLK + 7ns		1 CLK + 7ns		–	26
			15		15		15		ns	27
Exit SELF REFRESH to ACTIVE command		^{t}XSR	80		80		90		ns	20, 31

*Specifications for the SDRAM components used on the module.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

PARAMETER		SYMBOL	-10E	-10C	-662	UNITS	NOTES
READ/WRITE command to READ/WRITE command		tCCD	1	1	1	tCK	17
CKE to clock disable or power-down entry mode		tCKED	1	1	1	tCK	14
CKE to clock enable or power-down exit setup mode		tPED	1	1	1	tCK	14
DQM to input data delay		tDQD	0	0	0	tCK	17
DQM to data mask during WRITEs		tDQM	0	0	0	tCK	17
DQM to data high-impedance during READs		tDQZ	2	2	2	tCK	17
WRITE command to input data delay		tDWD	0	0	0	tCK	17
Data-in to ACTIVE command		tDAL	4	4	4	tCK	15, 21
Data-in to PRECHARGE command		tDPL	2	2	2	tCK	16, 21
Last data-in to burst STOP command		tBDL	1	1	1	tCK	17
Last data-in to new READ/WRITE command		tCDL	1	1	1	tCK	17
Last data-in to PRECHARGE command		tRDL	2	2	2	tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	2	tCK	28
Data-out to high-impedance from PRECHARGE command	CL = 3	tROH	3	3	3	tCK	17
	CL = 2	tROH	2	2	2	tCK	17

SDRAM COMPONENT* ELECTRICAL TIMING CHARACTERISTICS BETWEEN -8 SPEED OPTIONS

(Notes: 5, 6, 8, 9, 11)

AC CHARACTERISTICS			-8E		-8C			
PARAMETER		SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	tAC		6		6	ns	29
	CL = 2	tAC		6		9	ns	29
Clock cycle time	CL = 3	tCK	8		8		ns	29
	CL = 2	tCK	10		12		ns	29
ACTIVE to READ or WRITE delay		tRCD	20		20		ns	29
PRECHARGE command period		tRP	20		20		ns	29
AUTO REFRESH, ACTIVE command period		tRC	70		70		ns	29
WRITE recovery time		tWR	2		2		tCK	21
100 MHz Speed Reference (CL-tRCD-tRP)			2-2-2		3-2-2		CLKs	

*Specifications for the SDRAM components used on the module.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V	
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	$V_{DD} \times 0.3$	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V	
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA	
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA	
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA	

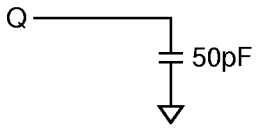
SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^{t}BUF	4.7		µs	
Data-out hold time	^{t}DH	300		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	4		µs	
Clock HIGH period	$^{t}HIGH$	4		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		100	ns	
Clock LOW period	^{t}LOW	4.7		µs	
SDA and SCL rise time	^{t}R		1	µs	
SCL clock frequency	^{t}SCL		100	KHz	
Data-in setup time	$^{t}SU:DAT$	250		ns	
Start condition setup time	$^{t}SU:STA$	4.7		µs	
Stop condition setup time	$^{t}SU:STO$	4.7		µs	
WRITE cycle time	^{t}WRC		10	ms	16

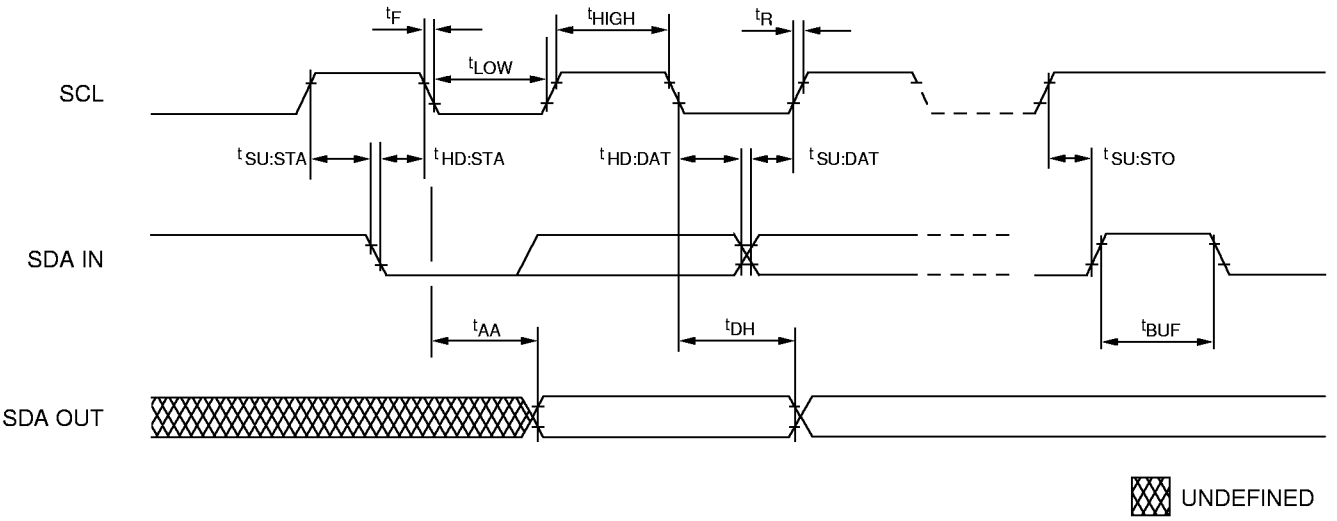
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 66 MHz (-662) or 100 MHz (-10E/C).
22. 32MB module values will be half of those shown.
23. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
24. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.
25. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
26. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 8ns after the first clock delay, after the last WRITE is executed.
27. Precharge mode only.
28. JEDEC and PC100 specify three clocks.
29. These five parameters vary between speed grades and define the differences between the -8 SDRAM speeds: -8C and -8E. All other -8 timing parameters remain constant.
30. ^{t}CK = 15ns for -662; ^{t}CK = 10ns for -10E/C.
31. ^{t}XSR = 70ns for -10E/C 128Mb-based modules.
32. Parameter guaranteed by design.

SPD EEPROM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

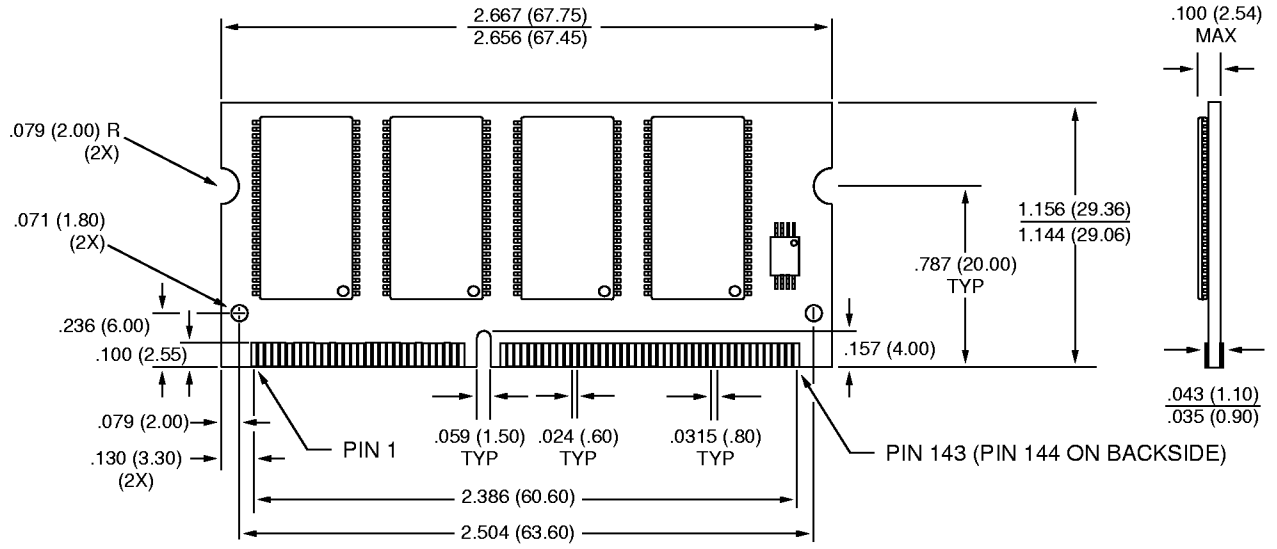
SYMBOL	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
tHIGH	4		µs
tLOW	4.7		µs
tR		1	µs
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs

144-PIN SODIMM

(32MB, 66 MHz)

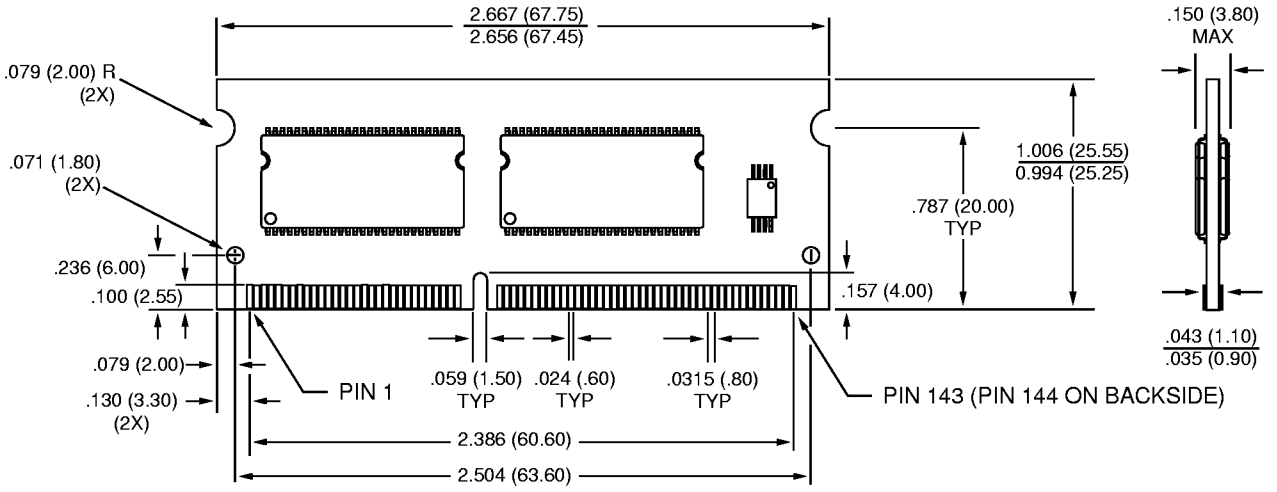
FRONT VIEW



144-PIN SODIMM

(32MB, 66 MHz)

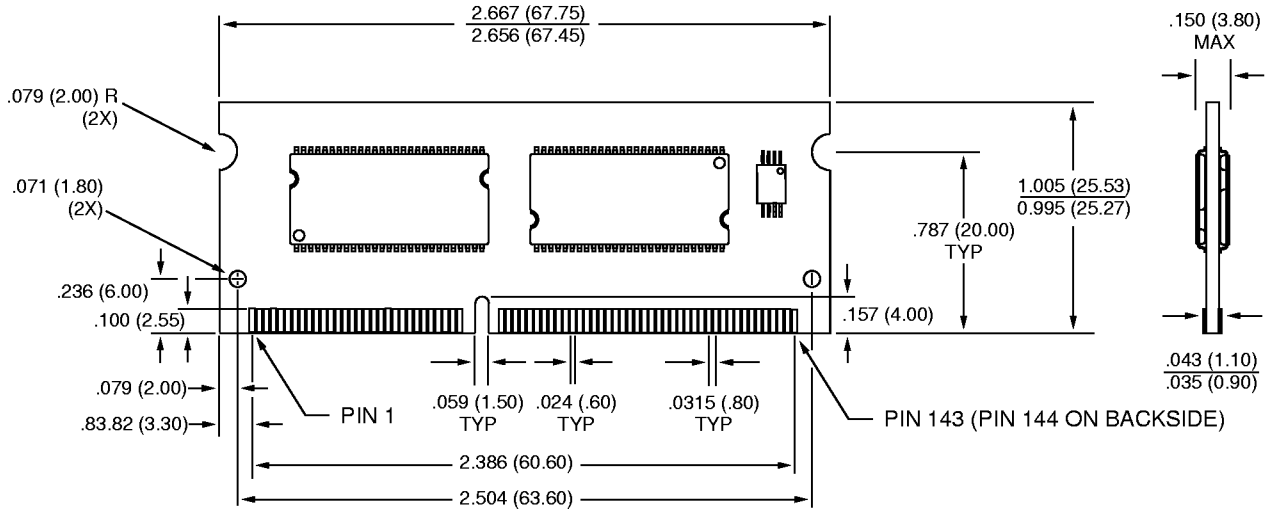
FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

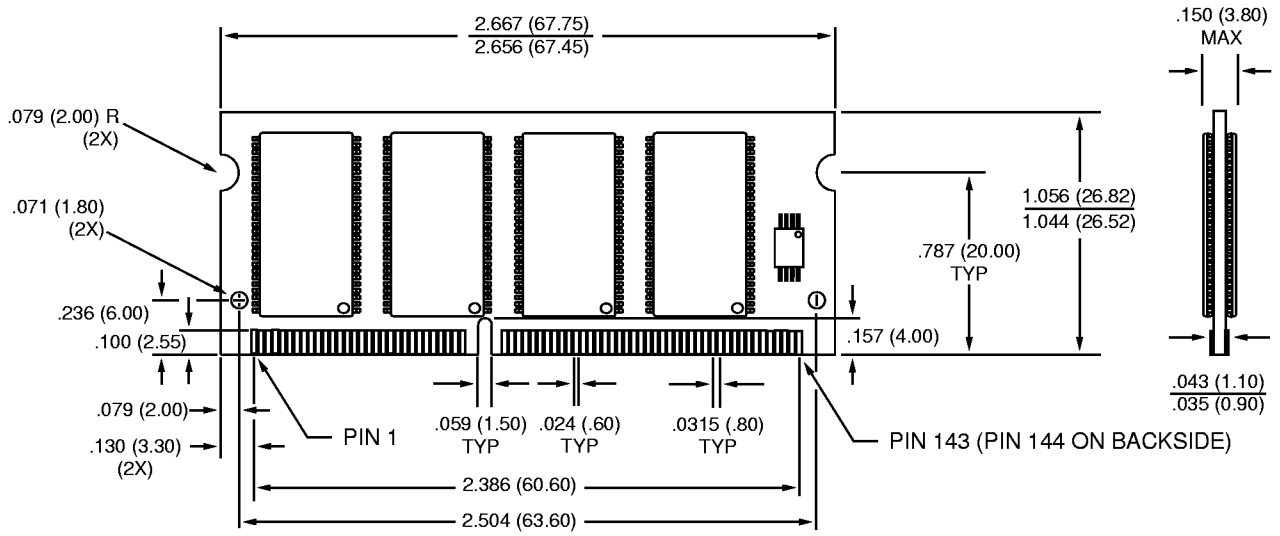
144-PIN SODIMM
(32MB, 100 MHz)

FRONT VIEW



144-PIN SODIMM
(64MB, 66 MHz)

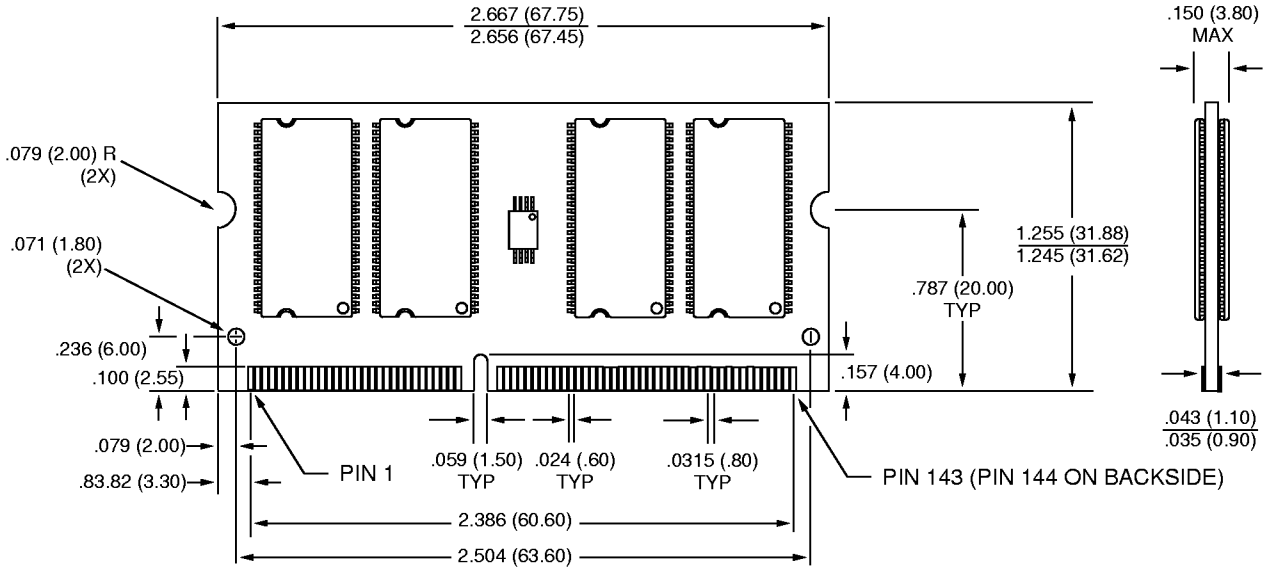
FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

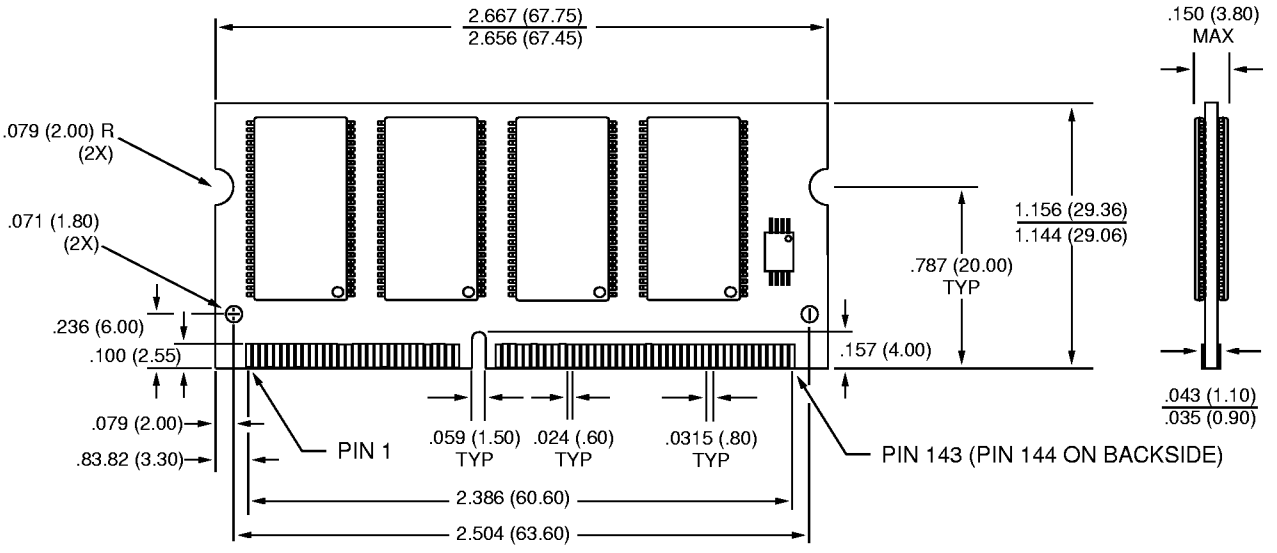
144-PIN SODIMM
(64MB, 100 MHz)

FRONT VIEW



144-PIN SODIMM
(128MB, 66 MHz)

FRONT VIEW

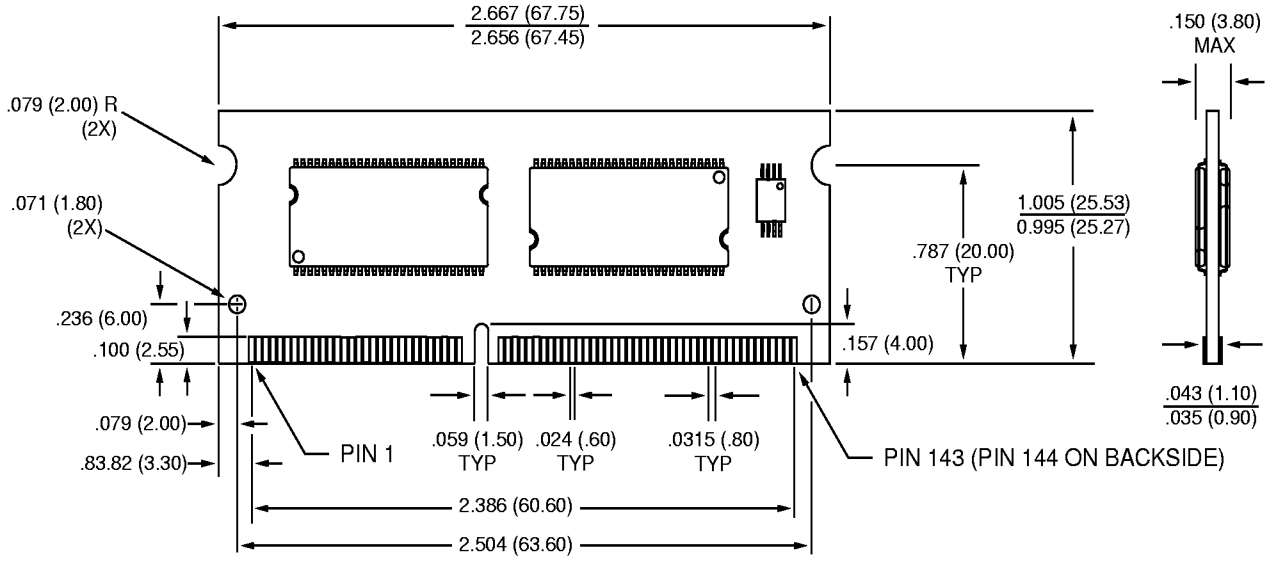


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

144-PIN SODIMM

(128MB, 100 MHz)

FRONT VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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