查询MAX509供应商

19-0155; Rev 2; 1/96

MAXIM

Quad, Serial 8-Bit DACs with Rail-to-Rail Outputs

General Description

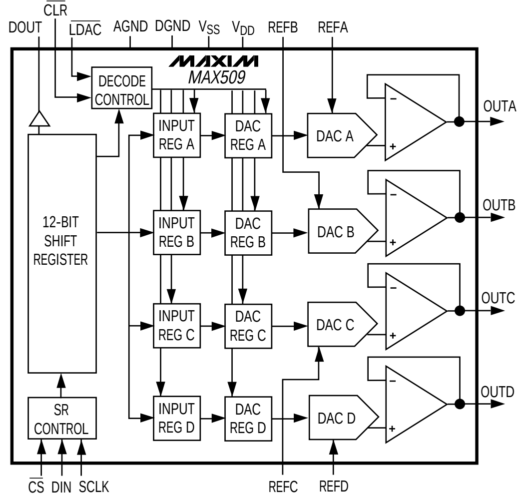
The MAX509/MAX510 are quad, serial-input, 8-bit voltage-output digital-to-analog converters (DACs). They operate with a single +5V supply or dual ±5V supplies. Internal, precision buffers swing rail-to-rail. The reference input range includes both supply rails.

The MAX509 has four separate reference inputs, allowing each DAC's full-scale range to be set independently. 20-pin DIP, SSOP, and SO packages are available. The MAX510 is identical to the MAX509 except it has two reference inputs, each shared by two DACs. The MAX510 is housed in space-saving 16-pin DIP and SO packages.

The serial interface is double-buffered: A 12-bit input shift register is followed by four 8-bit buffer registers and four 8-bit DAC registers. A 12-bit serial word is used to load data into each register. Both input and DAC registers can be updated independently or simultaneously with single software commands. Two additional asynchronous control pins provide simultaneous updating ($\overline{LDAC}$) or clearing ($\overline{CLR}$) of input and DAC registers.

The interface is compatible with Microwire™ and SPI/QSPI™. All digital inputs and outputs are TTL/CMOS compatible. A buffered data output provides for read-back or daisy-chaining of serial devices.

Functional Diagrams



Functional Diagrams continued at end of data sheet.

Features

- ♦ **Single +5V or Dual ±5V Supply Operation**
- ♦ **Output Buffer Amplifiers Swing Rail-to-Rail**
- ♦ **Reference Input Range Includes Both Supply Rails**
- ♦ **Calibrated Offset, Gain, and Linearity (1LSB TUE)**
- ♦ **10MHz Serial Interface, Compatible with SPI, QSPI (CPOL = CPHA = 0) and Microwire**
- ♦ **Double-Buffered Registers for Synchronous Updating**
- ♦ **Serial Data Output for Daisy-Chaining**
- ♦ **Power-On Reset Clears Serial Interface and Sets All Registers to Zero**

Ordering Information

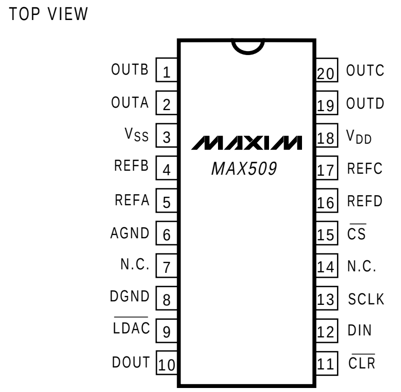
PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX509ACPP	0°C to +70°C	20 Plastic DIP	±1
MAX509BCPP	0°C to +70°C	20 Plastic DIP	±1 1/2
MAX509ACWP	0°C to +70°C	20 Wide SO	±1
MAX509BCWP	0°C to +70°C	20 Wide SO	±1 1/2
MAX509ACAP	0°C to +70°C	20 SSOP	±1
MAX509BCAP	0°C to +70°C	20 SSOP	±1 1/2
MAX509BC/D	0°C to +70°C	Dice*	±1 1/2

Ordering Information continued on last page.

** Dice are specified at +25°C, DC parameters only.*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



DIP/SO/SSOP

Pin Configurations continued at end of data sheet.

Microwire is a trademark of National Semiconductor. SPI and QSPI are trademarks of Motorola.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ....-0.3V, +6V
V_{DD} to AGND..............................-0.3V, +6V
V_{SS} to DGND ....-6V, +0.3V
V_{SS} to AGND ....-6V, +0.3V
V_{DD} to V_{SS} ....-0.3V, +12V
Digital Input Voltage to DGND ....-0.3V, (V_{DD} + 0.3V)
REF_..............................(V_{SS} - 0.3V), (V_{DD} + 0.3V)
OUT_..............................V_{DD}, V_{SS}
Maximum Current into Any Pin..............................50mA
Continuous Power Dissipation (T_A = +70°C)
  16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
  16-Pin Wide SO (derate 9.52mW/°C above +70°C).........762mW
  16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
  20-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
  20-Pin Wide SO (derate 10.00mW/°C above +70°C).......800mW
  20-Pin SSOP (derate 10.00mW/°C above +70°C)...........800mW
  20-Pin CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
  MAX5_ _ _C_ _ ....0°C to +70°C
  MAX5_ _ _E_ _ ....-40°C to +85°C
  MAX5_ _ _MJ_ ....-55°C to +125°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10sec) ....+300°C

Note: The outputs may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 50mA. Do not bias AGND more than +1V above DGND, or more than 2.5V below DGND.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, V_{REF} = 4V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE	VREF = +4V, V_{SS} = 0V or -5V ±10%	MAX5_ _A			±1	LSB
			MAX5_ _B			±1.5	
		VREF = -4V, V_{SS} = -5V ±10%	MAX5_ _A			±1	
			MAX5_ _B			±1.5	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	Code = 00 hex, V_{SS} = 0V	MAX5_ _C			14	mV
			MAX5_ _E			16	
			MAX5_ _M			20	
		Code = 00 hex, V_{SS} = -5V ±10%	MAX5_ _C			±14	
			MAX5_ _E			±16	
			MAX5_ _M			±20	
Zero-Code-Error Supply Rejection		Code = 00 hex, V_{DD} = 5V ±10%, V_{SS} = 0V or -5V ±10%			1	2	mV
Zero-Code Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex				±14	mV
Full-Scale-Error Supply Rejection		Code = FF hex, V_{DD} = +5V ±10%, V_{SS} = 0V or -5V ±10%	MAX5_ _C		1	4	mV
			MAX5_ _E		1	8	
			MAX5_ _M		1	12	
Full-Scale-Error Temperature Coefficient		Code = FF hex			±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, V_{REF} = 4V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Input Voltage Range				V_{SS}		V_{DD}	V
Input Resistance (Note 1)		Code = 55 hex	MAX509	16	24		kΩ
			MAX510	8	12		
Input Capacitance (Note 2)		Code = 00 hex	MAX509		15		pF
			MAX510		30		
Channel-to-Channel Isolation		(Note 3)			-60		dB
AC Feedthrough		(Note 4)			-70		dB
DAC OUTPUTS							
Full-Scale Output Voltage				V_{SS}		V_{DD}	V
Resistive Load		VREF = 4V, load regulation ≤ 1/4LSB		2			kΩ
		VREF = -4V, V_{SS} = -5V ±10%, load regulation ≤ 1/4LSB		2			
		VREF = V_{DD} MAX5_ _C/E, load regulation ≤ 1LSB		10			
		VREF = V_{DD} MAX5_ _M, load regulation ≤ 2LSB		10			
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance	C_{IN}	(Note 5)				10	pF
DIGITAL OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA		V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate		Positive and negative	MAX5_ _C	1.0			V/µs
			MAX5_ _E	0.7			
			MAX5_ _M	0.5			
Output Settling Time (Note 6)		To 1/2LSB, 10kΩ II 100pF load			6		µs
Digital Feedthrough		Code = 00 hex, all digital inputs from 0V to V_{DD}			5		nV-s
Digital-to-Analog Glitch Impulse		Code 128→127			12		nV-s
Signal-to-Noise + Distortion Ratio	SINAD	VREF = $4V_{p-p}$ at 1kHz, V_{DD} = 5V, code = FF hex			87		dB
		VREF = $4V_{p-p}$ at 20kHz, V_{SS} = -5V ±10%			74		
Multiplying Bandwidth		VREF = $0.5V_{p-p}$, 3dB bandwidth			1		MHz
Wideband Amplifier Noise					60		$µV_{RMS}$

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, V_{REF} = 4V, AGND = DGND = 0V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specified performance		4.5		5.5	V
Negative Supply Voltage	V_{SS}	For specified performance		-5.5		0	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or V_{DD}	MAX5_ _C/E		5	10	mA
			MAX5_ _M		5	12	
Negative Supply Current	I_{SS}	V_{SS} = -5V ±10%, outputs unloaded, all digital inputs = 0V or V_{DD}	MAX5_ _C/E		5	10	mA
			MAX5_ _M		5	12	

Note 1: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 2: Input capacitance is code dependent. The highest input capacitance occurs at code = 00 hex.
Note 3: VREF = $4V_{p-p}$, 10kHz. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 4: VREF = $4V_{p-p}$, 10kHz. DAC code = 00 hex.
Note 5: Guaranteed by design.
Note 6: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

TIMING CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5V, V_{REF} = 4V, AGND = DGND = 0V, C_L = 50pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

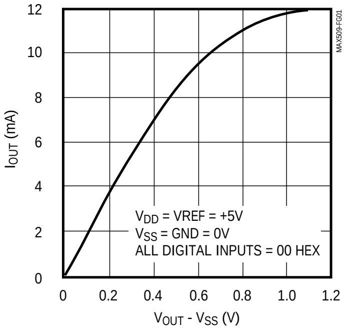
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{LDAC}}$ Pulse Width Low	t_{LDW}	MAX5_ _C/E	40	20		ns
		MAX5_ _M	50	25		
$\overline{\text{CS}}$ Rise to $\overline{\text{LDAC}}$ Fall Setup Time	t_{CLL}	(Notes 7, 8)	0			ns
$\overline{\text{CLR}}$ Pulse Width Low	t_{CLW}	MAX5_ _C/E	40	20		ns
		MAX5_ _M	50	25		
SERIAL INTERFACE TIMING						
$\overline{\text{CS}}$ Fall to SCLK Setup Time	t_{CSS}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
SCLK Fall to $\overline{\text{CS}}$ Rise Hold Time	t_{CSH2}		0			ns
SCLK Rise to $\overline{\text{CS}}$ Rise Hold Time	t_{CSH1}	(Note 9)	40			ns
SCLK Fall to $\overline{\text{CS}}$ Fall Hold Time	t_{CSH0}	(Note 7)	0			ns
DIN to SCLK Rise Setup Time	t_{DS}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Clock Frequency	f_{CLK}	MAX5_ _C/E		20	12.5	MHz
		MAX5_ _M		20	10	
SCLK Pulse Width High	t_{CH}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
SCLK Pulse Width Low	t_{CL}	MAX5_ _C/E	40			ns
		MAX5_ _M	50			
SCLK to DOUT Valid	t_{DO}	MAX5_ _C/E	10		100	ns
		MAX5_ _M	10		100	

Note 7: Guaranteed by design.
Note 8: If $\overline{\text{LDAC}}$ is activated prior to $\overline{\text{CS}}$'s rising edge, it must stay low for t_{LDW} or longer after $\overline{\text{CS}}$ goes high.
Note 9: Minimum delay from 12th clock cycle to $\overline{\text{CS}}$ rise.

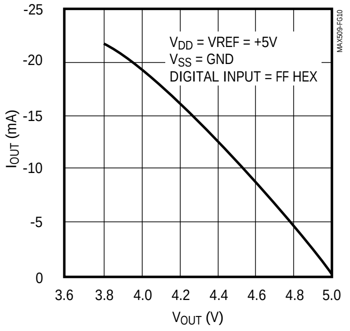
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

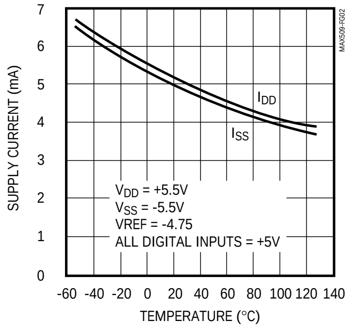
OUTPUT SINK CURRENT vs. (V_{OUT} - V_{SS})



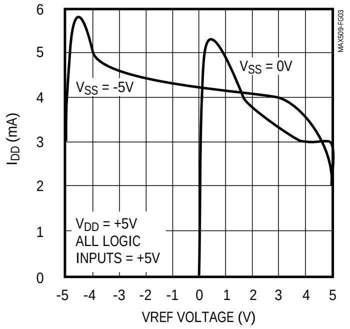
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



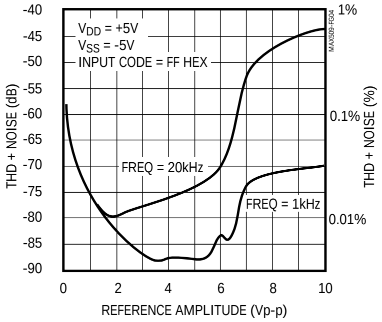
SUPPLY CURRENT vs. TEMPERATURE



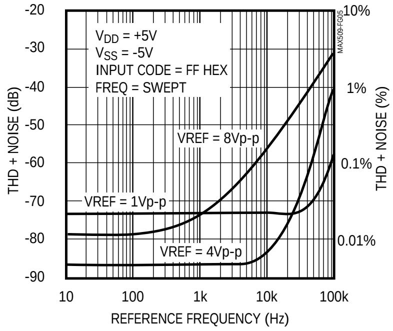
SUPPLY CURRENT vs. REFERENCE VOLTAGE



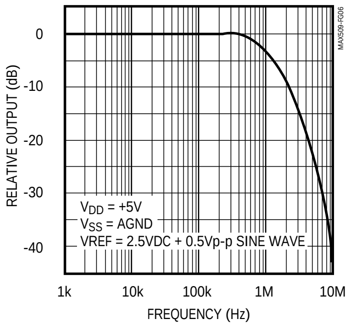
THD + NOISE AT DAC OUTPUT vs. REFERENCE AMPLITUDE



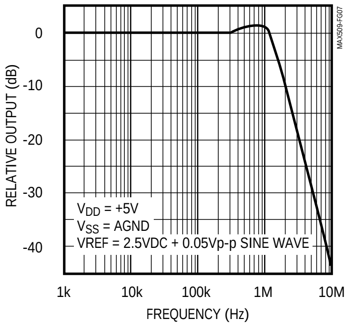
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



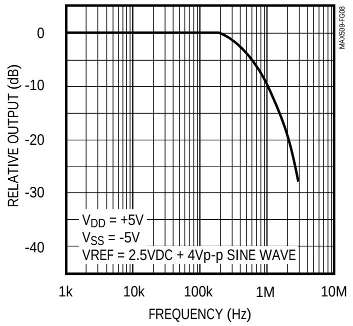
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

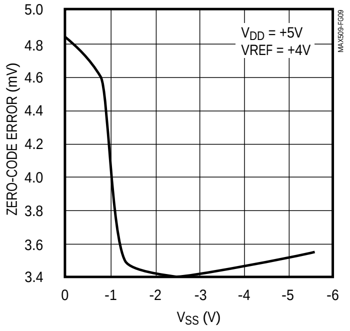


REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE

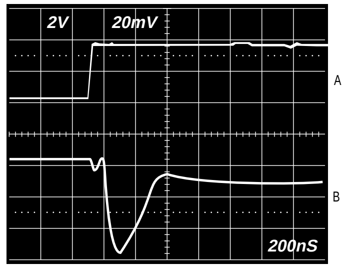


Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

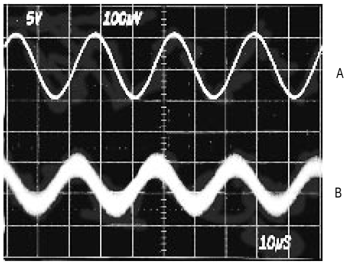


ZERO-CODE ERROR vs. NEGATIVE SUPPLY VOLTAGE



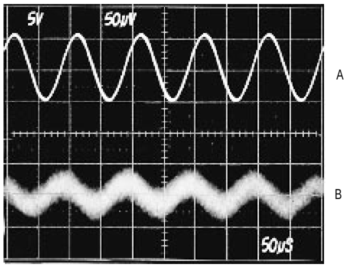
WORST-CASE 1LSB DIGITAL STEP CHANGE

A = $\overline{CS}$, 2V/div
B = OUTA, 20mV ~
TIMEBASE = 200ns/div



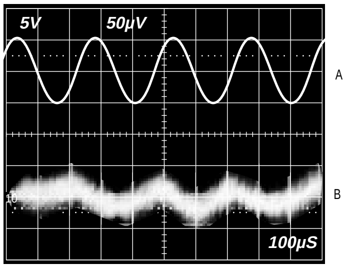
REFERENCE FEEDTHROUGH AT 40kHz

A = REFA, 10V_{p-p}
B = OUTA, 100µV/div, UNLOADED
TIMEBASE = 10µs/div
V_{DD} = +5V, V_{SS} = -5V
CODE = ALL 0s



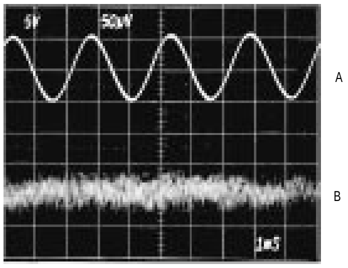
REFERENCE FEEDTHROUGH AT 10kHz

A = REFA, 10V_{p-p}
B = OUTA, 50µV/div, UNLOADED
TIMEBASE = 50µs/div



REFERENCE FEEDTHROUGH AT 4kHz

A = REFA, 10V_{p-p}
B = OUTA, 50µV/div, UNLOADED
TIMEBASE = 100µs/div



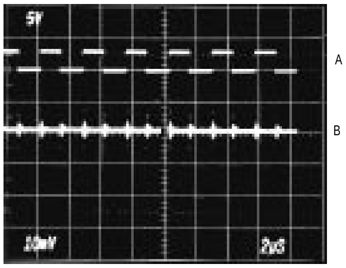
REFERENCE FEEDTHROUGH AT 400Hz

A = REFA, 10V_{p-p}
B = OUTA, 50µV/div, UNLOADED
TIMEBASE = 1ms/div

Typical Operating Characteristics (continued)

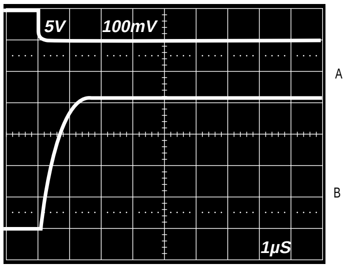
(T_A = +25°C, unless otherwise noted.)

CLOCK FEEDTHROUGH



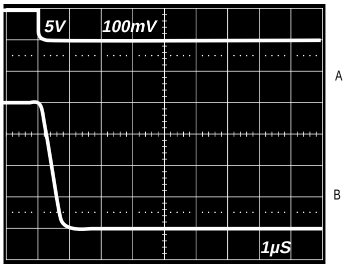
A = SCLK, 333kHz
B = OUT_, 10mV/div
TIMEBASE = 2µs/div

POSITIVE SETTLING TIME
(V_{SS} = AGND OR -5V)



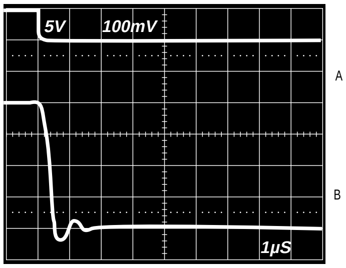
A = DIGITAL INPUT, 5V/div
B = OUT_ , 2V/div
TIMEBASE = 1µs/div
V_{DD} = +5V
REF_ = +4V
ALL BITS OFF TO ALL BITS ON
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME
(V_{SS} = AGND)



A = DIGITAL INPUT, 5V/div
B = OUT_ , 2V/div
TIMEBASE = 1µs/div
V_{DD} = +5V
REF_ = +4V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME
(V_{SS} = -5V)



A = DIGITAL INPUT, 5V/div
B = OUT_ , 2V/div
TIMEBASE = 1µs/div
V_{DD} = +5V
REF_ = +4V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

Pin Description

PIN		NAME	FUNCTION
MAX509	MAX510		
1	1	OUTB	DAC B Voltage Output
2	2	OUTA	DAC A Voltage Output
3	3	V_{SS}	Negative Power Supply, 0V to -5V ±10%. Connect to AGND for single-supply operation.
4	–	REFB	Reference Voltage Input for DAC B
–	4	REFAB	Reference Voltage Input for DACs A and B
5	–	REFA	Reference Voltage Input for DAC A
6	5	AGND	Analog Ground
7, 14	–	N.C.	Not Internally Connected
8	6	DGND	Digital Ground
9	7	$\overline{\text{LDAC}}$	Load DAC Input (active low). Driving this asynchronous input low (level sensitive) transfers the contents of each input latch to its respective DAC latch.
10	8	DOUT	Serial Data Output. Can sink and source current. Data at DOUT is adjustable to be clocked out on rising or falling edge of SCLK.
11	9	$\overline{\text{CLR}}$	Clear DAC input (active low). Driving $\overline{\text{CLR}}$ low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero.
12	10	DIN	Serial Data Input. TTL/CMOS-compatible input. Data is clocked into DIN on the rising edge of SCLK. $\overline{\text{CS}}$ must be low for data to be clocked in.
13	11	SCLK	Serial Clock Input. Data is clocked in on the rising edge and clocked out on either the rising (default) or the falling edge.
15	12	$\overline{\text{CS}}$	Chip-Select Input (active low). Data is shifted in and out when $\overline{\text{CS}}$ is low. Programming commands are executed when $\overline{\text{CS}}$ rises.
16	–	REFD	Reference Voltage Input for DAC D
–	13	REFCD	Reference Voltage Input for DACs C and D
17	–	REFC	Reference Voltage Input for DAC C
18	14	V_{DD}	Positive Power Supply, +5V ±10%
19	15	OUTD	DAC D Output Voltage
20	16	OUTC	DAC C Output Voltage

Detailed Description

Serial Interface

At power-on, the serial interface and all DACs are cleared and set to code zero. The serial data output (DOUT) is set to transition on SCLK's rising edge.

The MAX509/MAX510 communicate with microprocessors through a synchronous, full-duplex, 3-wire interface (Figure 1). Data is sent MSB first and can be transmitted in one 4-bit and one 8-bit (byte) packet or in one 12-bit word. If a 16-bit control word is used, the first four bits are ignored. A 4-wire interface adds a line for $\overline{\text{LDAC}}$ and allows asynchronous updating. The serial clock (SCLK) synchronizes the data transfer. Data is transmitted and received simultaneously.

Figure 2 shows a detailed serial interface timing. Please note that the clock should be low if it is stopped between updates. DOUT does not go into a high-impedance state if the clock or $\overline{\text{CS}}$ is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is clocked in on SCLK's rising edge while $\overline{\text{CS}}$ is low. Data at DOUT is clocked out 12 clock cycles later, either at SCLK's rising edge (default or mode 1) or falling edge (mode 0).

Chip select ($\overline{\text{CS}}$) must be low to enable the DAC. If $\overline{\text{CS}}$ is high, the interface is disabled and DOUT remains unchanged. $\overline{\text{CS}}$ must go low at least 40ns before the first rising edge of the clock pulse to properly clock in the first bit. With $\overline{\text{CS}}$ low, data is clocked into the MAX509/MAX510's internal shift register on the rising edge of the external serial clock. SCLK can be driven at rates up to 12.5MHz.

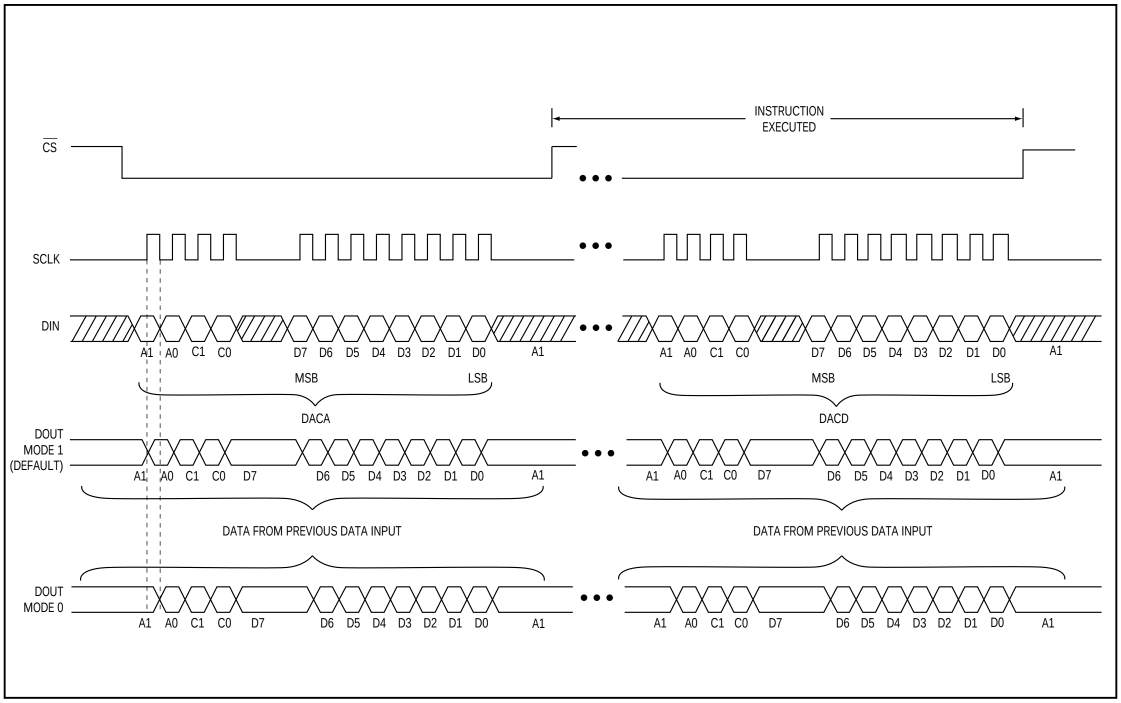
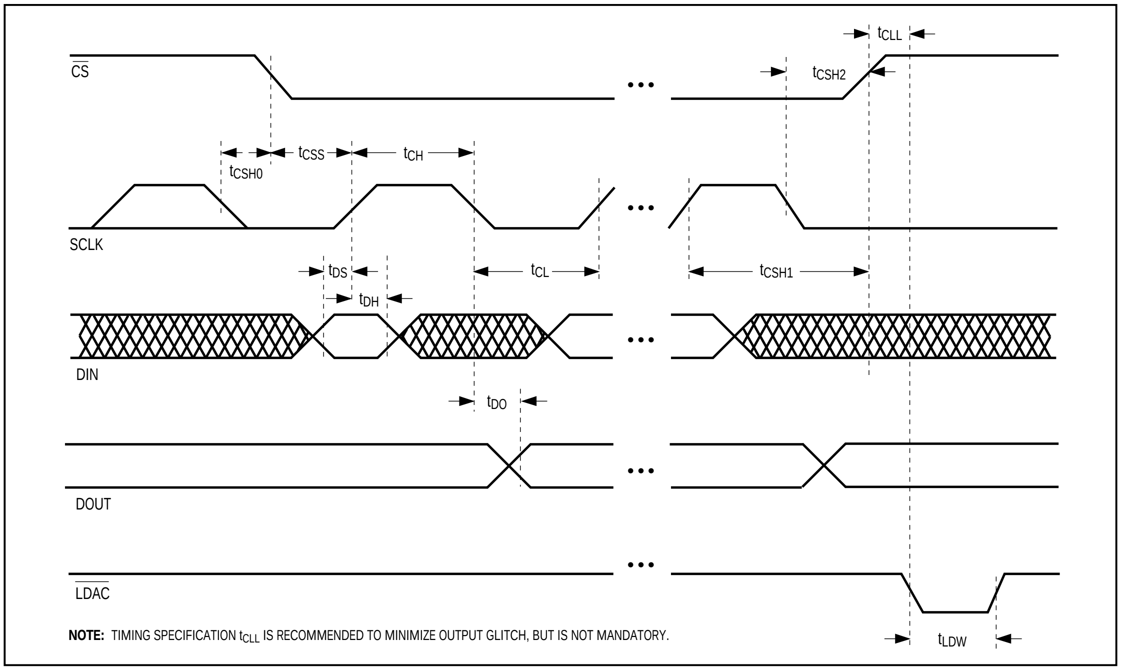


Figure 1. MAX509/MAX510 3-Wire Interface Timing



NOTE: TIMING SPECIFICATION t_{CLL} IS RECOMMENDED TO MINIMIZE OUTPUT GLITCH, BUT IS NOT MANDATORY.

Figure 2. Detailed Serial Interface Timing (Mode 0 Shown)

Table 1. Serial-Interface Programming Commands

12-Bit Serial Word					$\overline{\text{LDAC}}$	Function
A1	**A0**	**C1**	**C0**	**D7 . . . . D0**		
0	0	0	1	8-Bit DAC Data	1	Load DAC A input register, DAC output unchanged.
0	1	0	1	8-Bit DAC Data	1	Load DAC B input register, DAC output unchanged.
1	0	0	1	8-Bit DAC Data	1	Load DAC C input register, DAC output unchanged.
1	1	0	1	8-Bit DAC Data	1	Load DAC D input register, DAC output unchanged.
0	0	1	1	8-Bit DAC Data	1	Load input and DAC register A.
0	1	1	1	8-Bit DAC Data	1	Load input and DAC register B.
1	0	1	1	8-Bit DAC Data	1	Load input and DAC register C.
1	1	1	1	8-Bit DAC Data	1	Load input and DAC register D.
X	0	0	0	8-Bit DAC Data	X	Update all DACs from shift register.
X	1	0	0	X X X X X X X X	X	No Operation (NOP), shifts data in shift register.
0	X	1	0	X X X X X X X X	X	“$\overline{\text{LDAC}}$” Command, all DACs updated from respective input registers.
1	1	1	0	X X X X X X X X	X	Mode 1, DOUT clocked out on rising edge of SCLK (default). All DACs updated from respective input registers.
1	0	1	0	X X X X X X X X	X	Mode 0, DOUT clocked out on falling edge of SCLK. All DACs updated from input registers.

Serial Input Data Format and Control Codes

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two control bits (C1, C0) and eight bits of data (D0...D7).

The 4-bit address/control code configures the DAC as shown in Table 1.

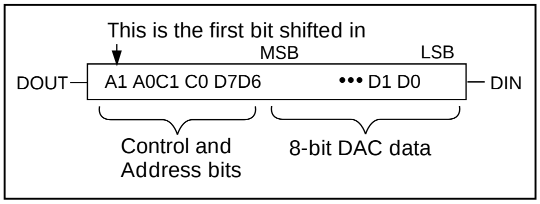


Figure 3. Serial Input Format

Load Input Register, DAC Registers Unchanged (Single Update Operation)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		0	1	8-Bit Data							

($\overline{\text{LDAC}}$ = H)

When performing a single update operation, A1 and A0 select the respective input register. At the rising edge of $\overline{\text{CS}}$, the selected input register is loaded with the current shift-register data. All DAC outputs remain unchanged. This preloads individual data in the input register without changing the DAC outputs.

Load Input and DAC Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
Address		1	1	8-Bit Data							

($\overline{\text{LDAC}}$ = H)

This command directly loads the selected DAC register at $\overline{\text{CS}}$'s rising edge. A1 and A0 set the DAC address. Current shift-register data is placed in the selected input and DAC registers.

For example, to load all four DAC registers simultaneously with individual settings (DAC A = 1V, DAC B = 2V, DAC C = 3V and DAC D = 4V), five commands are required. First, perform four single input register update operations. Next, perform an "$\overline{\text{LDAC}}$" command as a fifth command. All DACs will be updated from their respective input registers at the rising edge of $\overline{\text{CS}}$.

Update All DACs from Shift Registers

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
x	0	0	0	8-Bit DAC Data							

($\overline{\text{LDAC}}$ = x)

All four DAC registers are updated with shift-register data. This command allows all DACs to be set to any analog value within the reference range. This command can be used to substitute $\overline{\text{CLR}}$ if code 00 hex is programmed, which clears all DACs.

No Operation (NOP)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
x	1	0	0	x	x	x	x	x	x	x	x

($\overline{\text{LDAC}}$ = x)

The NOP command (no operation) allows data to be shifted through the MAX509/MAX510 shift register without affecting the input or DAC registers. This is useful in daisy chaining (also see the *Daisy-Chaining Devices* section). For this command, the data bits are "Don't Cares." As an example, three MAX509/MAX510s are daisy-chained (A, B and C), and DAC A and DAC C need to be updated. The 36-bit-wide command would consist of one 12-bit word for device C, followed by an NOP instruction for device B and a third 12-bit word with data for device A. At $\overline{\text{CS}}$'s rising edge, only device B is not updated.

"$\overline{\text{LDAC}}$" Command (Software)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
0	x	1	0	x	x	x	x	x	x	x	x

($\overline{\text{LDAC}}$ = x)

All DAC registers are updated with the contents of their respective input registers at $\overline{\text{CS}}$'s rising edge. With the exception of using $\overline{\text{CS}}$ to execute, this performs the same function as the asynchronous $\overline{\text{LDAC}}$.

Set DOUT Phase – SCLK Rising (Mode 1, Default)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	x	x	x	x	x	x	x	x

($\overline{\text{LDAC}}$ = x)

Mode 1 resets the serial output DOUT to transition at SCLK's rising edge. This is the MAX509/MAX510's default setting after the supply voltage has been applied.

The command also loads all DAC registers with the contents of their respective input registers, and is identical to the "$\overline{\text{LDAC}}$" command.

Set DOUT Phase – SCLK Falling (Mode 0)

A1	A0	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	x	x	x	x	x	x	x	x

($\overline{\text{LDAC}}$ = x)

This command resets DOUT to transition at SCLK's falling edge. Once this command is issued, the phase of DOUT is latched and will not change except on power-up or if the specific command is issued that sets the phase to rising edge.

The same command also updates all DAC registers with the contents of their respective input registers, identical to the "$\overline{\text{LDAC}}$" command.

$\overline{\text{LDAC}}$ Operation (Hardware)

$\overline{\text{LDAC}}$ is typically used in 4-wire interfaces (Figure 7). $\overline{\text{LDAC}}$ allows asynchronous hardware control of the DAC outputs and is level-sensitive. With $\overline{\text{LDAC}}$ low, the DAC registers are transparent and any time an input register is updated, the DAC output immediately follows.

Clear DACs with $\overline{\text{CLR}}$

Strobing the $\overline{\text{CLR}}$ pin low causes an asynchronous clear of input and DAC registers and sets all DAC outputs to zero. Similar to the $\overline{\text{LDAC}}$ pin, $\overline{\text{CLR}}$ can be invoked at any time, typically when the device is not selected ($\overline{\text{CS}}$ = H). When the DAC data is all zeros, this function is equivalent to the "Update all DACs from Shift Registers" command.

Digital Inputs and Outputs

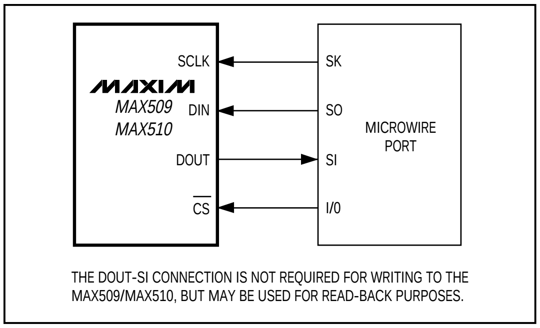
Digital inputs and outputs are compatible with both TTL and 5V CMOS logic. The power-supply current (I_{DD}) depends on the input logic levels. Using CMOS logic to drive $\overline{\text{CS}}$, SCLK, DIN, $\overline{\text{CLR}}$ and $\overline{\text{LDAC}}$ turns off the internal level translators and minimizes supply currents.

Serial Data Output

DOUT is the output of the internal shift register. DOUT can be programmed to clock out data on SCLK's falling edge (mode 0) or rising edge (mode 1). In mode 0, output data lags the input data by 12.5 clock cycles, maintaining compatibility with Microwire, SPI, and QSPI. In mode 1, output data lags the input by 12 clock cycles. On power-up, DOUT defaults to mode 1 timing. DOUT never three-states; it always actively drives either high or low and remains unchanged when $\overline{\text{CS}}$ is high.

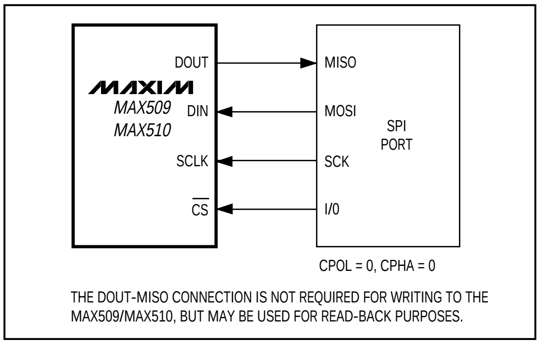
Interfacing to the Microprocessor

The MAX509/MAX510 are Microwire, SPI, and QSPI compatible. For SPI and QSPI, clear the CPOL and CPHA configuration bits (CPOL = CPHA = 0). The SPI/QSPI CPOL = CPHA = 1 configuration can also be used if the DOUT output is ignored.



THE DOUT-SI CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX509/MAX510, BUT MAY BE USED FOR READ-BACK PURPOSES.

Figure 4. Connections for Microwire



CPOL = 0, CPHA = 0

THE DOUT-MISO CONNECTION IS NOT REQUIRED FOR WRITING TO THE MAX509/MAX510, BUT MAY BE USED FOR READ-BACK PURPOSES.

Figure 5. Connections for SPI

The MAX509/MAX510 can interface with Intel's 80C5X/80C3X family in mode 0 if the SCLK clock polarity is inverted. More universally, if a serial port is not available, three lines from one of the parallel ports can be used for bit manipulation.

Digital feedthrough at the voltage outputs is greatly minimized by operating the serial clock only to update the registers. Also see the Clock Feedthrough photo in the *Typical Operating Characteristics* section. The clock idle state is low.

Daisy-Chaining Devices

Any number of MAX509/MAX510s can be daisy-chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain. The NOP instruction (Table 1) allows data to be passed from DIN to DOUT without changing the input or DAC registers of the passing device. A three-wire interface updates daisy-chained or individual MAX509/MAX510s simultaneously by bringing $\overline{\text{CS}}$ high.

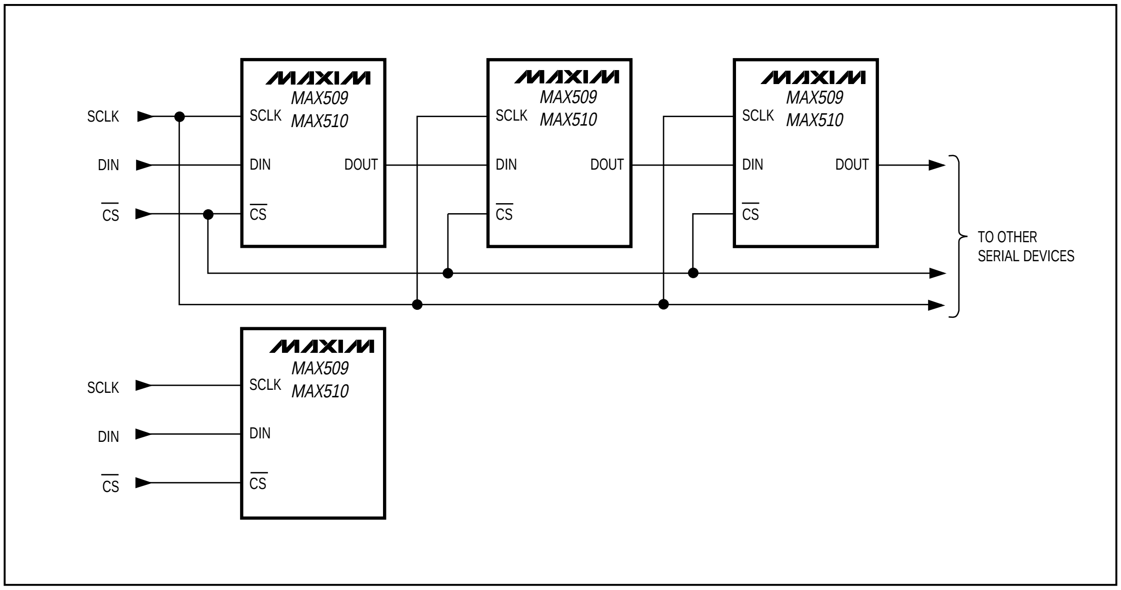


Figure 6. Daisy-chained or individual MAX509/MAX510s are simultaneously updated by bringing $\overline{CS}$ high. Only three wires are required.

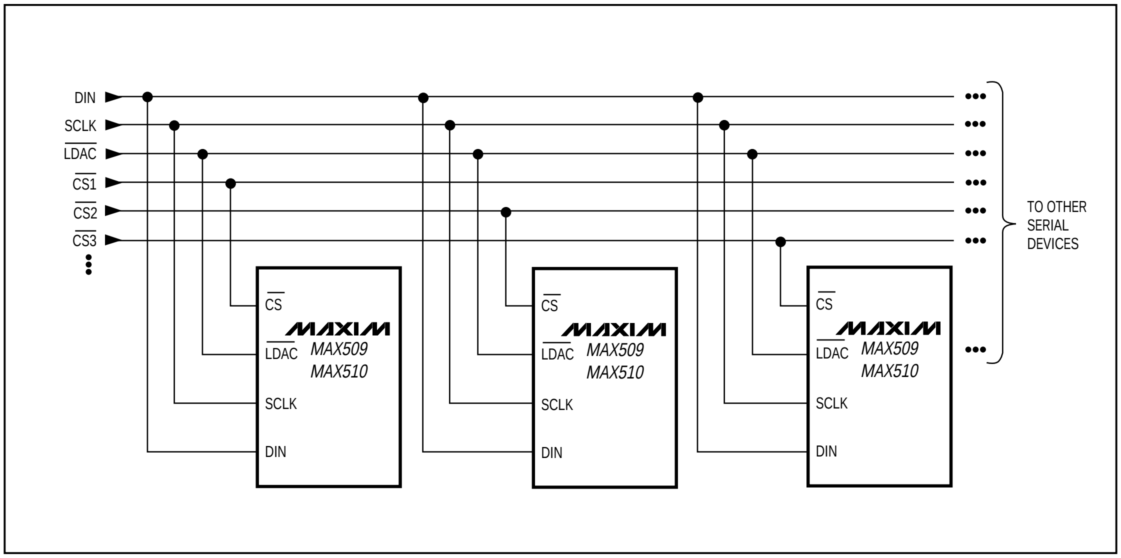


Figure 7. Multiple MAX509/MAX510 DACs sharing one DIN line. Simultaneously update by strobing $\overline{LDAC}$, or specifically update by enabling individual $\overline{CS}$.

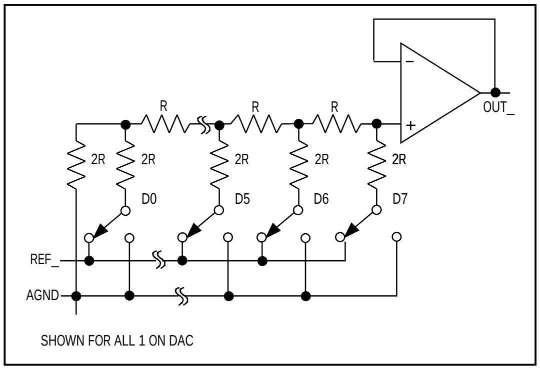


Figure 8. DAC Simplified Circuit Diagram

If multiple devices share a common DIN line, Figure 7's configuration provides simultaneous update by strobing $\overline{\text{LDAC}}$ low. $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$... are driven separately, thus controlling which data are written to devices 1, 2, 3....

Analog Section

DAC Operation

The MAX509/MAX510 contain four matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltages. Each DAC in the MAX509 has a separate reference input, while the two reference inputs in the MAX510 each share a pair of DACs. The two reference inputs permit different full-scale output voltage ranges for each pair of DACs. A simplified diagram of one of the four DACs is shown in Figure 8.

Reference Input

The MAX509/MAX510 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each REF input sets the full-scale output voltage for its respective DAC(s). If the reference voltage is positive, both the MAX509 and MAX510 can be operated from a single supply. If dual supplies are used, the reference input can vary from V_{SS} to V_{DD}, but is always referred to AGND. The input impedance at REF is code dependent, with the lowest value (16kΩ for the MAX509 and 8kΩ for the MAX510) occurring when the input code is 55 hex or 0101 0101. The maximum value, practically infinity, occurs when the input code is 00 hex. Since the REF input impedance is code dependent, the DAC's reference sources must have a low output impedance (no more than 32Ω for the MAX509 and 16Ω for the MAX510) to maintain output linearity. The REF input capacitance is also code dependent: 15pF typical for the MAX509 and 30pF typical for the MAX510.

The output voltage for any DAC can be represented by a digitally programmable voltage source as:

$$VOUT = (NB \times VREF) / 256$$

where NB is the numerical value of the DAC's binary input code.

Output Buffer Amplifiers

All MAX509/MAX510 voltage outputs are internally buffered by precision unity-gain followers that slew at up to 1V/µs. The outputs can swing from V_{SS} to V_{DD}. With a 0V to +4V (or +4V to 0V) output transition, the amplifier outputs will settle to 1/2LSB in typically 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 300pF.

Applications Information

Power Supply and Reference Operating Ranges

The MAX509/MAX510 are fully specified to operate with V_{DD} = 5V ±10% and V_{SS} = 0V to -5.5V. 8-bit performance is guaranteed for both single- and dual-supply operation. The zero-code output error is less than 14mV when operating from a single +5V supply.

The DACs work well with reference voltages from V_{SS} to V_{DD}. The reference voltage is referred to AGND.

The preferred power-up sequence is to apply V_{SS} and then V_{DD}, but bringing up both supplies at the same time is also acceptable. In either case, the voltage applied to REF should not exceed V_{DD} during power-up or at any other time. If proper power sequencing is not possible, connect an external Schottky diode between V_{SS} and AGND to ensure compliance with the *Absolute Maximum Ratings*. Do not apply signals to the digital inputs before the device is fully powered up.

Power-Supply Bypassing and Ground Management

In single-supply operation (AGND = DGND = V_{SS} = 0V), AGND, DGND and V_{SS} should be connected together in a "star" ground at the chip. This ground should then return to the highest quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and DGND as possible. In dual-supply operation, bypass V_{SS} to AGND with 0.1µF.

Careful PC board layout minimizes crosstalk among DAC outputs, reference inputs, and digital inputs. Figures 9 and 10 show suggested circuit board layouts to minimize crosstalk.

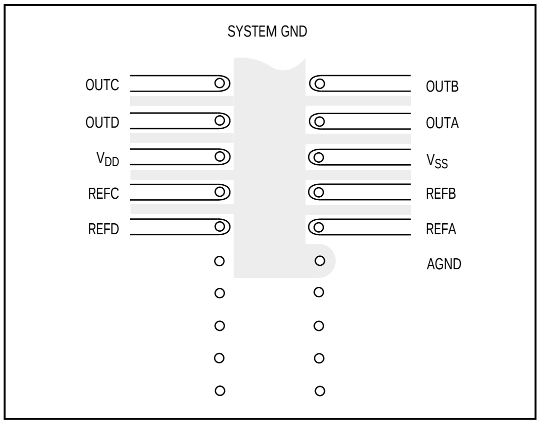


Figure 9. Suggested MAX509 PC Board Layout for Minimizing Crosstalk (Bottom View)

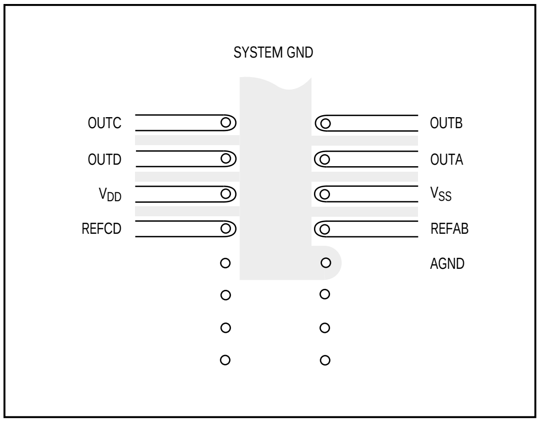


Figure 10. Suggested MAX510 PC Board Layout for Minimizing Crosstalk (Bottom View)

Unipolar-Output, 2-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Figures 11 and 12 show the MAX509/MAX510 unipolar configurations. Both devices can be operated from a single supply if the reference inputs are positive. If dual supplies are used, the reference input can vary from V_{SS} to V_{DD}. Table 2 shows the unipolar code.

Table 2. Unipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	0V

Note: $1LSB = (V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

Bipolar-Output, 2-Quadrant Multiplication

Bipolar-output, 2-quadrant multiplication is achieved by offsetting AGND positively or negatively. Table 3 shows the bipolar code.

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a 0 input code, as shown in Figure 13. The output voltage at OUTA is:

$$V_{OUTA} = V_{BIAS} + (NB/256)(V_{IN}),$$

Table 3. Bipolar Code Table

DAC CONTENTS		ANALOG OUTPUT
MSB	LSB	
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	0V
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

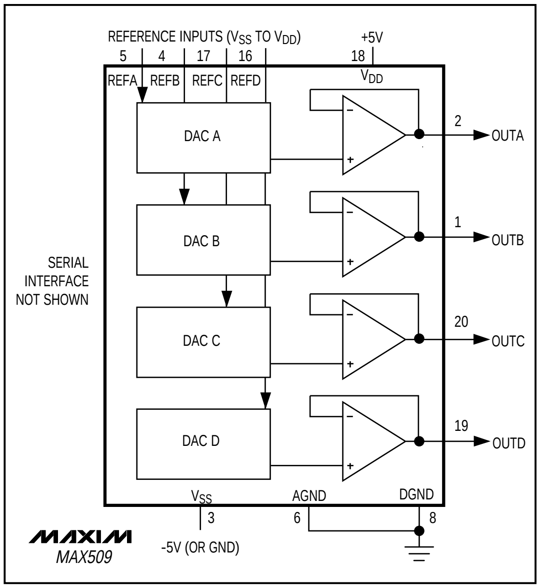


Figure 11. MAX509 Unipolar Output Circuit

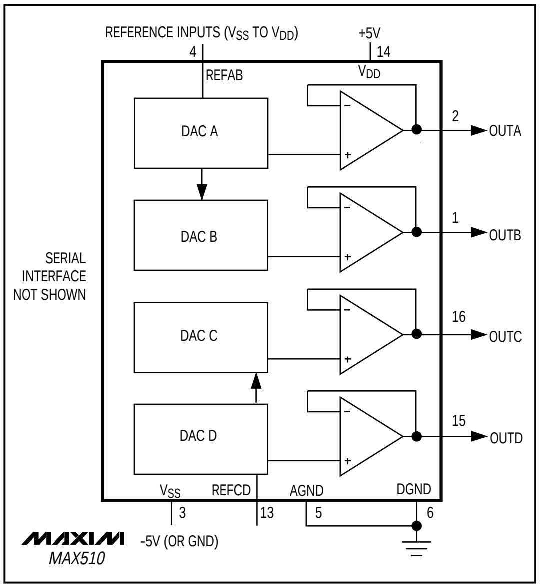


Figure 12. MAX510 Unipolar Output Circuit

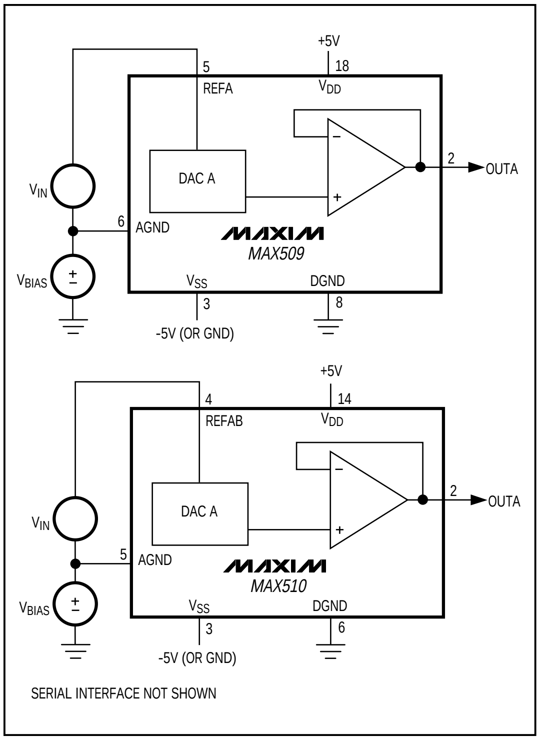


Figure 13. MAX509/MAX510 AGND Bias Circuits (Positive Offset)

where NB represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Do not bias AGND more than +1V above DGND, or more than 2.5V below DGND.

Figures 14 and 15 illustrate the generation of negative offsets with bipolar outputs. In these circuits, AGND is biased negatively (up to -2.5V with respect to DGND) to provide an arbitrary negative output voltage for a 0 input code. The output voltage at OUTA is:

$$OUTA = -(R2/R1)(2.5V) + (NB/256)(2.5V)(R2/R1+1)$$

where NB represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Table 3, with V_{REF} = 2.5V, shows the digital code vs. output voltage for Figure 14 and 15's circuits with R1 = R2. The ICL7612 op amp is chosen because its common-mode range extends to both supply rails.

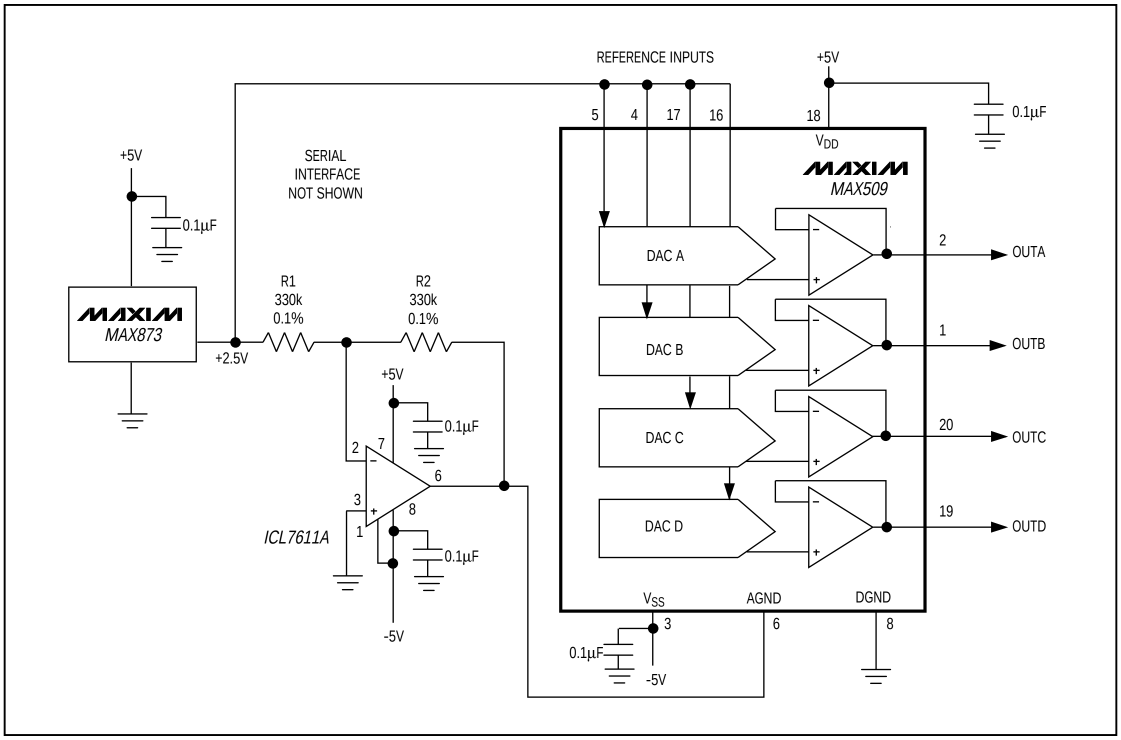


Figure 14. MAX509 AGND Bias Circuit (Negative Offset)

4-Quadrant Multiplication

Each DAC output may be configured for 4-quadrant multiplication using Figure 16 and 17's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF} [2(NB/256)-1]$$

where NB represents the digital word in DAC register A.

The recommended value for resistors R1 and R2 is 330kΩ (±0.1%). Table 3 shows the digital code vs. output voltage for Figure 16 and 17's circuit.

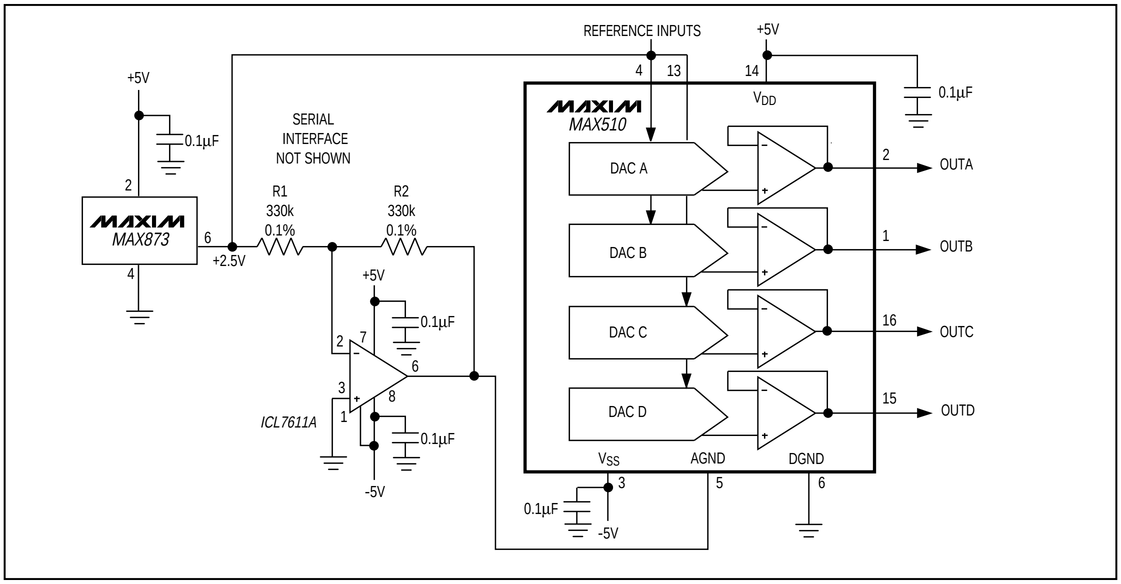


Figure 15. MAX510 AGND Bias Circuit (Negative Offset)

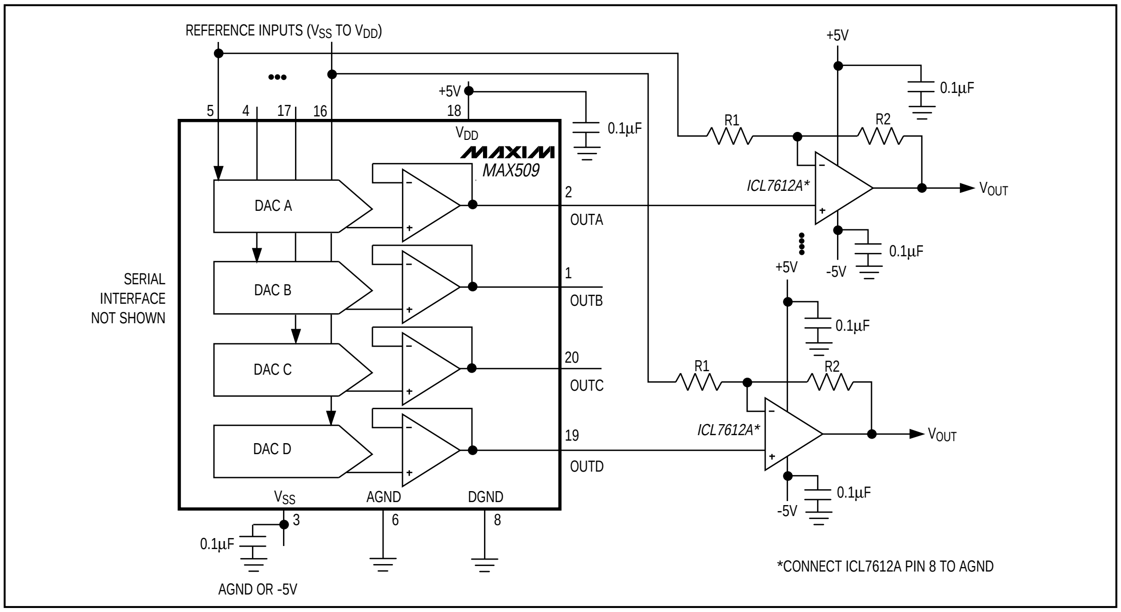


Figure 16. MAX509 Bipolar Output Circuit

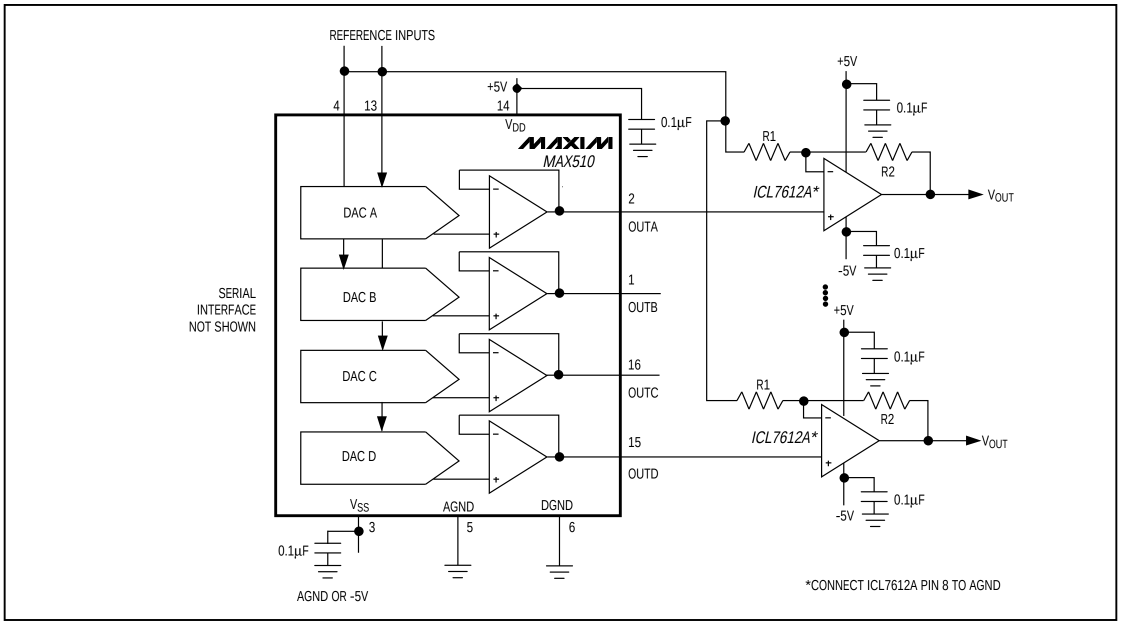
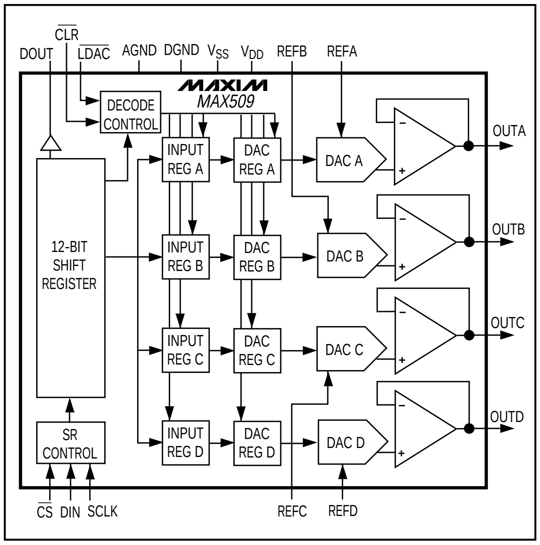
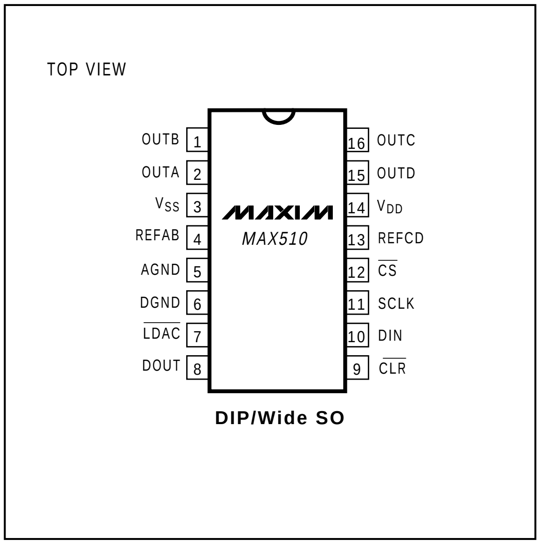


Figure 17. MAX510 Bipolar Output Circuit

Functional Diagrams (continued)



Pin Configurations (continued)

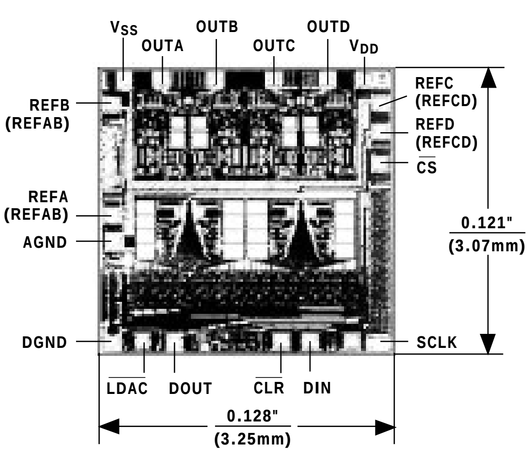


Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSB)
MAX509AEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX509BEPP	-40°C to +85°C	20 Plastic DIP	±1 1/2
MAX509AEWP	-40°C to +85°C	20 Wide SO	±1
MAX509BEWP	-40°C to +85°C	20 Wide SO	±1 1/2
MAX509AEAP	-40°C to +85°C	20 SSOP	±1
MAX509BEAP	-40°C to +85°C	20 SSOP	±1 1/2
MAX509AMJP	-55°C to +125°C	20 CERDIP**	±1
MAX509BMJP	-55°C to +125°C	20 CERDIP**	±1 1/2
MAX510ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX510BCPE	0°C to +70°C	16 Plastic DIP	±1 1/2
MAX510ACWE	0°C to +70°C	16 Wide SO	±1
MAX510BCWE	0°C to +70°C	16 Wide SO	±1 1/2
MAX510AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX510BEPE	-40°C to +85°C	16 Plastic DIP	±1 1/2
MAX510AEWE	-40°C to +85°C	16 Wide SO	±1
MAX510BEWE	-40°C to +85°C	16 Wide SO	±1 1/2
MAX510AMJE	-55°C to +125°C	16 CERDIP**	±1
MAX510BMJE	-55°C to +125°C	16 CERDIP**	±1 1/2

***Contact factory for availability and processing to MIL-STD-883.*

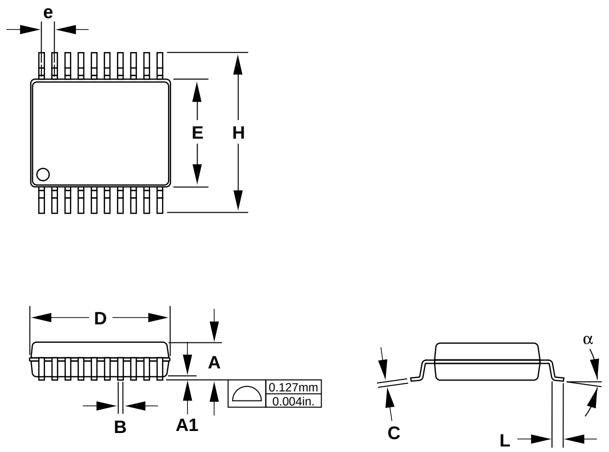
Chip Topography



NOTE: LABELS IN ( ) ARE FOR MAX510 ONLY.

TRANSISTOR COUNT: 2235;
SUBSTRATE CONNECTED TO V_{DD}.

Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.278	0.289	7.07	7.33
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

21-0003A

**20-PIN PLASTIC
SHRINK
SMALL-OUTLINE
PACKAGE**

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