19-1534; Rev 1; 10/99

MAXIM

+3.3V, 2.5Gbps, SDH/SONET, 4-Channel Interconnect Mux/Demux ICs with Clock Generator

General Description

The MAX3831/MAX3832 are 4:1 multiplexers (muxes) and 1:4 demultiplexers (demuxes) with automatic channel assignment. Operating from a single +3.3V supply, the mux receives four parallel, 622Mbps SDH/SONET channels. These channels are bit interleaved to generate a serial data stream of 2.488Gbps for interfacing to an optical or an electrical driver. A 10-bit-wide elastic buffer tolerates up to ±7.5ns skew between any parallel data input and the reference clock. An external 155MHz reference clock is required for the on-chip PLL to synthesize a high-frequency 2.488GHz clock for timing the outgoing data streams.

The MAX3831/MAX3832's demux receives 2.488Gbps serial data and the 2.488GHz clock from an external clock/data recovery device (MAX3876), converting it to four 622Mbps LVDS outputs. The MAX3831 provides a 622MHz LVDS clock output, and the MAX3832 provides a 155MHz LVDS clock output. An internal frame detector looks for a 622Mbps SDH/SONET framing pattern and rolls the demux to maintain proper channel assignment at the outputs.

These devices also include an embedded pattern generator that enables a full-speed, built-in self-test (BIST). Two different loopback modes provide system test flexibility. A TTL loss-of-frame monitor is included. The MAX3831/MAX3832 are available in 64-pin TQFP-EP (exposed paddle) packages and are specified over the upper commercial (0°C to +85°C) temperature range.

Pin Configuration appears at end of data sheet.

Features

- **+3.3V Single Supply**
- **1.45W Power Dissipation (MAX3831)**
- **4-Channel Mux/Demux with Fully Integrated 2.488GHz Clock Generator**
- **Frame Detection Maintains Channel Assignment**
- **±7.5ns Elastic Store Range**
- **2.5ps RMS Serial-Data Output Random Jitter**
- **8ps Serial-Data Output Deterministic Jitter**
- **622Mbps LVDS Parallel Input/Output**
- **2.488Gbps Serial CML Input/Output**
- **On-Chip Pattern Generator Provides High-Speed BIST**
- **System Test Flexibility: System Loopback, Line Loopback**
- **Loss-of-Frame Indicator**

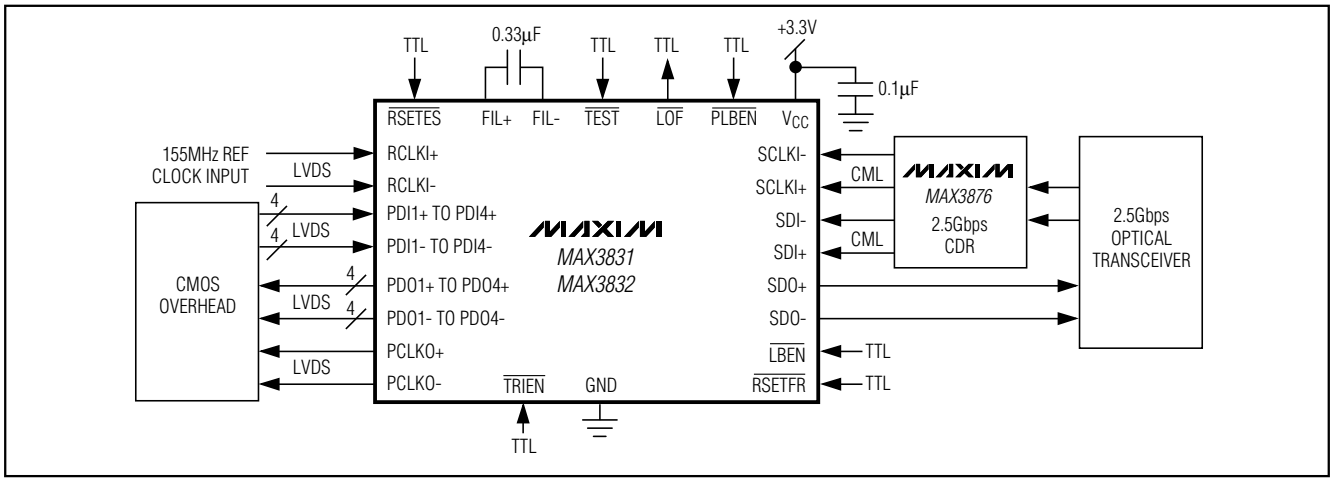
Applications

SDH/SONET Backplanes	ATM Switching Networks
High-Speed Parallel Links	Line Extenders
Intrarack/Subrack Interconnects	Dense Digital Cross-Connects

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3831UCB	0°C to +85°C	64 TQFP-EP
MAX3832UCB	0°C to +85°C	64 TQFP-EP

Typical Application Circuit



+3.3V, 2.5Gbps, SDH/SONET, 4-Channel Interconnect Mux/Demux ICs with Clock Generator

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_{CC}).....-0.5V to +5.0V
Input Voltage (LVDS, TTL).....-0.5V to (V_{CC} + 0.5V)
CML Input Voltage .....(V_{CC} - 0.8V) to (V_{CC} + 0.5V)
FIL+, FIL- Voltage.....-0.5V to (V_{CC} + 0.5V)
TTL Output Voltage .....-0.5V to (V_{CC} + 0.5V)
LVDS Output Voltage .....-0.5V to (V_{CC} +0.5V)
CML Output Currents.....22mA

Continuous Power Dissipation (T_A = +85°C) (Note 1)
64-Pin TQFP-EP (derate 40.0mW/°C above +85°C).....2.6W
Operating Temperature Range.....0°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Based on empirical data from the MAX3831/MAX3832 evaluation kit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML load = 50Ω ±1% to V_{CC}, all TTL inputs are open, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	CML inputs and outputs open, LVDS input V_{OS} = 1.2V (Note 2)	MAX3831		440	580	mA
			MAX3832		480	614	
LVDS INPUTS AND OUTPUTS							
Input Voltage Range	V_{IN}			0		2400	mV
Differential Input Threshold	V_{IDTH}			-100		+100	mV
Threshold Hysteresis	V_{HYST}				90		mV
Input Impedance	R_{IN}			85	100	115	Ω
Input Common-Mode Current	I_{OS}	LVDS input, V_{OS} = 1.2V			270		µA
Output Voltage High	V_{OH}					1.475	V
Output Voltage Low	V_{OL}			0.925			V
Differential Output Voltage	$\|V_{OD}\|$	Figure 1		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta\|V_{OD}\|$					±25	mV
Output Offset Voltage	V_{OS}			1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\|V_{OS}\|$					±25	mV
Differential Output Impedance		$\overline{TRIEN}$ = GND			>1		MΩ
		$\overline{TRIEN}$ = V_{CC}		80		120	Ω
Output Current		Short outputs together (Note 3)				12	mA
CML INPUTS AND OUTPUTS							
Differential Output Voltage	V_{ODp-p}			640	800	1000	mVp-p
Differential Output Impedance				85	100	115	Ω
Output Common-Mode Voltage					V_{CC} - 0.2		V
Single-Ended Input Voltage Range	V_{IS}			V_{CC} - 0.6		V_{CC} + 0.4	V
Differential Input Voltage Swing		Figure 2		400		1200	mVp-p
Differential Input Impedance				85	100	115	Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML load = 50Ω ±1% to V_{CC}, all TTL inputs are open, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TTL INPUTS AND OUTPUTS						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current High	I_{IH}	V_{IH} = 2.0V	-250		-50	µA
Input Current Low	I_{IL}	V_{IL} = 0	-550		-100	µA
Output Voltage High	V_{OH}	I_{OH} = 20µA	2.4			V
Output Voltage Low	V_{OL}	I_{OL} = 2mA			0.4	V
Output Impedance		$\overline{TRIEN}$ = GND		6		kΩ

Note 2: When $\overline{TEST}$ = GND, the pattern generator will consume an additional 30mA.
Note 3: Guaranteed by design and characterization.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML load = 50Ω ±1% to V_{CC}, all TTL inputs are open, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = +3.3V.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
4:1 MULTIPLEXER WITH CLOCK GENERATOR						
Parallel Input Data Rate				622.08		Mbps
Maximum Parallel Input Skew	t_{es}	(Note 5)		±7.5		ns
Serial-Data Output Rate				2.48832		Gbps
Serial-Data Output Rise/Fall Time	t_r, t_f	20% to 80%			120	ps
Serial-Data Output Random Jitter	SRJ	(Note 6)			3.5	ps_{RMS}
					40	ps_{p-p}
Serial-Data Output Deterministic Jitter	SDJ	(Note 7)		8	18	ps_{p-p}
1:4 DEMULTIPLEXER						
Serial-Data Input Rate				2.48832		Gbps
Serial-Data Setup Time	t_{SU}	Figure 3	100			ps
Serial-Data Hold Time	t_H	Figure 3	100			ps
Parallel-Data Output Rate	PDO±			622.08		Mbps
Parallel-Clock Output Frequency	PCLKO±	MAX3831		622.08		MHz
		MAX3832		155.52		
PCLKO to PDO_ Delay	t_{CLK-Q}	MAX3831, Figure 3	-100	90	300	ps
LVDS Output Rise/Fall Time		20% to 80%			350	ps
LVDS Differential Skew	t_{SKEW1}	Any differential pair			65	ps
LVDS Channel-to-Channel Skew	t_{SKEW2}	PDO1± to PDO4±		<100		ps
LVDS Three-State Enable Time				30		ns

Note 4: AC characteristics are guaranteed by design and characterization.
Note 5: Relative to the positive edge of the 155MHz reference clock. PDI1 to PDI4 aligned to RCLKI at reset.
Note 6: Measured with a reference clock jitter of <1ps_{RMS}.
Note 7: Deterministic jitter is the arithmetic sum of pattern-dependent jitter and pulse-width distortion.

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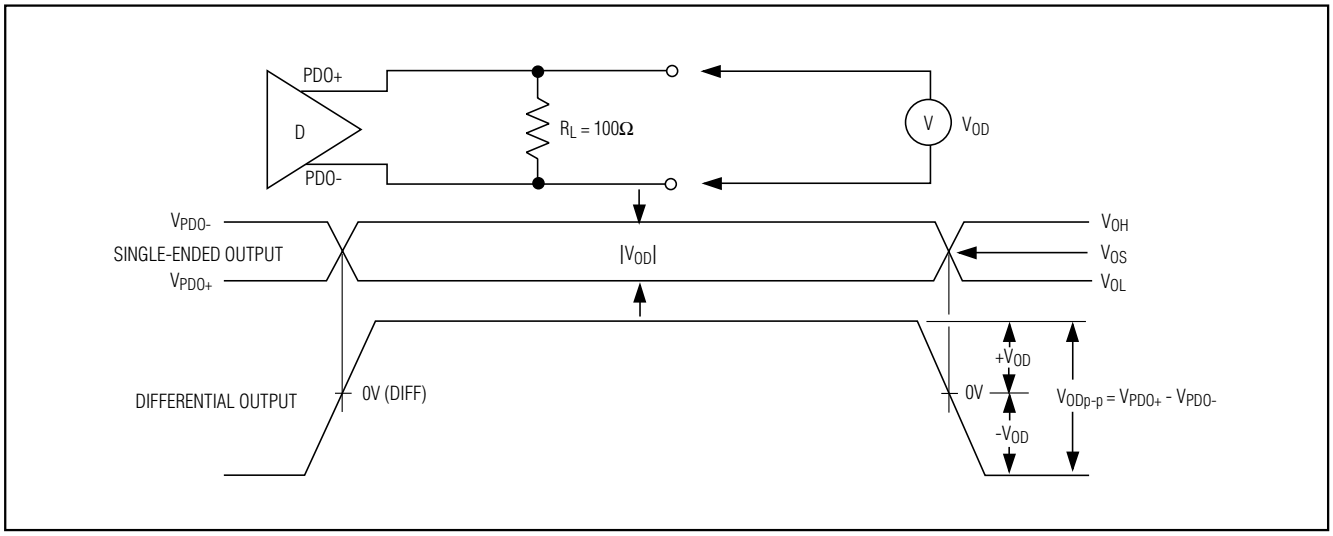


Figure 1. Definition of the LVDS Output

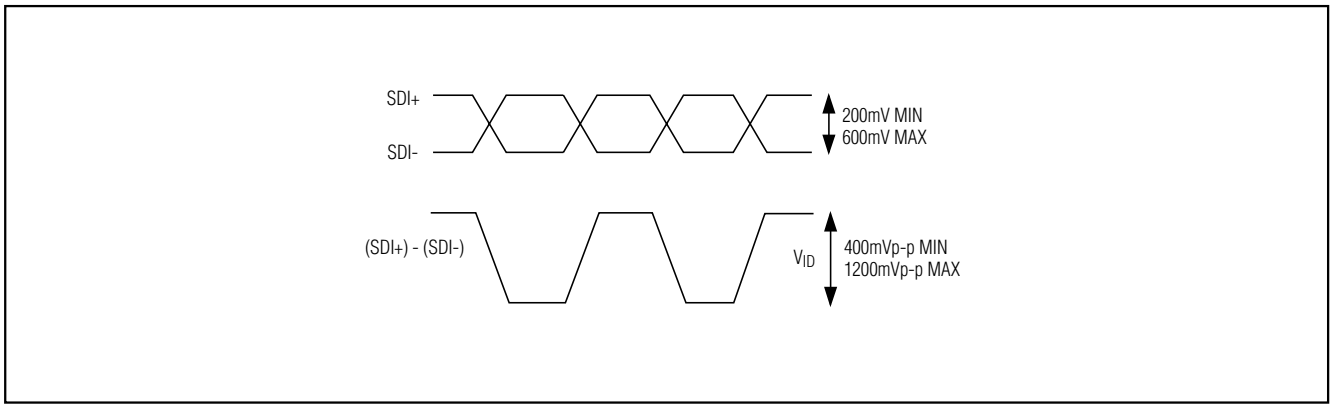
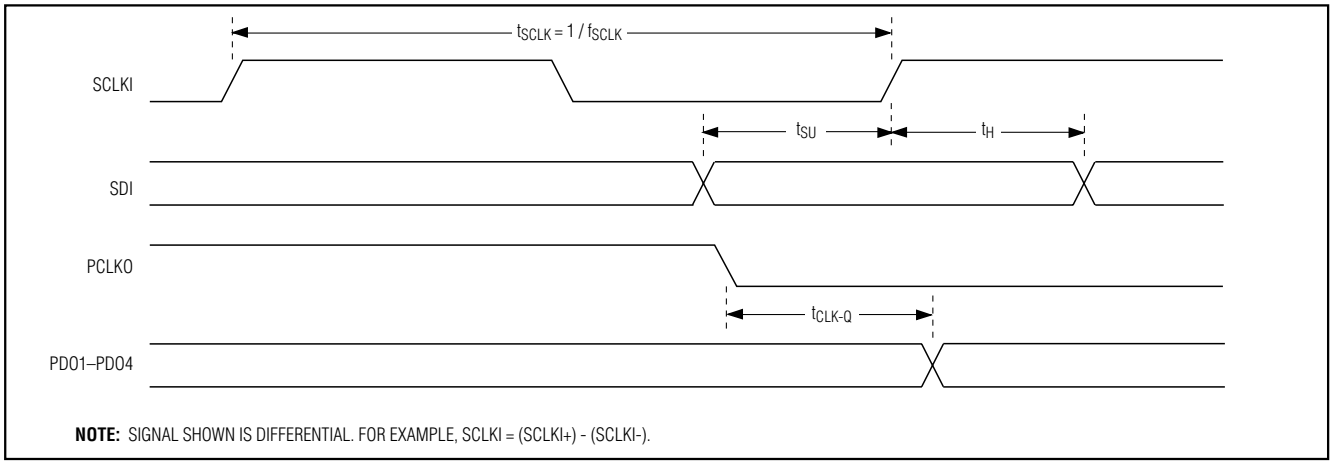


Figure 2. Definition of the CML Input



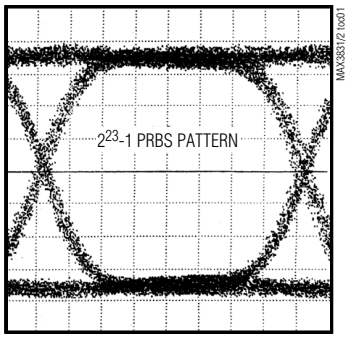
NOTE: SIGNAL SHOWN IS DIFFERENTIAL. FOR EXAMPLE, SCLKI = (SCLKI+) - (SCLKI-).

Figure 3. Timing Parameters

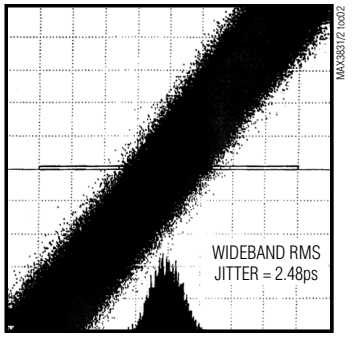
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

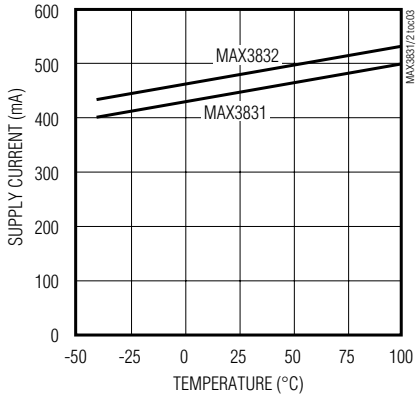
SERIAL-DATA OUTPUT EYE DIAGRAM



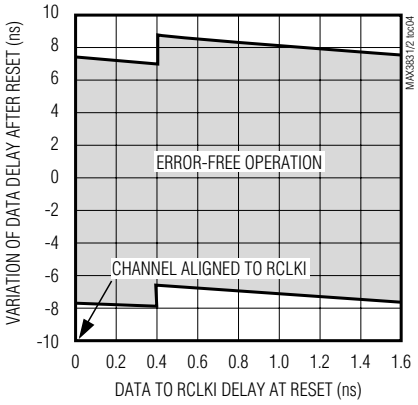
SERIAL-DATA OUTPUT JITTER



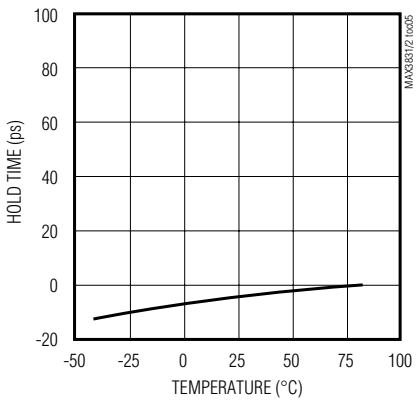
SUPPLY CURRENT vs. TEMPERATURE



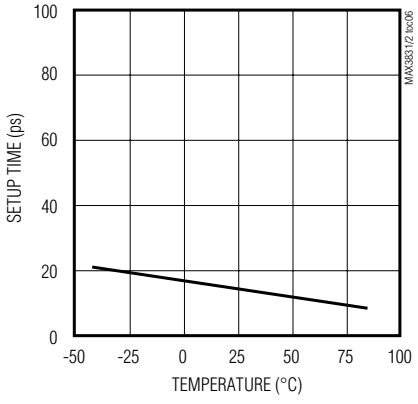
ELASTIC STORE RANGE



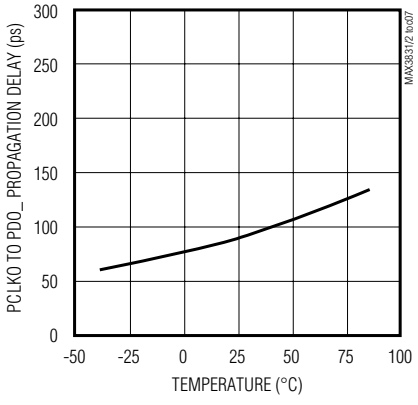
SERIAL-DATA HOLD TIME



SERIAL-DATA SETUP TIME



MAX3831
PARALLEL CLOCK-TO-DATA OUTPUT
PROPAGATION DELAY vs. TEMPERATURE



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Pin Description

PIN	NAME	FUNCTION
1, 16, 25, 28, 29, 32, 43, 48, 49, 60, 63	GND	Supply Ground
2, 5, 10, 13, 17, 24, 38, 55, 59, 64	V_{CC}	+3.3V Supply Voltage
3	SDO-	Negative CML Serial-Data Output, 2.488Gbps
4	SDO+	Positive CML Serial-Data Output, 2.488Gbps
6	$\overline{LBEN}$	Line Loopback Enable. When this TTL input is forced low, the CML serial-data inputs (SDI±) route directly to the CML serial-data outputs (SDO±). No other inputs or outputs are affected. An internal 15kΩ pull-up resistor pulls $\overline{LBEN}$ high for normal operation. See *Test Loopbacks*.
7	$\overline{TEST}$	Self-Test Enable. When this TTL input is forced low, the built-in pattern generator generates a standard OC-12 SONET-like frame of 12 A1s, 12 A2s, and 9696 bytes of 2^7 - 1 pseudo-random bits. This also enables an internal serial-system-loopback path. The CML inputs (SDI± and the SCLK±) and the LVDS inputs are ignored in this mode. An internal 15kΩ pull-up resistor pulls $\overline{TEST}$ high for normal operation.
8	SDI+	Positive CML Serial-Data Input, 2.488Gbps
9	SDI-	Negative CML Serial-Data Input, 2.488Gbps
11	SCLKI+	Positive CML Serial-Clock Input, 2.488GHz
12	SCLKI-	Negative CML Serial-Clock Input, 2.488GHz
14	PCLKO-	Negative LVDS Parallel-Clock Output, 622.08MHz (MAX3831); 155.52MHz (MAX3832)
15	PCLKO+	Positive LVDS Parallel-Clock Output, 622.08MHz (MAX3831); 155.52MHz (MAX3832)
18–23, 26, 27	N.C.	No Connection
30	$\overline{RSETFR}$	Frame Reset. When this TTL input is forced low, the frame detector and pattern generator are reset. The $\overline{LOF}$ output is also asserted low. An internal 15kΩ pull-up resistor pulls $\overline{RSETFR}$ high for normal operation.
31	$\overline{LOF}$	TTL Loss-of-Frame Output. Asserts low in a loss-of-frame condition.
33	$\overline{TRIEN}$	3-State Enable. When this TTL input is forced low, all TTL and LVDS outputs go into a high-impedance state. An internal 15kΩ pull-up resistor pulls $\overline{TRIEN}$ high for normal operation.
34, 36, 39, 41	PDO4- to PDO1-	Negative LVDS Parallel-Data Output, 622Mbps
35, 37, 40, 42	PDO4+ to PDO1+	Positive LVDS Parallel-Data Output, 622Mbps
44, 46, 50, 52	PDI4- to PDI1-	Negative LVDS Parallel-Data Input, 622Mbps
45, 47, 51, 53	PDI4+ to PDI1+	Positive LVDS Parallel-Data Input, 622Mbps
54	$\overline{PLBEN}$	Parallel System Loopback Enable. When this TTL input is forced low, the LVDS parallel inputs route through the elastic store to the LVDS parallel outputs. This bypasses the high-speed mux and demux. An internal 15kΩ pull-up resistor pulls $\overline{PLBEN}$ high for normal operation.
56	RCLKI-	Negative LVDS Reference Clock Input, 155.52MHz
57	RCLKI+	Positive LVDS Reference Clock Input, 155.52MHz

Pin Description (continued)

PIN	NAME	FUNCTION
58	$\overline{\text{RSETES}}$	Elastic Store Reset. The elastic buffer is centered on a rising edge of $\overline{\text{RSETES}}$, maximizing the elastic store range. Data must be present for 10µs before applying a pulse of at least 10ns. An internal 15kΩ pull-up resistor pulls $\overline{\text{RSETES}}$ high for normal operation.
61	FIL-	Negative PLL Filter Capacitor Input. Connect a 0.33µF capacitor between FIL+ and FIL-.
62	FIL+	Positive PLL Filter Capacitor Input. Connect a 0.33µF capacitor between FIL+ and FIL-.
EP	Exposed Paddle	Ground. This must be soldered to a circuit board for proper thermal performance (see *Package Information*).

Detailed Description

The MAX3831/MAX3832 use a 4:1 mux and 1:4 demux with an elastic store buffer to simplify SDH/SONET interconnect I/O routing. The 622Mbps low-voltage differential signal (LVDS) parallel inputs pass through the 10-bit elastic store buffer, which accommodates ±7.5ns skew on any single input relative to the 155MHz reference clock input RCLKI. This reference clock is required to synthesize the internal 2.488GHz clock used to drive the elastic store and 4:1 multiplexer. All TTL and LVDS outputs can be placed in a high-impedance state. See Figure 4 for a functional diagram.

The 4:1 mux bit-interleaves the parallel data, providing a 2.488Gbps CML serial output to the optical or electrical driver. The CML serial input receives the 2.488Gbps data, the demux deinterleaves it to 622Mbps and sends the data to the frame detector. The frame detector monitors one 622Mbps channel and rolls the demux into the proper channel assignment. The MAX3831/MAX3832 include high-speed, built-in self-test (BIST), which also allows testing of the 622Mbps parallel-system loopback and the 2.488Gbps line loopback.

Elastic Store Buffer

Each parallel-data input, PDI1 to PDI4, passes through its respective 10-bit elastic store buffer. Following an elastic store reset, this buffer accommodates ±7.5ns of skew on any input relative to the 155MHz reference clock. Figure 5 illustrates the elastic store buffer relationship with RCLKI. The Elastic Store Range graph in the *Typical Operating Characteristics* shows the amount of data skew tolerated.

Following a 10µs power-up period, the locations of the individual data-channel bit transitions are acquired, guaranteeing data preservation. The output of this block passes directly into the 4:1 mux. After power-up, the elastic store buffer must be reset by applying a low pulse on $\overline{\text{RSETES}}$ for at least 10ns.

Due to the inherent uncertainty of the data transitions between the parallel-data inputs there is no bit or frame alignment between these inputs. However, the demux ensures proper channel assignment is maintained.

Bit-Interleaved Multiplexer/ Demultiplexer

The MAX3831/MAX3832 use a bit interleave/deinterleave mux/demux. To guarantee channel assignment, one of the four channels is inverted before multiplexing to provide a reference for the frame detector during demultiplexing. After demultiplexing, the same channel is inverted back to the original data format.

Frame Detector

After a 2.5Gbps serial data is bit deinterleaved into four 622Mbps channels, an SDH/SONET frame detector monitors the fourth channel, looking for the 32-bit pattern (A1A1A2A2) in the OC-12 header. To maintain correct channel assignment, the demux outputs rotate until this 32-bit overhead pattern is reliably detected. A loss-of-frame output, $\overline{\text{LOF}}$, indicates when the received data is in or out of frame. When $\overline{\text{LOF}}$ goes high, the frame pattern is detected and the demux outputs are correctly assigned. When $\overline{\text{LOF}}$ is low, the frame detection circuitry is searching for the correct frame. A $\overline{\text{RSETFR}}$ (TTL, active low) is included to reset the frame detector when necessary.

The frame detector uses an algorithm to detect an in-frame condition and a loss-of-frame condition; this algorithm is implemented to meet the SONET in-frame and false-frame specs. The frame_search state will occur upon start-up or reset. In this state, the frame detector scans through the incoming serial data searching for the framing pattern in the channel 4 output of the demux. While in this state, if the framing pattern is not found within 250µs, the demux channels are shifted (rolled) and the frame search continues (Figure 6).

In-frame will be declared if two consecutive framing patterns are found at the correct byte locations within the SONET frame (9720 bytes). If this pattern is not pre-

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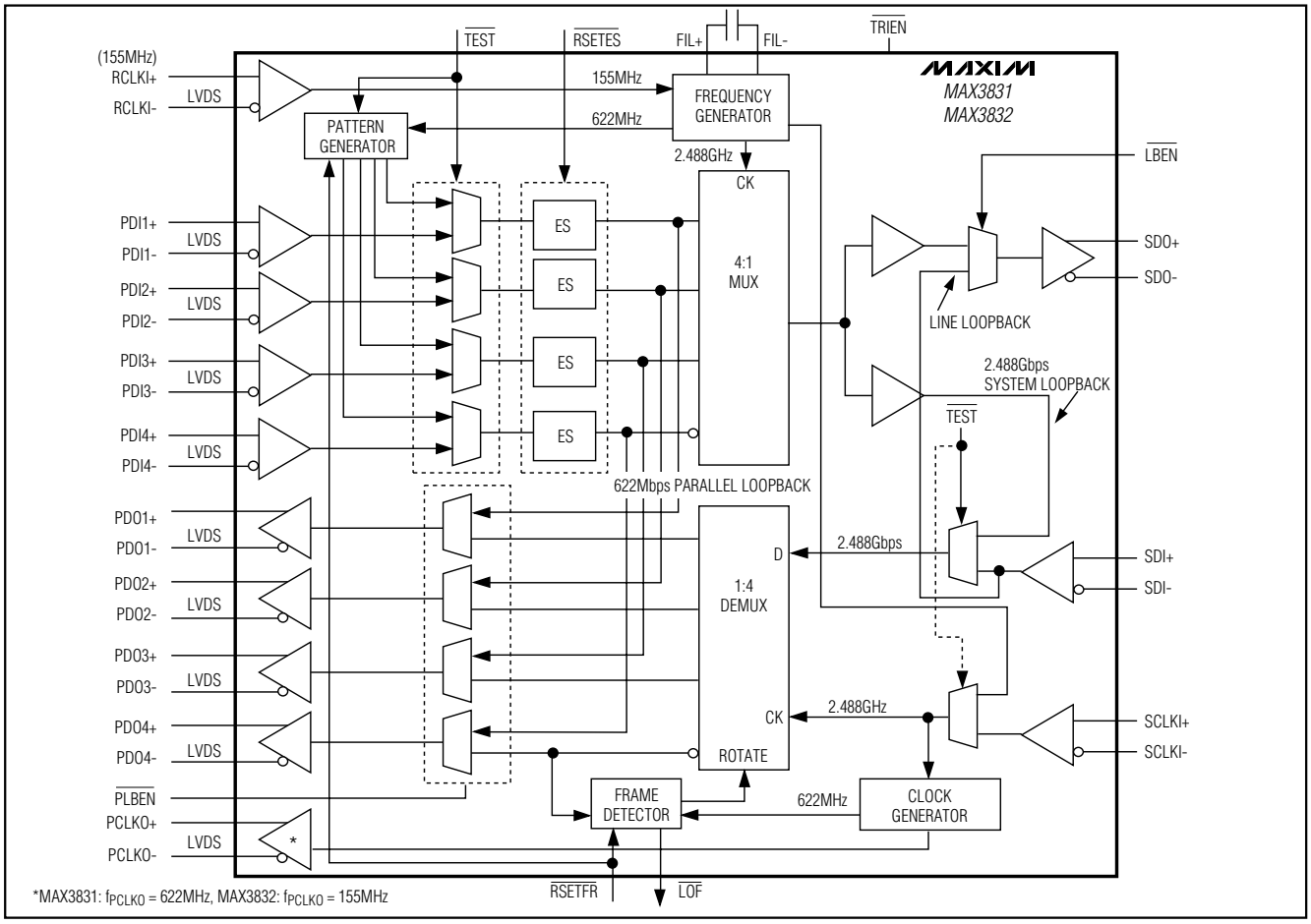

Figure 4. Functional Diagram

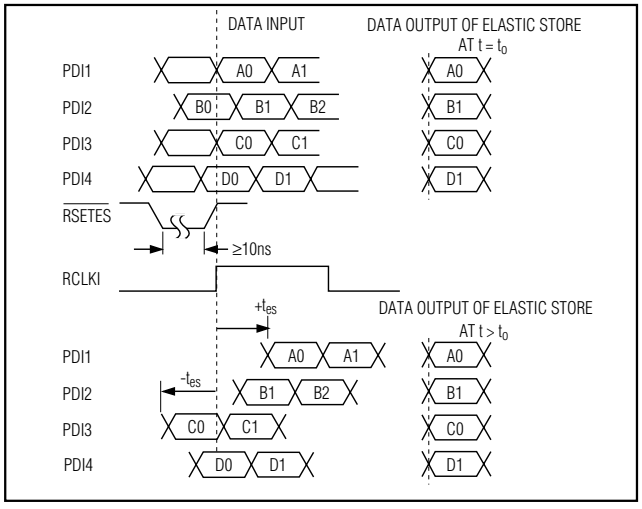

Figure 5. Example of Elastic Store Function

sent at the correct location (false frame), the state machine will return to the frame_search state described above. While in the in_frame state, each frame will be checked for a framing pattern at the correct location. Four consecutive false frames will cause the state machine to return to the frame_search state described above. The false-frame counter is reset with three or fewer consecutive false frames.

Built-In Self-Test with On-Chip Serial Loopback

An on-chip pattern generator can be enabled to produce a 622Mbps SDH/SONET-like transport overhead followed by a pseudorandom bit sequence. This consists of 12 A1s, 12 A2s, and a pseudorandom bit stream (PRBS = 2^7 - 1). When $\overline{TEST}$ is low, this pattern is distributed to all parallel inputs, bypassing the LVDS input buffers. Note, this pattern is skewed by one 622MHz

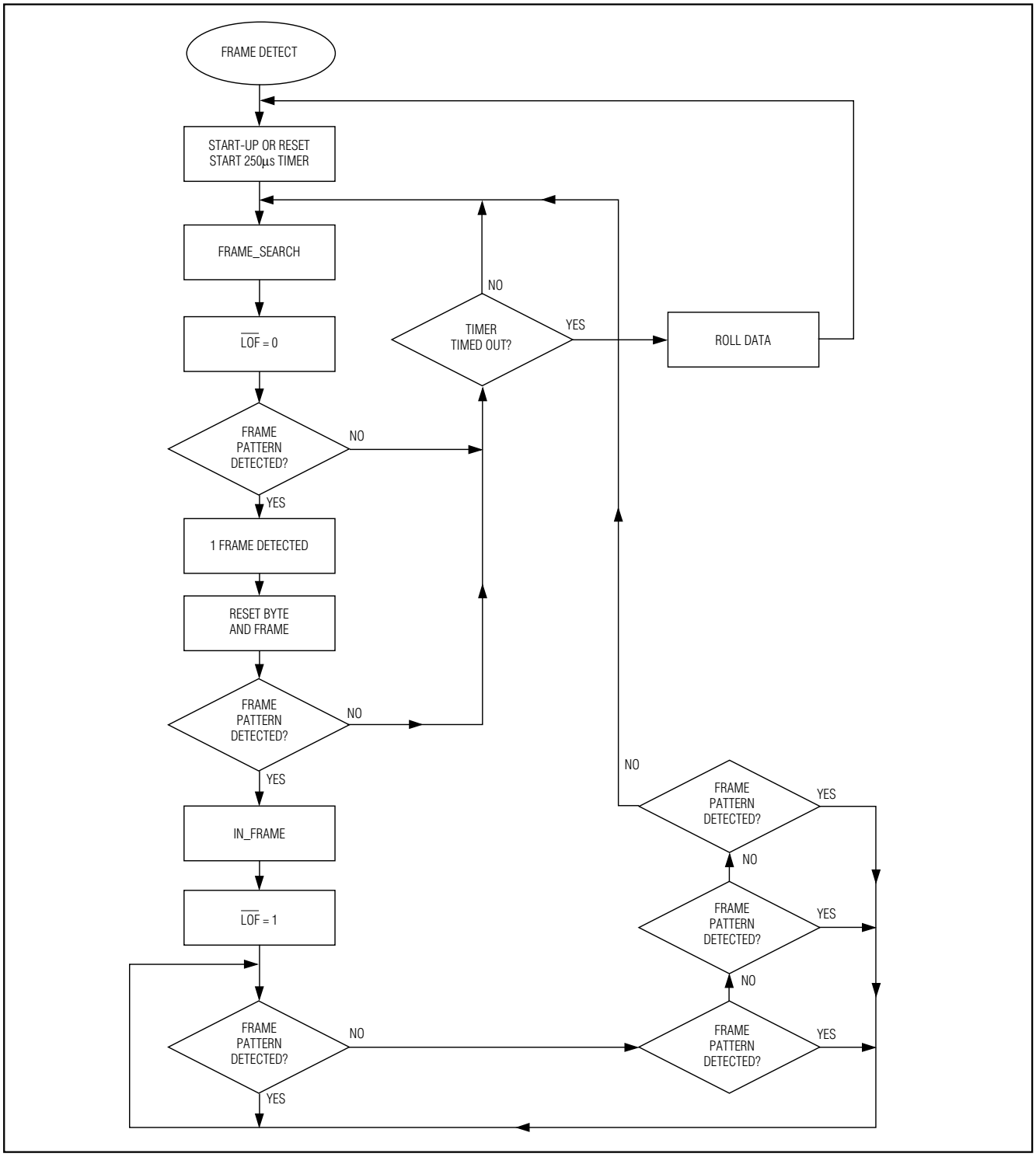

Figure 6. Frame Detection Flow Diagram

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clock cycle between each channel. In this test mode, serial data is internally looped back to the demux. All frame detect logic is exercised using this mode. The CML inputs (SDI± and SCLKI±) and LVDS inputs (PDI_±) are ignored in this mode. After the BIST mode is enabled, the loss-of-frame flag $\overline{LOF}$ goes high, indicating that the self-test has passed. In normal operation, $\overline{TEST}$ is left open (internally pulled high), disabling the pattern generator and accepting data from the parallel input channels.

Test Loopbacks

Two additional test loopbacks are provided: parallel system loopback and serial line loopback.

Parallel System Loopback

In parallel system loopback, four 622Mbps parallel input channels are phase aligned by an associated 10-bit elastic store and routed to the output LVDS buffers. This loopback is controlled by setting $\overline{PLBEN}$ low. Normal data transmission is resumed when $\overline{PLBEN}$ goes high (internally pulled high).

Serial Line Loopback

Serial line loopback is used for testing the performance of the optical transceiver and the transmission link. The received 2.488Gbps data stream is routed to the transmit CML output buffer. Line loopback is enabled when $\overline{LBEN}$ is asserted low. When $\overline{LBEN}$ is left open (internally pulled high), normal serial-data transmission resumes.

LVDS Parallel Interface

The MAX3831 parallel interface includes four OC-12 data inputs, a 155MHz reference clock input, four 622Mbps parallel-data outputs, and a 622MHz parallel-clock output (MAX3832, f_{PCLKO} = 155MHz). All parallel inputs and outputs are LVDS compatible to minimize power dissipation, speed transition time, and improve noise immunity. The 155MHz input signal at RCLKI requires a duty cycle between 40% and 60%.

The LVDS outputs go into a high-impedance state when $\overline{TRIEN}$ is forced low. This simplifies system checks by allowing vectors to be forced on the LVDS outputs.

CML Serial Interface

The MAX3831/MAX3832 provide a 2.488Gbps serial-data stream to a driver and accept 2.488Gbps serial data and a 2.488GHz clock signal from an external clock and data recovery device (MAX3876). The high-speed interface is CML compatible, resulting in lower system power dissipation and excellent performance (Figure 7).

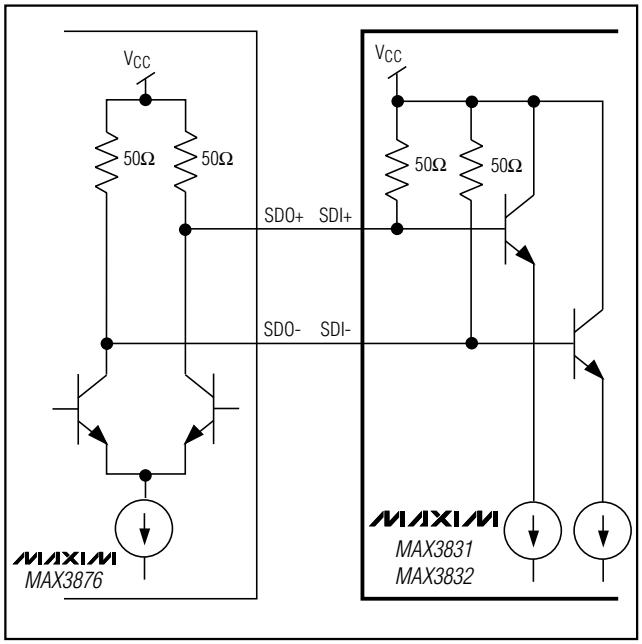


Figure 7. CML-to-CML Interface

Applications Information

Low-Voltage Differential Signal Inputs/Outputs

The MAX3831/MAX3832 have LVDS inputs and outputs for interfacing with high-speed digital circuitry. All LVDS inputs and outputs are compatible with the IEEE-1596.3 LVDS specification. This technology uses 250mV to 400mV differential low-voltage amplitudes to achieve fast transition times, minimize power dissipation, and improve noise immunity.

For proper operation, the parallel clock and data LVDS outputs (PCLKO+, PCLKO-, PDO_+, PDO_-) require 100Ω differential DC termination between the inverting and noninverting outputs. Do not terminate these outputs to ground. The parallel-data LVDS inputs (PDI_+, PDI_-) are internally terminated with 100Ω differential input resistance and therefore do not require external termination.

Interfacing with PECL/ECL Input Levels

When interfacing with differential PECL input levels, it is important to attenuate the signal while still maintaining 50Ω termination (Figures 8 and 9). Observe the common-mode input voltage specifications. AC-coupling is required if a V_{CC} other than 3.3V is used to maintain the input common-mode level (Figure 8).

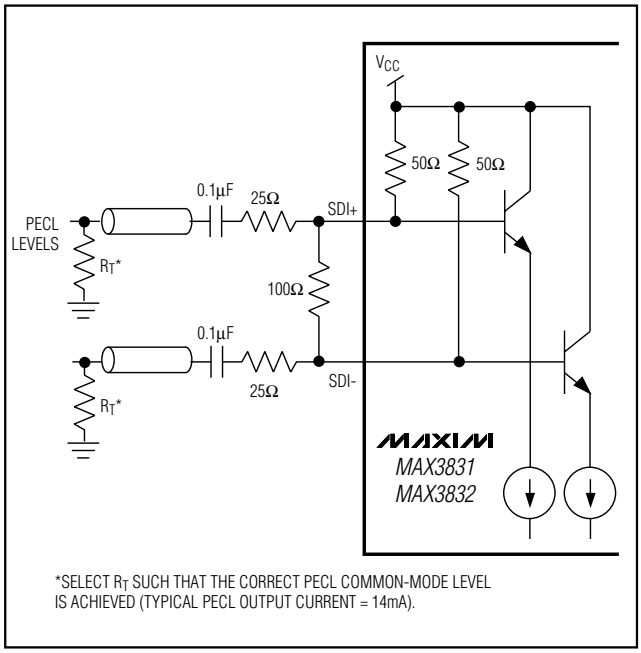


Figure 8. PECL-to-CML Interface

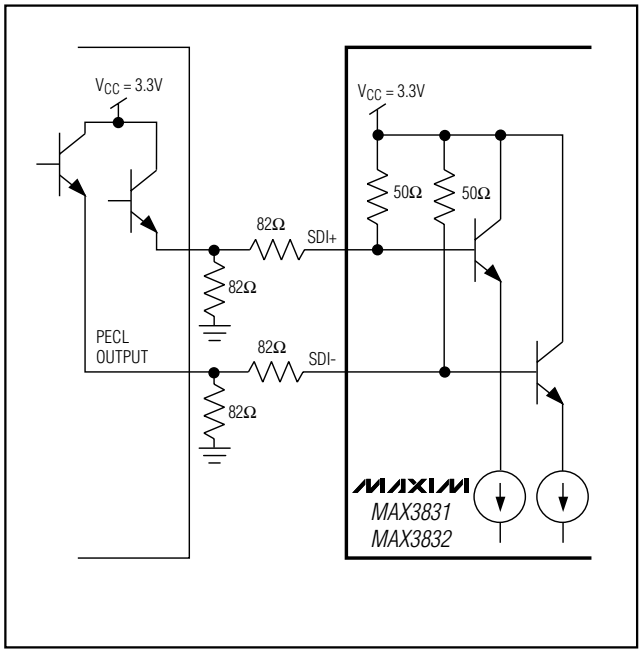


Figure 9. Direct Coupling of a PECL Output into the MAX3831/ MAX3832

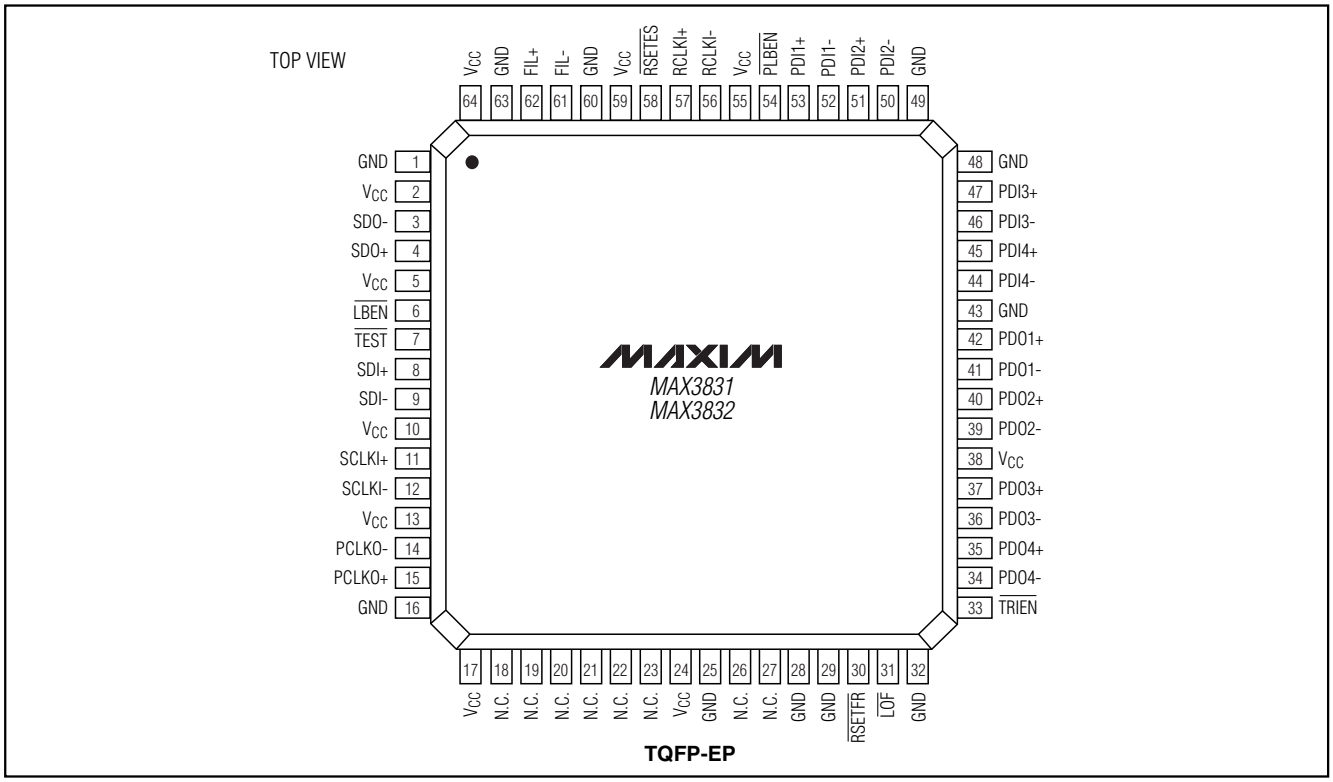
Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3831/MAX3832 high-speed inputs and outputs.

Place power-supply decoupling as close to V_{CC} as possible. To reduce feedthrough, take care to isolate the input signals from the output signals.

+3.3V, 2.5Gbps, SDH/SONET, 4-Channel Interconnect Mux/Demux ICs with Clock Generator

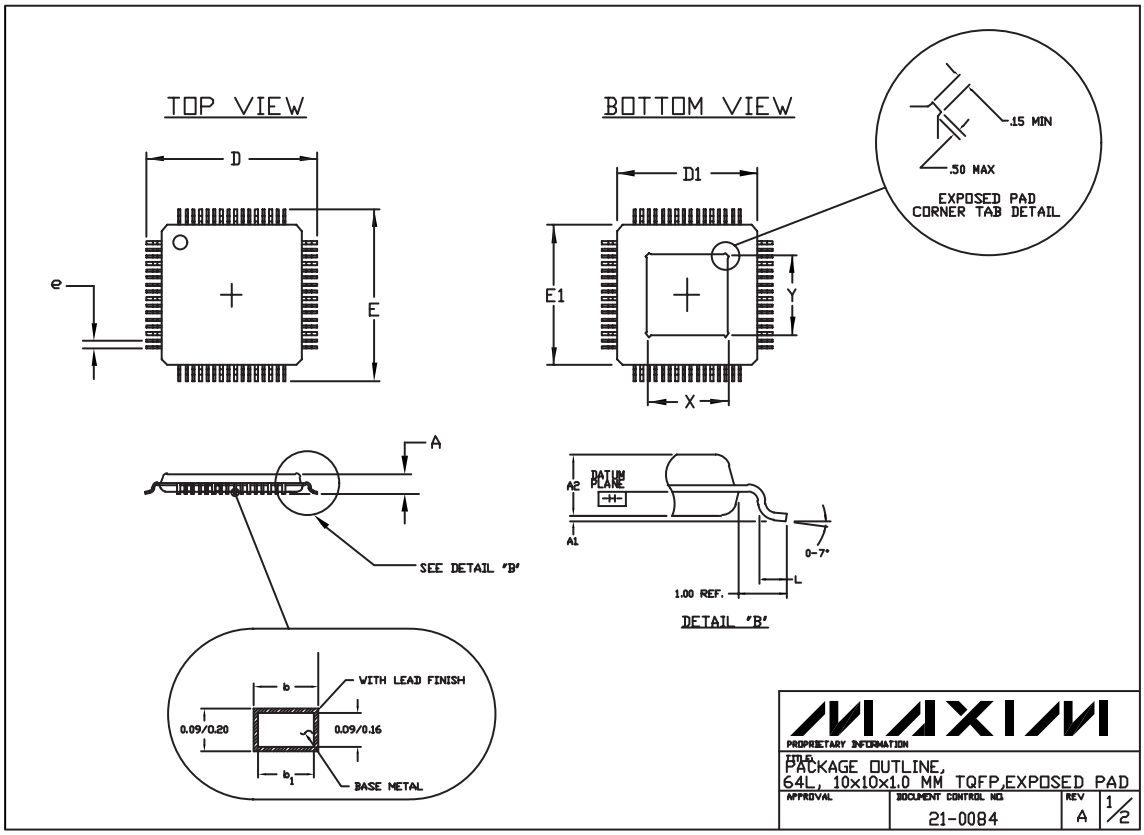
Pin Configuration



Chip Information

TRANSISTOR COUNT: 14,134

Package Information



+3.3V, 2.5Gbps, SDH/SONET, 4-Channel Interconnect Mux/Demux ICs with Clock Generator

Package Information (continued)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION AJ.
8. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
9. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS	
	AJ	
	MIN.	MAX.
A		1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	12.00 BSC.	
D_1	10.00 BSC.	
E	12.00 BSC.	
E_1	10.00 BSC.	
L	0.45	0.75
N	64	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23
X	4.7	5.30
Y	4.70	5.30

MAXIM PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 64L, 10x10x1.0 MM TQFP, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0084	A	2/2

NOTES

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